Space product assurance

High-reliability soldering for surface-mount and mixed technology

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Foreword

This Standard is one of the series of ECSS Standards intended to be applied together for the management, engineering and product assurance in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards. Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

This Standard has been prepared by the ECSS Executive Secretariat, reviewed by the Document and Discipline Focal point, and approved by the ECSS Technical Authority.

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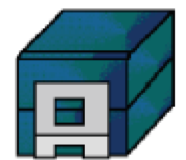
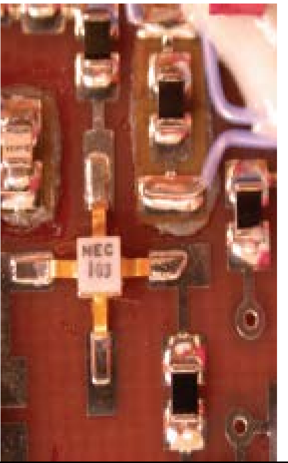
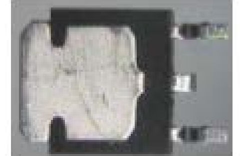
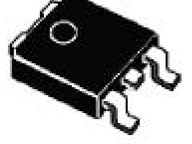
Introduction

This Standard prescribes requirements for electrical connections of leadless and leaded surface mounted devices (SMD) on spacecraft and associated equipment, utilising a range of substrate assemblies and employing solder as the interconnection media. The principal types of SMDs can be gathered in the following families:

Rectangular and square end-capped or end-metallized device with rectangular body e.g. end capped chip resistors and end capped chip capacitors.	
Bottom terminated chip device This type of device has metallised terminations on the bottom side only.	
Cylindrical or square end--capped devices with cylindrical body e.g. MELF.	
Castellated chip carrier device The main device of this type is leadless ceramic chip carrier (LCCC).	
Device with round, flattened, ribbon "L" and gull-wing leads e.g. small-outline transistor (SOT), small—outline package (SO), flat pack and quad flat pack (QFP). This family also comprises devices for through-hole mounting that have been reconfigured to surface mounting.	
"J" leaded device e.g. ceramic leaded chip carriers (CLCC) and plastic leaded chip carriers (PLCC).	

<table>
<tr><td>Area array devices
These devices are leadless (no leads). The interconnections between solder pads on the devices and solder pads on the PCB consist entirely of solder.
The devices have either solder balls (Ball Grid Array - BGA) or solder columns (Column Grid Array - CGA) applied to the solder pads on the devices prior to mounting on a PCB (normally done by the device manufacturer). The solder balls on the BGAs can consist of either eutectic solder or high temperature solder (5 - 10 % Sn) whereas the solder columns on the CGAs always consist of high temperature solder. Although BGAs are usually presented as a device family, there exist a large number of BGA devices with wide-ranging properties. The vast majority of BGA devices are nonhermetic.</td><td> </td></tr>
<tr><td>Device with Inward formed L--shaped leads
e.g. moulded tantalum chip capacitors.</td><td></td></tr>
<tr><td>Device with flat lug leads
This package has flat leads extending from the sides.</td><td></td></tr>
<tr><td>Leaded device with plane termination
e.g. Diode PAcKage (DPAK).</td><td>

DPAK</td></tr>
<tr><td>Leadless device with plane termination
This SMD package consists of three terminal pads, ceramic housing, and lid brazed together to form a hermetic semiconductor die carrier.</td><td> </td></tr>
</table>

1
Scope

This Standard defines the technical requirements and quality assurance provisions for the manufacture and verification of high-reliability electronic circuits based on surface mounted device (SMD) and mixed technology.

The Standard defines acceptance and rejection criteria for high-reliability manufacture of surface-mount and mixed-technology circuit assemblies intended to withstand normal terrestrial conditions and the vibrational g-loads and environment imposed by space flight.

The proper tools, correct materials, design and workmanship are covered by this document. Workmanship standards are included to permit discrimination between proper and improper work.

The assembly of leaded devices to through-hole terminations and general soldering principles are covered in ECSS-Q-ST-70-08.

Requirements related to printed circuit boards are contained in ECSS-Q-ST-70-10, ECSS-Q-ST-70-11 and ECSS-Q-ST-70-12 . The substrates covered by this document are divided into five classes in accordance with their average X and Y coefficient of thermal expansion (CTE).

The mounting and supporting of devices, terminals and conductors prescribed herein applies to assemblies designed to operate within the temperature limits of -55 °C to +85 °C.

For temperatures outside this normal range, special design, verification and qualification testing is performed to ensure the necessary environmental survival capability.

Special thermal heat sinks are applied to devices having high thermal dissipation (e.g. junction temperatures of 110 °C, power transistors) in order to ensure that solder joints do not exceed 85 °C.

Verification of SMD assembly processes is made on test vehicles (surface mount verification samples). Temperature cycling ensures the operational lifetime for spacecraft. However, mechanical testing only indicates SMD reliability as it is unlikely that the test vehicle represents every flight configuration.

.This Standard does not cover the qualification and acceptance of the EQM and FM equipment with surface-mount and mixed-technology.

The qualification and acceptance tests of equipment manufactured in accordance with this Standard are covered by ECSS-E-ST-10-03.

This standard may be tailored for the specific characteristics and constraints of a space project, in accordance with ECSS-S-ST-00.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references the latest edition of the publication referred to applies.

ECSS-S-ST-00-01	ECSS system — Glossary of terms
ECSS-M-ST-40	Space project management — Configuration and information management
ECSS-Q-ST-10-09	Space product assurance — Nonconformance control system
ECSS-Q-ST-20	Space product assurance — Quality assurance
ECSS-Q-ST-60	Space product assurance — Electrical, electronic and electromechanical (EEE) components
ECSS-Q-ST-60-05	Space product assurance — Generic requirements for hybrids
ECSS-Q-ST-70	Space product assurance — Materials, mechanical parts and processes
ECSS-Q-ST-70-01	Space product assurance — Cleanliness and contamination control
ECSS-Q-ST-70-02	Space product assurance — Thermal vacuum outgassing test for the screening of space materials
ECSS-Q-ST-70-08	Space product assurance — Manual soldering of high–reliability electrical connections
ECSS-Q-ST-70-10	Space product assurance — Qualification of printed circuit boards
ECSS-Q-ST-70-11	Space product assurance — Procurement of printed circuit boards
ECSS-Q-ST-70-12	Space product assurance — Design rules for printed circuit boards
ECSS-Q-ST-70-71	Space product assurance — Materials processes and their data selection
ECSS-E-HB-32-25	Space engineering — Mechanical shock design and

	verification handbook
MIL-STD-883 Method 2009	Test Method Standard, Microcircuits
IPC-TM-650: 2.6.3.3 Issue 2004	Test methods manual. Surface Insulation Resistance, Fluxes

3 Terms, definitions and abbreviated terms

3.1 Terms from other standards

a. For the purpose of this Standard, the terms and definitions from ECSS-S-ST-00-01C apply

b. For the purpose of this Standard, the terms and definitions from ECSS-Q-ST-60 Rev.2 apply, in particular for the following terms:

1. commercial component

3.2 Terms specific to the present standard

3.2.1 approval authority

entity that reviews and accepts the verification programme, evaluating the test results and grants the final approval

3.2.2 co-planarity

maximum distance between lowest and highest termination when device rests on flat surface

3.2.3 commercial device

see "**commercial component**" in ECSS-Q-ST-60.

3.2.4 electrical clearance

spacing between non-common electrical conductors on external layers of a printed circuit board assembly

NOTE The distance between conductors depends on the design voltage and DC or AC peaks. Any violation of minimum electrical clearance as a result of a nonconformance is a defect condition.

3.2.5 scavenging (leaching)

basis metal or metallization partly or wholly dissolved in melted solder during a soldering operation

3.2.6 selective plating

tin-lead plated solder pads connected to gold plated copper tracks

NOTE It is usually related to RF circuits.

3.2.7 solder balling (solder balls)

numerous spheres of solder having not melted in with the joint form and being scattered around the joint area normally attached by flux residues

NOTE Can be caused by incorrect preheating or poor quality solder.

3.2.8 tombstoning

chip devices lifting off one of their two terminal pads causing the chip to stand up like a tombstone

NOTE Normally caused by:

- bad design where one pad reaches solder reflow temperature before the other;
- different quantities of solder paste on each pad;
- different solderability of one pad or one termination with respect to the other.

3.2.9 underfill

encapsulant material deposited between a device and substrate used to reduce the mechanical stress resulting from a mismatch in the coefficient of thermal expansion (CTE) between the device and the substrate

3.2.10 dynamic wave soldering machine

system that achieves wave soldering and which consists of stations for fluxing, preheating, and soldering by means of a conveyer.

3.2.11 sensitive devices

devices having passed verification programme with identified cracks in excess of 25% into critical zone.

NOTE A list of known devices having verification anomalies, identified by more than one supplier is published on ESCIES.

NOTE It is the responsibility of industry to maintain its own listing applicable to their own boundary.

3.2.12 critical zone

area of the solder joint where crack length more than 33% causes verification failure.

NOTE With exception of TSOP device where no cracks in the critical zone are accepted.

3.2.13 device

package, component or part

3.2.14 reprocessing

to put any device or material through any additional process to change it prior to being used again

3.2.15 solder stand off

thickness of solder between the underside of the device termination and the surface of the PCB pad.

3.3 Abbreviated terms

For the purpose of this Standard, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
AAD	area array device
BGA	ball grid array
CBGA	ceramic ball grid array
CGA	column grid array
CCGA	ceramic column grid array
CLCC	ceramic leaded chip carrier
CTE	coefficient of thermal expansion
JEDEC	Joint Electron Device Engineering Council
LCCC	leadless ceramic chip carrier
MELF	metal electrode face bonded
	NOTE: Also known as minimelf or micromelf
MIP	mandatory inspection point
PCB	printed circuit board
PLCC	plastic leaded chip carrier
PID	process identification document
QFP	quad flat pack
r.m.s.	root-mean-square
SIR	surface insulation resistance
SMD	surface mounted device
SMT	surface-mount technology
SO	small outline
SOD	small outline device
SOT	small outline transistor
SOP	small outline package

TO	transistor outline
TSOP	thin small outline package

3.4 Nomenclature

3.4.1 Formal verbs

The following nomenclature apply throughout this document:

a. The word "shall" is used in this document to express requirements. All the requirements are expressed with the word "shall".

b. The word "should" is used in this document to express recommendations. All the recommendations are expressed with the word "should".

NOTE It is expected that, during tailoring, all the recommendations in this standard are either converted into requirements or tailored out.

c. The words "may" and "need not" are used in this document to express positive and negative permissions respectively. All the positive permissions are expressed with the word "may". All the negative permissions are expressed with the words "need not".

d. The word "can" is used in this document to express capabilities or possibilities, and therefore, if not accompanied by one of the previous words, it implies descriptive text.

NOTE In ECSS "may" and "can" have a complete different meaning: "may" is normative (permission) and "can" is descriptive.

e. The present and past tense are used in this document to express statement of fact, and therefore they imply descriptive text.

4 Principles of reliable soldered connections

The following are the general principles to ensure reliable soldered connections:

- Reliable soldered connections are the result of proper design, control of tools, materials, processes and work environments, and workmanship performed in accordance to verified and approved procedures, inspection control and precautions.
- The basic design concepts to ensure reliable connections and to avoid solder joint failure are as follows:
    - Stress relief is an inherent part of the design, which reduces detrimental thermal and mechanical stresses on the solder connections.
    - Where adequate stress relief is not possible materials are so selected that the mismatch of thermal expansion coefficients is a minimum at the constraint points in the device mounting configuration.
- The assembled substrates are designed to allow easy inspection.
- Since only the outer row of solder joints to area array packages can be visually inspected, inner rows are inspected using X-ray techniques. To facilitate X-ray inspection of the solder joints to BGAs, the solder pads have a teardrop design.
- Circuit designs for area array devices, (e.g. BGA, CGA) have clearance around the perimeter of these packages to ensure that reflow nozzles can perform rework or repair operations (see ECSS-Q-ST-70-28 [12]). The clearance depends on the equipment used for reworking and the height of adjacent components.

    NOTE Unpopulated areas on the underside of the substrate assist indirect heating for removal of these packages.

- Soldering to gold using tin-lead alloy can cause failure.

5 Process identification document (PID)

5.1 General

5.1.1 Purpose

The purpose of the PID is to ensure that a precise reference is established for the assembly processes approved in accordance with this Standard.

The PID provides a standard reference against which any anomalies occurring after the approval can be examined and resolved.

5.1.2 Document preparation

a. The supplier shall prepare the PID in conformance with DRD from Annex F.

b. The supplier shall provide a draft PID prior to any start of verification to the approval authority.

5.1.3 Content

a. <<deleted>>

b. <<deleted>>

5.1.4 Approval

a. The PID shall be submitted to the approval authority

b. The Approval authority shall approve the PID.

NOTE The approval can be achieved by PID signature or minutes of meeting being issued by the approval authority.

5.2 <<deleted>>

a. <<deleted>>

NOTE <<deleted>>.

b. <<deleted>>.

c. <<deleted>>

d. <<deleted>>

e. <<deleted>>

5.3 Process identification document updating

a. The PID shall be managed in accordance with ECSS-M-ST-40.

b. A PID shall represent the current verified manufacturing processes and production controls.

c. Any proposed changes to the PID shall be agreed by the Approval authority.

d. <<deleted>>

e. The PID, the summary table and the relevant applicable documents shall be re-issued and agreed by the approval authority at least every two years.

6 Preparatory conditions

6.1 Calibration

a. Records of tool calibration and verification shall be maintained.

6.2 Facility cleanliness

a. ECSS-Q-ST-70-08 shall apply for “Facility cleanliness”.

6.3 Environmental conditions

a. ECSS-Q-ST-70-08 shall apply for “Environmental conditions”.

6.4 Precautions against static charges

a. ECSS-Q-ST-70-08 shall apply for “Precautions against static charges”.

6.5 Lighting requirements

a. ECSS-Q-ST-70-08 shall apply for “Lighting requirements”.

6.6 Equipment and tools

6.6.1 Brushes

a. ECSS-Q-ST-70-08 shall apply for "Brushes".

6.6.2 Cutters and Pliers

a. ECSS-Q-ST-70-08, shall apply for "Cutters and Pliers".

6.6.3 Bending tools

a. ECSS-Q-ST-70-08 shall apply for "Bending tools".

6.6.4 Clinching tools

a. ECSS-Q-ST-70-08 shall apply "Clinching tools".

6.6.5 Insulation strippers

a. ECSS-Q-ST-70-08 shall apply for "Insulation strippers".

6.6.6 Soldering tools

a. ECSS-Q-ST-70-08 shall apply for "Soldering tools".

6.6.7 Soldering irons and resistance soldering equipment

a. ECSS-Q-ST-70-08 shall apply for "Soldering irons and resistance soldering equipment".

b. For surface mounted devices, the soldering tip shall not exceed 340 °C.

NOTE Based on the device manufacturer's recommendations, solder iron can be substituted by applying, for instance, hot air in order to avoid thermal shock.

6.6.8 Non-contact heat sources

a. <<deleted>>.

6.6.9 Solder baths

a. ECSS-Q-ST-70-08 shall apply for "Solder baths".

6.7 Soldering machines and equipment

6.7.1 General

a. Machines and equipment used to solder surface mount devices shall either be a type incorporating dynamic single or dual solder wave, or be of the solder reflow type.

NOTE Machines and equipment can be of two types:

- leadless and leaded devices specifically designed for surface mounting,
- devices initially designed for insertion mounting,

.

b. The soldering machine shall be grounded in order to avoid electrostatic discharge.

c. The supplier shall ensure that the soldering conditions do not exceed the values given by the individual device data sheets (e.g. maximum temperature to avoid internal melting, removal of marking ink, degradation of encapsulating plastic).

d. Temperature and time profiles for assembly shall be identified by the supplier and approved by the approval authority.

e. The supplier shall identify changes and implement a verification programme in compliance with the requirements from clause 14.13.

6.7.2 Dynamic wave-solder machines

a. Dynamic soldering machines shall be of automatic type and of a design offering the following:

1 Controllable preheating to drive off volatile solvents and to avoid thermal shock damage to the PCB and device packages.

2 The capacity to maintain the solder temperature at the printed circuit board assembly to within 5 °C of the established bath temperature throughout the duration of any continuous soldering run when measured 3,0 mm below the surface of the wave.

3 A wave system that limits shadowing and allows solder fillet formation.

4 Carriers made from a material that cannot contaminate, degrade or damage the printed circuit board or substrate nor transmit vibrations or shock stress from the conveyors to a degree permitting physical, functional or electrostatic damage to devices, board or substrate during transport through preheating, soldering and cooling stages.

5 An extraction system, either integral or separate, conforming to the requirements of clauses 6.2a and 6.3a.

6.7.3 Condensation (vapour phase) reflow machines

a. Condensation reflow machines shall conform to the following requirements:

1 Not transmit a movement or vibration into the assemblies being soldered that result in misalignment of devices or disturbed solder joints.

2 Be capable of preheating an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering.

3 Use a reflow fluid whose boiling point is a minimum of 12 °C above the melting point of the solder being used.

4 Maintain the preselected temperature to within ±5 °C in the reflow zone during soldering.

5 Include an extraction system that conforms to clauses 6.2a and 6.3a.

6.7.4 Hot gas reflow machines

a. Hot gas reflow machines shall conform to the following requirements:

1 Does not transmit movement or vibration to the assemblies being soldered which result in misalignment of devices or disturbed solder joints.

2 Preheats an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering.

3 Heats the area of the assembly to be soldered to a preselected temperature between 220 °C and 250 °C as measured on the substrate surface.

4 Prevents the reflow of adjacent devices.

5 Maintains the preselected reflow temperature within ±5 °C as measured at the substrate surface.

6.7.5 Shorted bar and parallel gap resistance reflow machines

a. Resistance reflow machines shall be of a design such that the system meets the following requirements:

1 Does not impart mechanical damage to the device leads.

2 Provides "time at temperature" control type of power supply.

3 Maintains the shorted bar or device lead to a preselected temperature that is a minimum of 12 °C above the melting point of the solder being used.

4 Maintains the dwell time at temperature to within 5 % of the preset value.

5 Provides a repeatable down force to within 15 % of the preset value.

6 Provides a system (e.g. an optical feature) to ensure that the shorted bar or electrode alignment with the device lead foot is within 20 % of the nominal lead foot length.

6.7.6 Convection and radiation reflow systems

a. Convection and radiation reflow machines shall be of design such that the system meets the following requirements:

1 Provides a controlled temperature profile and does not transmit movement or vibration into the assembly being soldered.

2 Preheats an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering.

3 Heats the area of the assembly to be soldered using focused or unfocussed energy, to a preselected temperature that is a minimum of 12 °C above the melting point of the solder being used as measured at laminate or substrate surface.

4 Maintains the preselected temperature to within 6 °C in the reflow zone during soldering.

6.7.7 Other equipment for reflow soldering

a. Other solder reflow systems can be approved for use by the Approval authority. This approval shall be subject to compliance with clauses 6.7.1 to 6.7.6.

6.8 Ancillary equipment

6.8.1 General

a. Equipment shall not generate, induce or transmit electrostatic charges to devices being placed.

6.8.2 Solder deposition equipment

a. Equipment used to deposit solder pastes shall be of a screening, stencilling, dispensing, roller coating or dotting type.

b. Equipment shall apply pastes of a viscosity and quantity such that the positioned device is retained on the board before and during soldering operations, ensuring self-centring and solder fillet formation.

c. Equipment used to apply solder preforms shall ensure alignment of the preform with the land or device lead and termination.

6.8.3 Automatic device placement equipment

a. Automatic or computer controlled equipment used for device placement shall be of the coordinate-driven pick-and-place type or of the robotic type.

b. The placement equipment used shall be of a type that:

1 prevents device or board damages

2 indexes devices with respect to the circuit

3 aligns the device leads or castellations with the board terminal areas.

6.8.4 Cleaning equipment and systems

a. ECSS-Q-ST-70-08 requirements on "Cleaning of PCB assemblies – General" and "Cleaning of PCB assemblies – Ultrasonic cleaning" shall apply.

6.8.5 Cleanliness testing equipment

a. ECSS-Q-ST-70-08 shall apply for "Cleanliness testing".

6.8.6 Magnification aids

a. Clause 13.1 shall apply.

6.8.7 X-ray inspection equipment

a. X-ray inspection shall not damage the devices.

b. X-ray equipment shall be calibrated in order to evaluate the total dose received by the devices during the inspection.

NOTE In order to minimize the dose given to the device, it is good practice to:

- Record the total dose received.
- Use off-line image analysis as much as possible.
- Use filters, optimizing the direction of the X-ray beam and masking sensitive areas.

c. The resolution of the X-ray equipment shall be able to detect solder balls having a diameter of 0,03 mm.

d. The sensitivity shall be demonstrated by means of actual 0,03 mm diameter solder balls, stuck to adhesive tape, attached to the multilayer board assembly being inspected.

NOTE <<deleted>>

6.8.8 Metallographic equipment

a. The metallographic equipment shall enable moulding, cross-sectioning and polishing of the solder interconnections.

7 Material selection

7.1 General

a. Material selection shall be performed in accordance with ECSS-Q-ST-70-71 and ECSS-Q-ST-70.

7.2 Solder

7.2.1 Form

a. Solder paste, ribbon, wire and preforms shall be used provided that the alloy and flux meet the requirements in clause 7.2.2.

b. Alloy for use in solder baths shall be supplied as ingots (without flux).

7.2.2 Composition

a. The solder alloy shall have a composition specified in Table 7-1.

NOTE 1 See ISO 9453 [13] or EN61190-1-3 for further details.

NOTE 2 The solder alloy used depends upon the application. See Annex E.2 for Guide for choice of solder type.

7.2.3 Solder paste

a. Solder paste shall conform to the requirements of clause 7.2.1.

NOTE The solder ball size and flux percentage are selected depending on the process employed, i.e. screen, stencil or needle application.

b. The metal purity shall be as specified in Table 7-1.

Table 7-1: Chemical composition of spacecraft solders

ESA designation	Sn min % - max %	Pb max %	In min % – max %	Sb max %	Ag min % – max %	Bi max %	Cu max %	Fe max %	Zn max %	Al max %	As max %	Cd max %	Other max %
63 tin solder	62,5-63,5	remain	-	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
62 tin silver loaded	61,5-62,5	remain	-	0,05	1,8-2,2	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
60 tin solder	59,5-61,5	remain	-	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
96 tin solder	remain	0,10	-	0,05	3,5-4,0	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
75 indium lead	max 0,25	remain	74,0-76,0	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
70 indium lead	0,00-0,10	remain	69,3-70,7	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
50 indium lead	0,00-0,10	remain	49,5-50,5	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
10 tin lead	9,0-10,5	remain	-	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08

7.2.4 Maintenance of paste purity

a. When purchased premixed or mixed in house, the purity of solder paste shall be maintained.

b. Manufacturers’ instructions shall be applied for the handling and storage of containers of solder paste purchased premixed.

c. Refrigerated solder paste shall reach room temperature before opening the container.

d. Neither paste purchased premixed nor paste mixed in-house shall be used if the use-by date or shelf life recommended by the manufacturer of the paste or paste constituents has expired.

e. When the solder paste’s shelf life has expired (see ECSS-Q-ST-70-22 [11]), it shall not be used unless:

1 relifing is performed

2 tests that include visual inspection and viscosity measurements (according to the manufacturer’s recommendations) are passed successfully.

f. When relifing is performed, and the material passes the specified tests, the new shelf life shall be half the initial shelf life.

g. Tools used for removing solder paste from the container shall not contaminate the paste dispensed or that remaining within.

7.3 Flux

7.3.1 Rosin based flux

a. ECSS-Q-ST-70-08 shall apply for "Rosin based flux".

7.3.2 Corrosive acid flux

a. ECSS-Q-ST-70-08 shall apply for "INH1 Corrosive acid flux".

7.3.3 Flux controls for wave-soldering equipment

a. A controlled method shall be established and implemented for wave-soldering machines such that the flux is not contaminated with remaining residues from previous non-space works.

7.4 Solvents

a. ECSS-Q-ST-70-08 shall apply for "Solvents".

7.5 Flexible insulation materials

a. ECSS-Q-ST-70-08 shall apply for "Flexible insulation materials".

7.6 Terminals

a. ECSS-Q-ST-70-08 shall apply for "Terminals".

7.7 Wires

a. ECSS-Q-ST-70-08 shall apply for "Wires".

7.8 Printed circuit substrates

7.8.1 Selection

a. Printed circuit boards and substrates shall be selected from the classes given in Table 7-2.

b. The class of board selected should have a CTE characteristic compatible with the CTE of the devices.

NOTE 1 The objective is that the impact of stresses from the environment is minimized.

NOTE 2 The warp and twist of multilayer boards can affect the geometry of the solder joints.

c. The warp and twist of the printed circuit multilayer board shall be in accordance with ECSS-Q-ST-70-11.

NOTE Symmetrical board design reduces warp and twist of the printed circuit board.

Table 7-2: Guide for choice of printed circuit boards and substrates

Class	Description	CTE (10^{-6}/°C) (X/Y plane of PCB)
1	Non-compensated printed board	14 – 17
2	Ceramic	5 –7
3	Compensated printed board	11 – 13
4	Compensated printed board	9 – 11
5	Compensated printed board	5 – 9

7.8.2 Class 1 - Non-compensated printed circuit board

a. Boards shall be made of materials and manufactured in conformance with the requirements of ECSS-Q-ST-70-10 and procured to ECSS-Q-ST-70-11.

NOTE Typical substrates are epoxy-woven glass and polyimide-woven glass.

7.8.3 Class 2 - Ceramic substrates

a. Hybrid microcircuits shall meet the requirements of ECSS-Q-ST-60-05.

NOTE Typical ceramic substrates are alumina and aluminium nitride.

7.8.4 Class 3 - Compensated printed circuit board

a. Boards shall be made of materials and manufactured in conformance with the requirements of ECSS-Q-ST-70-10 and procured in conformance with ECSS-Q-ST-70-11.

NOTE These boards can be reinforced with low CTE fibres such as aramid, quartz or carbon.

7.8.5 Class 4 - Compensated printed circuit board

a. Boards shall be made of materials and manufactured in conformance with the requirements of ECSS-Q-ST-70-10 and procured in conformance with ECSS-Q-ST-70-11.

NOTE CTE compensated boards use standard construction and are compensated with materials such as a distributed plane consisting of a low CTE material.

7.8.6 Class 5 - Compensated printed circuit board

a. Boards shall be made of materials and manufactured in conformance with the requirements of ECSS-Q-ST-70-10 and procured in conformance with ECSS-Q-ST-70-11.

NOTE CTE compensated boards use a standard construction with compensated materials such as low CTE substrate or cores. Typical cores are copper-plated invar and copper-plated molybdenum.

7.9 Devices

7.9.1 General

a. Devices and their finishes shall be selected from those approved in conformance with ECSS-Q-ST-60, for “manufacturer and component evaluation” and “Procurement control”.

NOTE It is good practice to select the device with solder finish applied over sintered metal on ceramic terminations having a diffusion barrier (nickel or equivalent diffusion layer) layer between the metallization and the solder finish.

b. <<deleted>> .

c. Solder may be applied to the terminations by hot dipping or by electro plating from a solution.

NOTE Devices with terminations finished by electro plating can impact the device wetting.

d. <<deleted>>.

e. The incoming inspection of each device batch shall include the verification of the termination composition (to avoid assembly of pure tin finish).

f. Pure tin finish with more than 97 % purity shall not be used.

NOTE This is due to the possibility of whisker growth and transformation to grey tin powder at low temperatures.

g. <deleted>>.

h. <<deleted>> .

i. Devices shall be capable of withstanding cleaning processes currently used in space projects.

j. Reprocessing shall not damage the device.

NOTE Reprocessing of ceramic chip capacitors is advised to be avoided due to potential crack formation.

k. If devices initially designed for insertion-mount application are used for surface mounting, they shall be of a type that can be surface-mount adapted.

l. The adaptation specified in the requirement 7.9.1k shall not functionally or physically degrade the device or the substrate to which the adapted device is to be attached.

m. Connectors shall be of a configuration incorporating either male or female quick-disconnect contacts and stress relief provision for the soldered connection of each individual contact when such connections are completed.

7.9.2 <<deleted>>

a. <<deleted>> .

b. <<deleted>> .

c. <<deleted>>

7.9.3 Moisture sensitive devices

a. Moisture sensitive devices shall be stored and handled in conformance with the device manufacturer's recommendations. See also clause 8.5b.

NOTE Many types of plastic encapsulated devices, particularly some plastic BGAs, are moisture sensitive.

b. When moisture sensitive devices are used, bakeout shall be performed in accordance with clause 8.5b.

7.9.4 <<deleted>>

a. <<deleted>> .

b. <<deleted>>

c. <<deleted>>

d. <<deleted>> .

e. <<deleted>>

7.10 Adhesives (staking compounds and heat sinking), encapsulants and conformal coatings

a. Adhesives shall be dispensable, non-stringing, and shall have a reproducible dot profile after application.

b. Adhesives, encapsulant and conformal coating shall be non-corrosive to devices and substrates.

c. The uncured strength shall be capable of holding devices during handling prior to curing.

d. Adhesives, encapsulants and conformal coatings shall conform to the outgassing requirements of ECSS-Q-ST-70-02.

e. Adhesives, encapsulants and conformal coatings shall have no adverse effects upon materials used on the substrate, or devices attached thereon.

NOTE The effects of some conformal coatings on the reliability of mounted SMDs are described in ESA SP-1173 [3].

f. Adhesives, encapsulants and conformal coatings shall be selected based on their thermal conductivity and dielectric properties (see ESA STM 265 [2]).

NOTE Some thermally conductive adhesives used to dissipate Joule heating are listed in ESA STM-265 “Evaluation of Thermally Conductive Adhesives as Staking Compounds during the Assembly of Spacecraft Electronics” [2].

g. The capability of the adhesives to meet their requirements shall be demonstrated by means of a verification test programme in conformance with clause 14.

h. Stress relief of device leads shall not be negated by the encapsulants or conformal coatings.

NOTE 1 This is particularly important at low service temperatures.

NOTE 2 The coefficient of expansion, glass transition temperature and modulus of adhesives used under devices for thermal reasons, for achieving stand-off heights or mechanical support during vibration, can be considered to ensure that the additional stress put on the solder joints does not degrade the solder joint reliability.

i. Bonding shall not be performed on fused tin lead except the case specified in the requirement 7.10j.

j. Bonding on fused tin lead may be accepted in case tin lead surface is limited to < 25% by area of the bonding surface and demonstrated by verification.

NOTE 1 Spread of bonding material onto surrounding areas can be accepted

NOTE 2 Adhesion to fused tin-lead finishes is poor (see also ECSS-Q-ST-70-28).

k. Bonding with epoxy adhesive directly to glass bodied devices shall not be used.

NOTE It is recommended to use a sleeve between glass and the epoxy adhesive.

8 Preparation for soldering

8.1 Preparation of devices and terminals

8.1.1 Preparation of wires and terminals

a. ECSS-Q-ST-70-08, clause "Preparation of conductors, terminals and solder cups" shall apply.

8.1.2 Preparation of surfaces to be soldered

a. ECSS-Q-ST-70-08, clause "Surfaces to be soldered" shall apply.

8.1.3 Degolding and pretinning of conductors

a. ECSS-Q-ST-70-08 shall apply for "Degolding and pretinning of conductors".

8.1.4 Alloying of pure tin finish

a. <<deleted>>.

NOTE 1 <<deleted>>.

NOTE 2 <<deleted>>

b. Pure tin device terminations shall be pretinned in compliance with requirements from ECSS-Q-ST-70-08 with full tin lead solder coverage.

NOTE 1 Pure tin terminations can be dipped into liquid solder as described in ECSS-Q-ST-70-08, clause 7.1.6 in order to replace the tin with tin-lead alloy.

NOTE 2 Reprocessing of ceramic chip capacitors is not recommended due to potential crack formation.

8.2 Preparation of solder bit

a. ECSS-Q-ST-70-08 shall apply for "Preparation of solder bit".

8.3 Handling

a. ECSS-Q-ST-70-08 shall apply for "Handling".

8.4 Storage

a. ECSS-Q-ST-70-08 shall apply for "Storage".

8.5 Baking of PCBs and moisture sensitive devices

a. "Baking of PCB's", shall apply for PCBs, partially assembled PCBs and assemblies going through reworking.

b. Baking of moisture sensitive devices shall be implemented before any reprocessing or assembly process.

NOTE This is to counteract the "popcorn" effect in soldering using oven or vapour phase reflow techniques.

c. Baking times and temperatures, for moisture sensitive devices, shall be documented.

NOTE 1 Typical baking conditions are from 6 h to 24 h at 125 °C depending on the JEDEC classification, except for devices delivered in reels for which a lower temperature and longer time are used.

NOTE 2 It is good practice to store devices under nitrogen, dry air (20 % RH maximum) or partial vacuum.

d. Baking of unpopulated PCB should be made as a minimum of 8 hours at 120° C.

e. Vacuum baking of PCB or alternative baking may be performed provided demonstration of absence of measling or delamination.

f. Baking of populated PCB shall be performed when the PCB has been kept under clean room conditions for more than 72 hours

g. Baking of populated PCB shall be made at a temperature which does not degrade the devices or assembly.

NOTE To limit the bake out operation, which could induce later failure, the PCB can be stored in dry environment after the baking.

9 Mounting of devices prior to soldering

9.1 General requirements

a. ECSS-Q-ST-70-08, “Mounting of components – General” shall apply.

9.2 Lead bending and cutting requirements

a. ECSS-Q-ST-70-08, clause “Lead bending requirements” shall apply.

9.3 Mounting of terminals to PCBs

a. ECSS-Q-ST-70-08 shall apply for "Mounting of terminals to PCBs".

9.4 Lead attachment to through holes

a. ECSS-Q-ST-70-08 shall apply for "Lead attachment to through holes".

9.5 Mounting of devices to terminals

a. ECSS-Q-ST-70-08 shall apply for "Mounting of components to terminals".

9.6 Mounting of connectors to PCBs

a. ECSS-Q-ST-70-08 shall apply for "Mounting of connectors to PCBs".

9.7 Surface mount requirements

9.7.1 General

a. Devices to be mounted shall be designed for, and be capable of withstanding the soldering temperatures of the particular process being used for fabrication of the assembly.

b. Surface mounted devices may be mounted on either one side or both sides of a printed circuit assembly.

c. Devices incapable of withstanding machine soldering temperatures shall be hand soldered in a subsequent operation.

d. Supplier shall ensure that degolding, pretinning, reprocessing and soldering conditions do not exceed the device suppliers mandated processing conditions.

NOTE 1 In case of non-applicable mounting notice from a component manufacturer, a company can apply different soldering temperature compliant with clause 6 after successful verification tests as described in clause 14 showing there is no degradation of these components.

NOTE 2 To mount component by hand soldering at very low temperature can degrade reliability of component and pad PCB by increasing the duration of soldering necessary to obtain an acceptable solder joint.

e. Supplier shall ensure that degolding and pretinning has been performed such that the solder fillet is not in contact with the gold or AuSn intermetallic.

f. Supplier shall ensure repeatability of the mounting when artificial standoff is adopted.

9.7.2 Stress relief

a. When Class 1 boards are employed (i.e. glass fibre epoxy or glass fibre polyimide resins with no CTE compensation), the supplier shall accommodate CTE mismatch by the mounting technology.

NOTE 1 Pure eutectic tin-lead solder or indium-lead solder provide better stress relief (due to their ductility) than those with additional elements, e.g. antimony, gold.

NOTE 2 Leadless devices with e.g. end-cap terminations, metallizations, can have some stress relief (such as additional foil or wire leads, possibly attached by welding or high melting point solder).

NOTE 3 A solder stand-off (see Figure 11-1, dimension “X”) can assist stress relief; in this situation, the CTE mismatch strain is taken up by the ductile solder.

NOTE 4 CTE compensated substrates or laminates of Classes 2 - 5 (listed in clause 7.8) can be selected to match the CTE of large leadless packages.

9.7.3 Registration of devices and pads

a. Devices shall be mounted on their associated terminal pads (lands).

b. The spacing between conductive elements shall not be reduced below the minimum electrical spacing specified in ECSS-Q-ST-70-12.

NOTE Some surface mounted devices that are not bonded to the PCB can self-align during the soldering process. It is the registration after soldering that is important.

9.7.4 Lead forming

a. The leads of leaded surface mount devices shall be formed to their final configuration prior to mounting.

b. Forming shall not degrade the solderability or cause loss of plating adhesion to the leads.

c. Forming shall not cause mechanical damage to the leads or attachment seals.

d. Leads of dual-in-line and gull-wing packages, flat-packs and other multileaded devices shall be dressed (mechanically re-aligned) to ensure co-planarity.

9.7.5 Mounting devices in solder paste

a. Both leaded and leadless surface mounted devices shall be mounted in solder paste prior to reflow soldering.

NOTE It is good practice to optimize the pick and place mounting force on the device lead, ball or column.

b. The solder paste deposited on each solder land shall be visually inspected for registration and coverage by the operator prior to mounting the devices.

NOTE <<deleted>>.

9.7.6 Leadless devices

a. Devices shall not be stacked.

b. Devices shall not bridge the spacing between other parts or devices such as terminals or other properly mounted devices.

c. The active element shall be mounted with that surface facing away from the printed circuit board or substrate, except the case specified in the requirement 9.7.6g.

NOTE See Figure 9-1 for details.

d. Devices that are bonded to the PCB prior to wave- or reflow-soldering shall be placed so that the requirements after soldering given in clause 11 are met.

e. The adhesive shall not extend onto the solder pads.

f. Increased solder stand-off may be achieved by removable spacers or other techniques in conformance with assembly process procedures.

NOTE Examples of increased solder stand-off is elevation as shown in clause 11.5.5.

g. The active element may be facing the substrate in case required by electrical performance.

NOTE For example: RF applications.

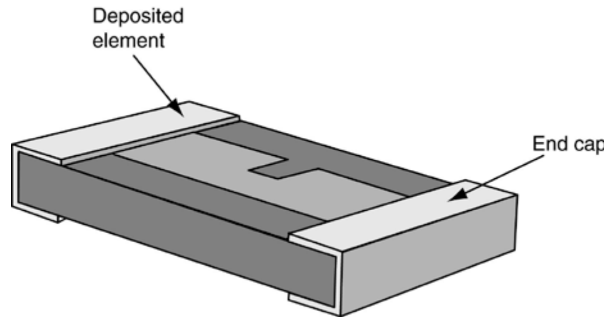


Figure 9-1: Exposed element

9.7.7 Leaded devices

a. Surface mounting of leaded (round or flattened cross section) devices shall be parallel to the board surface.

9.7.8 <<deleted>>

a. <<deleted>>

9.7.9 <<deleted>> Staking of heavy devices

a. Staking compounds shall be selected in conformance with clause 7.10.

NOTE 1 Staking shall be undertaken to clean interfaces

NOTE 2 Some surfaces can be prepared to enhance the adhesion (e.g. by mechanical abrasion).

b. <<deleted>>

NOTE <<deleted>>

c. Staking compounds shall be mixed and cured in accordance with the manufacturer's procedures.

d. The process of applying the staking compound shall be documented by a written procedure or by configured drawings which define the location

of the staking compound, the shape and the spread area (between device bottom surface and substrate upper surface).

e. The staking compound shall not negate the stress relief of the device, nor come into contact with surrounding devices.

f. All devices except area arrays weighing more than 5 g should be staked.

NOTE 1 This is to minimize shock and vibration loading on the leads

NOTE 2 The staking compound can be applied either before or after soldering in conformance with the supplier’s process identification document.

10 Attachment of conductors to terminals, solder cups and cables

a. ECSS-Q-ST-70-08 shall apply for “Attachment of conductors to terminals, solder cups and cables”.

11 Soldering to printed circuit boards

11.1 General

a. ECSS-Q-ST-70-08, clause "Soldering to terminals and printed circuit boards – General" shall apply.

11.2 <<deleted>>

a. <<deleted>> .

11.3 Solder applications to PCBs

a. ECSS-Q-ST-70-08 shall apply for "Solder applications to PCBs".

11.4 Wicking

a. ECSS-Q-ST-70-08 shall apply for "Wicking".

11.5 Soldering of SMDs

11.5.1 General requirements

a. Devices shall not be mounted on flexible substrates as defined "flexible printed boards" in ECSS-Q-ST-70-10.

b. Soldering to gold with tin/lead alloys shall not be performed except the case specified in the requirement 11.5.1g.

NOTE See also clause 8.1.3.

c. Devices shall not be stacked nor bridge the space between other devices or devices (e.g. as terminals or other properly mounted devices).

d. Positioning of devices shall not reduce the specified minimum electrical clearance to adjacent tracks or other metallized elements in conformance with requirements from clause 13 and clause 14 of ECSS-Q-ST-70-12.

e. Non-axial-leaded devices (e.g. small outline, flat-packs and similar devices) shall be mounted with all leads seated on a terminal area to ensure mechanical strength.

f. Solder shall cover and wet the solderable surfaces as specified in clause 13.2.

g. Soldering to gold finish less than 0,1 µm with tin-lead may be performed in case the following conditions are met:

1. PCB is qualified in compliance with the requirements of clause 6 of ECSS-Q-ST-70-10.
2. Assembly verification programme is reviewed and accepted by the Approval authority.
3. Assembly verification is compliant to requirements of clause 14.

h. The PCB footprint of the device shall be designed in compliance with the requirements from ECSS-Q-ST-70-12 to ensure the entire device termination surface is in contact.

i. The device positioning shall be such that visual inspection can be undertaken.

j. When visual inspection is difficult, due to surrounding devices, a step inspection shall be performed.

11.5.2 End-capped and end-metallized devices

a. There shall be no discernible discontinuities in the solder coverage of the terminal areas of devices.

b. Solder shall not encase any portion of the body of the device following reflow.

c. The solder joints to these devices shall meet the dimensional and solder fillet requirements of Table 11-1 and Figure 11-1.

NOTE End-capped and end-metallized devices having terminations of a square or rectangular configuration (such as chip resistors, chip capacitors, MELFs and similar leadless discrete devices) can have three or five face terminations, as shown in “a” and “b” in Figure 11-1.

Table 11-1: Dimensional and solder fillet requirements for rectangular and square end capped devices

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
End overhang	B	Not permitted
Minimum lap contact	L	75% single terminal length only
Minimum fillet height	M	X + 0,3 × H or X + 0,5 mm whichever is less
Solder Stand-off (elevation)	X	Present
Maximum tilt limit	C	10°

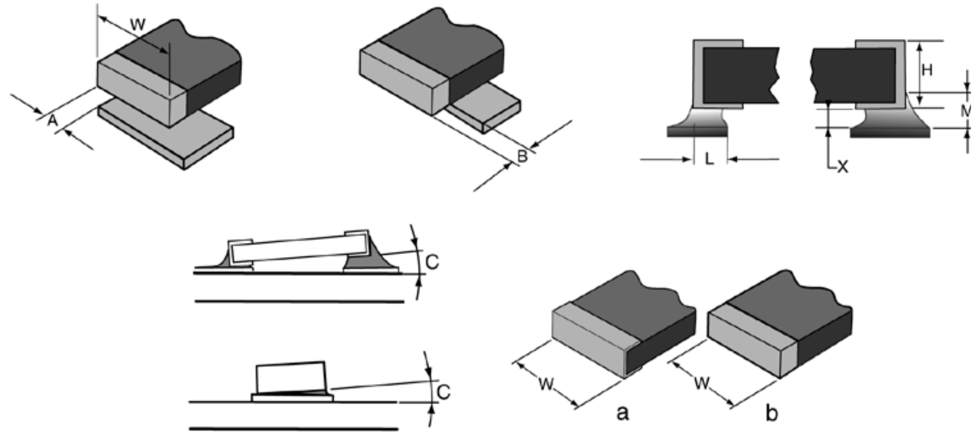


Figure 11-1: Mounting of rectangular and square end-capped and end-metallized devices

11.5.3 Bottom terminated chip devices

a. Devices having metallized terminations on the bottom side only (e.g. discrete chip devices, ceramic leadless chip carriers) shall meet the dimensional and solder fillet requirements of Table 11-2 and Figure 11-2.

b. Solder fillet shall show acceptable wetting on all visible side.

Table 11-2: Dimensional and solder fillet requirements for bottom terminated chip devices

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
End overhang	B	Not permitted
Minimum lap contact	L	Entire terminal of device
Solder Stand-off (elevation)	X	Present
Maximum tilt limit		10°

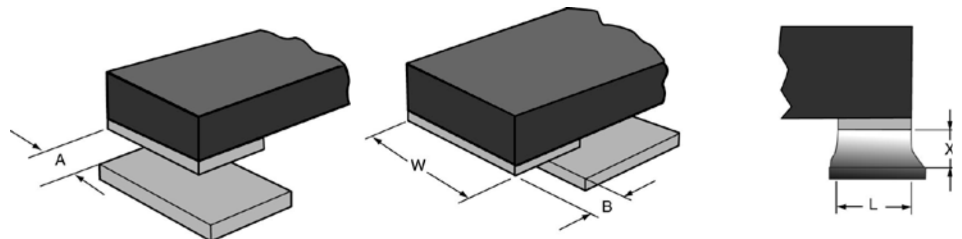


Figure 11-2: Mounting of bottom terminated chip devices

11.5.4 Cylindrical end-capped devices

a. Solder joints to devices having cylindrical terminations (such as MELF and SOD devices) shall meet the dimensional and solder fillet requirements of Table 11-3 and Figure 11-3.

Table 11-3: Dimensional and solder fillet requirements for cylindrical end-capped devices

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,25 × D
End overhang	B	Not permitted
Minimum fillet width	E	0,5 × D
Minimum fillet height	M & F	X + 0,3 × D or X + 1,0 mm whichever is less
Minimum side fillet length	L	0,75 × T single termination only
Solder Stand-off (elevation)	X	Present
Maximum tilt limit		10°

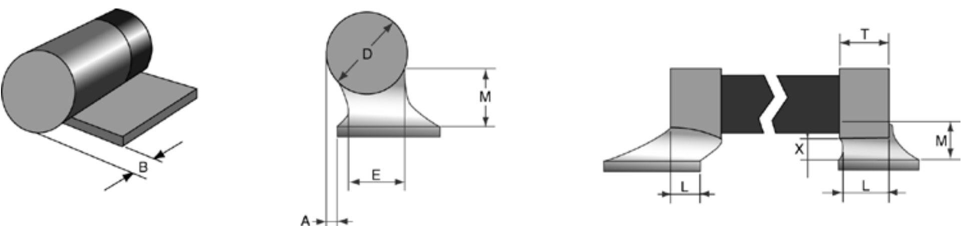


Figure 11-3: Mounting of cylindrical end-capped devices

11.5.5 Castellated chip carrier devices

a. Joints to castellated device terminations shall meet the dimensional and solder fillet requirements of Table 11-4 and Figure 11-4.

NOTE 1 The stand-off enables adequate cleaning beneath the assembled LCCC and also to enhance solder fatigue life (see also clause 9.7.6f)

NOTE 2 <<deleted>>

Table 11-4: Dimensional and solder fillet requirements for castellated chip carrier devices

Parameter	Dimension	Dimension limits
Maximum side overhang	A	Zero
Maximum fillet length	E	P
Minimum fillet height	M	0,50 × H (H= Castellation metallisation height)
Solder Stand-off (elevation)	X	Present
Underneath lap connection		Entire terminal of device

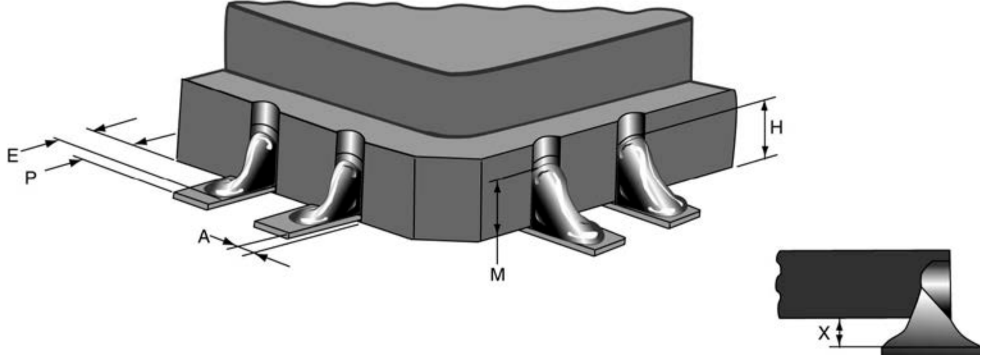


Figure 11-4: Mounting of castellated chip carrier devices

11.5.6 Devices with round, flattened, ribbon, "L" and gull-wing leads

a. Solder joints formed to round, flattened, ribbon, "L" and gull-wing shaped leads shall meet the dimensional and solder fillet requirements of Table 11-5 and Figure 11-5.

b. Solder fillet shall be visible on the side of the terminal lap connection.

Table 11-5: Dimensional and solder fillet requirements for devices with round, flattened, ribbon, "L" and gull-wing leads

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum distance to pad edge at toe	B	0,20 mm
Minimum distance to pad edge at heel	L	0,5 × W
Minimum side joint length	D	full lap connection soldered
Minimum heel fillet height	E	X + T
Minimum heel fillet height for SOP with outward bottom leads	E	X+ 0,5T provided good wetting visible
Solder Stand off	X	Present

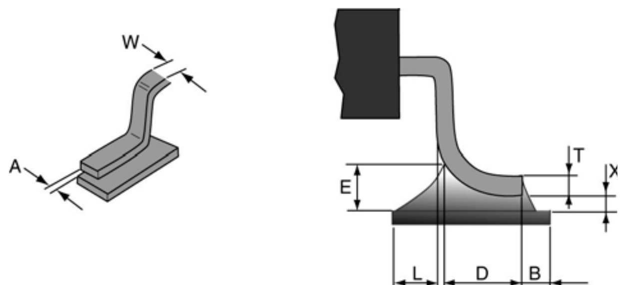


Figure 11-5: Mounting of devices with round, flattened, ribbon, "L" and gull-wing leads

11.5.7 Devices with "J" leads

a. Solder joints formed to "J" and "V" shaped leads shall meet the dimensional and solder fillet requirements of Table 11-6 and Figure 11-6.

Table 11-6: Dimensional and solder fillet requirements for devices with "J" leads

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum side joint length	L	1,5 × W
Minimum heel fillet height	M	X + T
Maximum stand-off	X	Present

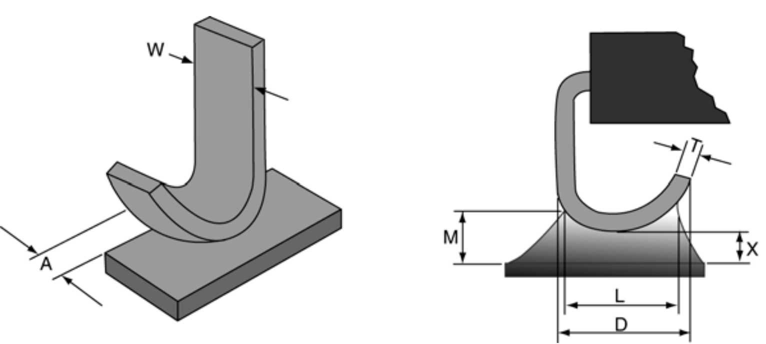


Figure 11-6: Mounting of devices with "J" leads

11.5.8 Area array devices

a. The outer row of solder joints to area array devices shall be visually inspected by looking from the side in accordance with the requirements in 11.5.1 and Table 11-7 and with the rejection criteria specified in clauses 13.3 and 13.4.

b. Solder joints shall be inspected using X-ray techniques in accordance with clause 6.8.7 and Table 11-7.

c. X-ray techniques shall be used to verify the acceptable wetting the absence of bridge, solder balls and minimum electrical clearance.

NOTE 1 <<deleted>>.

NOTE 2 As it is impossible to visually inspect solder joints to area array devices, reliability of these devices cannot be assured by inspection and rework. Even using X-ray techniques, some types of defect are difficult to detect. Therefore, reliability of these solder joints can only be assured by robust process control.

NOTE 3 Examples of typical area array devices are shown in Figure 11-7, Figure 11-8 and Figure 11-9.

Table 11-7: Dimensional and solder fillet requirements for area array devices

Parameter	Dimension limits
Misalignment	No pad overhang
BGA ball	Collapse of BGA ball spacing does not violate minimum electrical clearance or become less than 0,10 mm.
Maximum device height	Overall height of device does not exceed maximum specified.
Soldered connection	a. BGA balls contact and wet to the land forming a continuous connection b. CGA solder columns contact and wet to the land forming a continuous connection
Solder balls	No solder balls
Maximum CGA column tilt	10 degrees
D = Ball or column diameter	

Figure 11-7: <<deleted>>

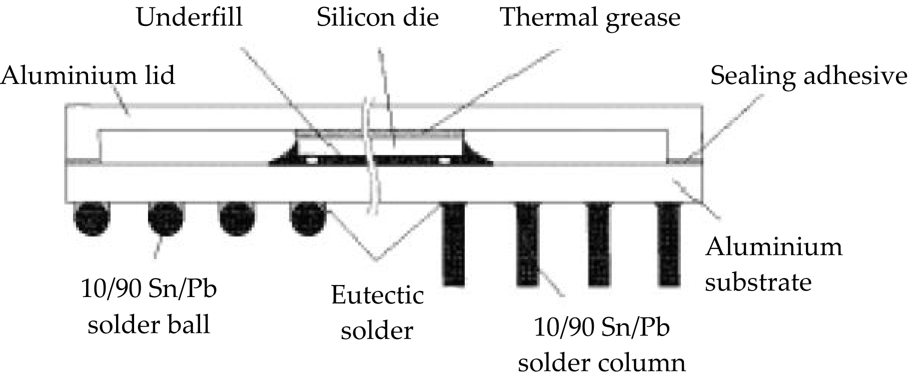


Figure 11-8: Typical ceramic area array showing ball grid array configuration on left and column grid array on right (CBGA & CCGA)

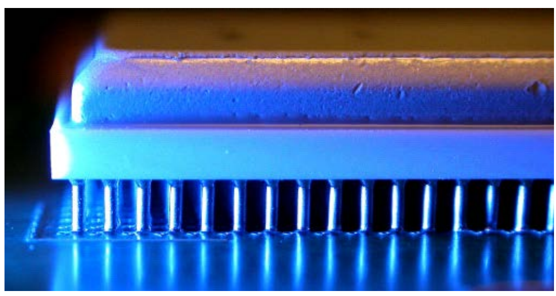


Figure 11-9: Typical assembled CCGA device

11.6 <<deleted>>

a. <<deleted>> .

b. <<deleted>> .

NOTE <<deleted>>

Figure 11-10: <<deleted>>

11.7 <<deleted>>

a. <<deleted>> .

11.8 <<deleted>>

a. <<deleted>> .

NOTE 1 <<deleted>>

NOTE 2 <<deleted>>

11.9 Devices with ribbon terminals without stress relief

a. Solder joints formed shall meet the dimensional and solder fillet requirements of Table 11-8.

NOTE Illustration is given in Figure 11-11.

b. The degolding and pretinning zone shall be outside the PCB pad

NOTE This is to ensure that the degolding and pretinning has been performed such that the solder fillet is not in contact with the gold or AuSn intermetallic.

Table 11-8: Dimensional and solder fillet requirements for devices without stress relief

Parameter	Dimension	Dimensions Limits
Max side overhang	A	≤ 0,1 x W
Minimum distance to pad edge at toe	B	≥ 0,20 mm
Stand off	X	Present
Minimum side joint fillet	D	3xW with full lap soldered connection
Max Tilt	C	10°

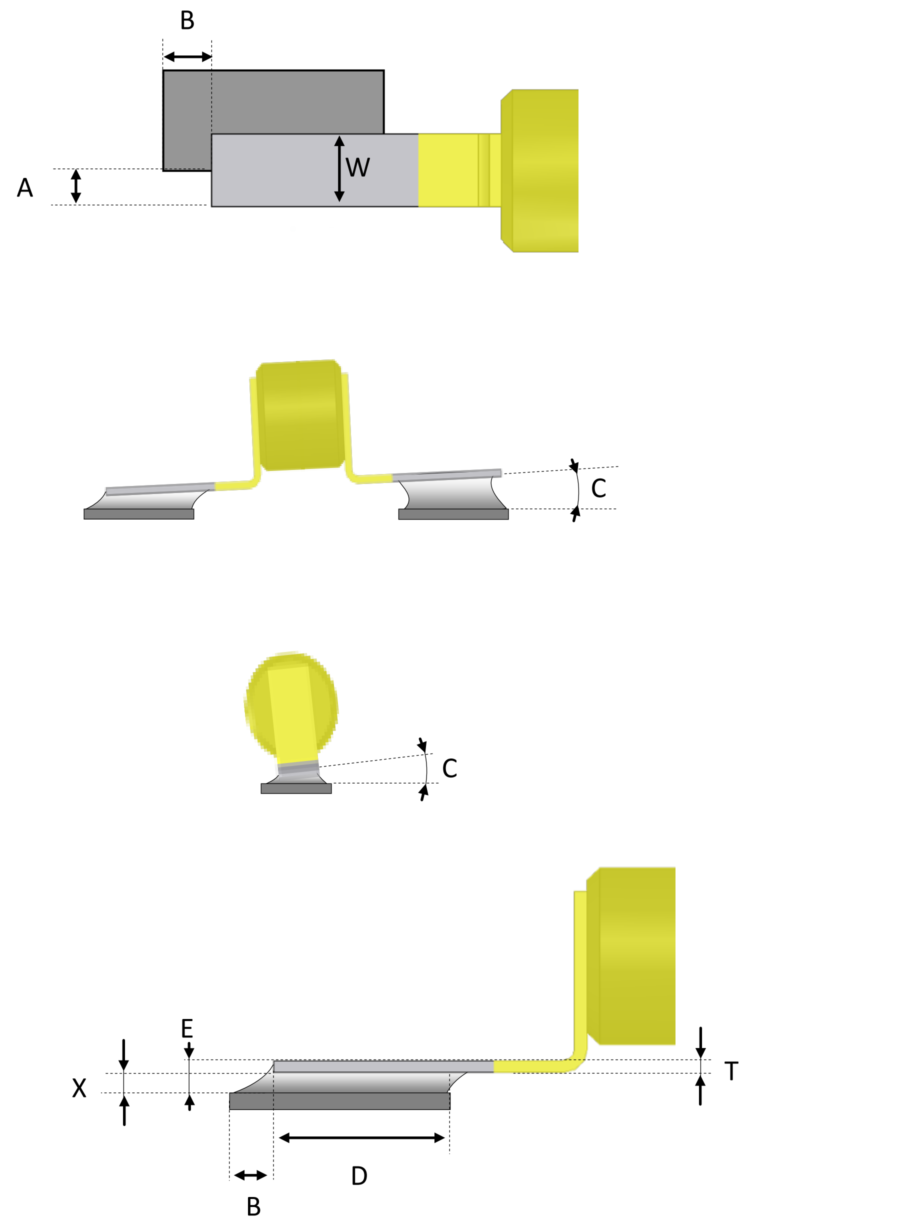


Figure 11-11: Mounting of devices without stress relief

11.10 L-Shape inwards devices

a. Devices having L-shape inwards terminals shall meet the dimensional and solder fillet requirements of Table 11-9.

NOTE Illustration is given in Figure 11-11.

b. Solder fillet shall be visible on the side of the terminal on the connection.

c. The device shall be centred on its pads such as the minimum lap contact length is fulfilled.

Table 11-9: Dimensional and solder fillet requirements for "L-shape inwards" devices

Parameter	Dimension	Dimension limits
Minimum fillet height, heel	F	(0,25 x H)+G or G +1mm whichever is less
Minimum distance to pad edge	K	0,2 mm
Minimum Lap contact length	D	75% terminal of device, limited to one side
Stand-off (elevation)	G	Present
Side of terminal wetting		Evidence of solder wetting

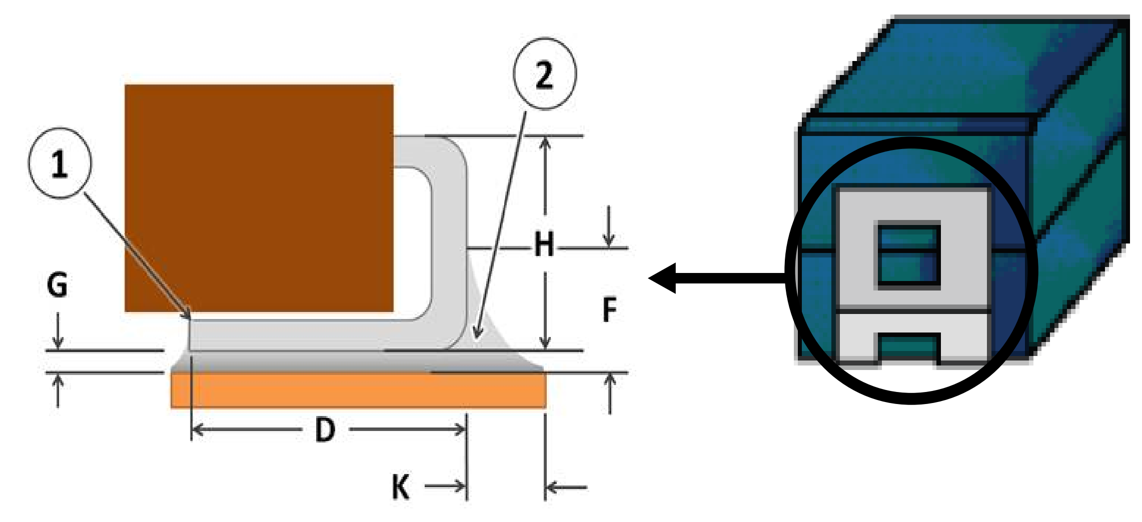


Figure 11-12: Mounting of devices with "L-shape inwards" leads (1 = Toe, 2 = Heel)

12 Cleaning of PCB assemblies

12.1 General

a. ECSS-Q-ST-70-08, clause “Cleaning of PCB assemblies – General” shall apply.

12.2 Ultrasonic cleaning

a. ECSS-Q-ST-70-08 shall apply for "Ultrasonic cleaning".

12.3 Monitoring for cleanliness

ECSS-Q-ST-70-08 shall apply for "Monitoring for cleanliness".

12.4 Verification of cleanliness

a. The verification of the cleanliness SIR test shall be performed for the following cases:

1 for the first verification programme performed by a company,

2 when the conditions of Table 14-1 request it.

b. The SIR test shall be conducted in accordance with requirements from the method 2.6.3.3 of IPC-TM-650 (2004).

13 Final inspection

13.1 General

a. <<deleted>>.

b. <<deleted>>.

c. <<deleted>>.

d. Devices and conductors shall not be physically moved to aid inspection.

e. The substrate, devices and device position, as well as the fasteners and the mounting hardware, shall be inspected in accordance with the requirements in clause 11.5.

NOTE Clause 16 includes examples of acceptable and unacceptable workmanship.

f. The assembly shall be visually inspected in two steps with the following methodology:

1 Visual inspection of the assembly is aided by magnification appropriate to the size of the connections between 4x and 10x.

2 Detailed inspection is performed with a minimum magnification 20x.

g. Additional magnification shall be used to resolve suspected anomalies or defects up to 40x.

h. X-ray inspection shall be applied when there are hidden solder joints that are not visually accessible.

13.2 Acceptance criteria

a. Acceptable solder connections shall be characterised by:

1 clean, smooth, satin to bright undisturbed surface,

2 solder fillets between conductor and termination areas as described and illustrated in clause 16,

3 visible contour of wires and leads such that their presence, direction of bend and termination end can be determined,

4 complete wetting as evidenced by a low contact angle between the solder and the joined surfaces,

5 acceptable amount and distribution of solder in accordance with clause 11.5,

6 absence of any of the defects mentioned in clauses 13.3 and 13.4.

13.3 Visual rejection criteria

a. The following are some characteristics of unsatisfactory conditions, any of which shall be cause for rejection:

1 charred, burned or melted insulation of devices,

2 conductor pattern separation from circuit board,

3 burns on base materials,

4 <<deleted>>

5 excessive solder (including peaks, icicles and bridging), see clause 16,

6 flux residue, solder splatter, solder balls, or other foreign matter on circuitry, beneath devices or on adjacent areas,

7 dewetting,

8 insufficient solder, see clause 16,

9 pits, holes or voids where bottom of the solder is not visible,

10 granular or disturbed solder joints,

11 fractured or cracked solder connection,

12 cut, nicked, gouged or scraped conductors or conductor pattern,

13 incorrect conductor length,

14 incorrect direction of clinch or lap termination on a PCB

15 damaged conductor pattern,

16 bare copper or base metal, excluding the ends of cut wire or leads or sides of tracks and soldering pads on substrate,

17 soldered joints made directly to gold-plated terminals or gold-plated conductors using tin-lead solders,

18 cold solder joints,

19 device body embedded within solder fillet,

20 open solder joints (e.g. tombstoning),

21 probe marks present on the metallization of chip devices caused by electrical testing after assembly,

22 glass seal does not conform to MIL-STD-883 Method 2009,

23 measling; which violates the minimum insulation distance,

24 delamination, except within region of the breakout regions for multi-panel processed,

25 exposed base metal excluding area of cut leads in the soldered connection,

26 cracks detected in glass diodes outside the relevant devices procurement standard,

27 bent connector pins outside the relevant devices procurement specification,

28 damage of the lead, device or PCB beyond that defined in the procurement standard of the item,

NOTE Damage such as end cap metallisation peeling , crack in device.

29 degraded insulation material of the connector in contact area,

30 bubble or void in conformal coating and or potting between high voltage conductors,

NOTE High voltage in this context is 100 V or higher.

31 bubble or void in the conformal coating and or potting bridging conductive elements,

32 lack of intended conformal coating,

33 unintended and continuous adhesive forming a bridge in contact with terminals, component body or solder joints,

34 excessive degolding,

35 insufficient degolding,

36 bonding on glass device body with epoxy,

37 separation of adhesive from the bonded surface,

38 separation of conformal coating from the surface,

39 any defect.

13.4 X-ray rejection criteria

a. The following are some characteristics of not acceptable conditions from X-ray inspection, utilizing equipment defined in clause 6.8.7, any of which shall be cause for rejection:

1 criteria and dimensions outside the limits given in Table 11-7 for area array devices,

2 bridges and other unintended metallic materials,

3 non-wetting of the solder,

4 void cumulative greater than 25 % by area of the solder joint.

NOTE Solder balls are a typical example of unintended metallic material.

b. X-ray inspection shall be applied when there are hidden solder joints that are not visually accessible.

13.5 Warp and twist of populated boards

a. <<deleted>>.

NOTE <<deleted<<

b. The PCB assembly shall be supported during handling and transportation in order to avoid any mechanical stress on the assembly or component damage.

NOTE Mechanical support can be provided by spacer and frame.

c. The PCB shall not be forced during integration to compensate any warp and twist.

NOTE Shims or spacers can be used to accommodate warp and twist during integration.

13.6 Inspection records

a. The result of the final inspection shall be recorded on the shop traveller.

14 Verification procedure

14.1 General

a. The supplier shall establish a verification programme in accordance with the DRD from Annex G and Annex H to be approved by the Approval authority.

b. The supplier shall demonstrate verification for each combination of substrate material, SMD type, soldering technique applied, staking compound, solder mask and conformal coating as used on flight models.

c. <<deleted>>.

d. <<deleted>>

e. The range of surface mounted devices and associated materials shall be documented in the verification programme, in accordance with the requirements in 0

1 deleted.

2 deleted.

3 deleted.

f. The verification shall be performed on at least three leaded devices, five leadless devices, five sensitive devices of each type and size which are assembled per assembly configuration in conformance with the PID specified in clause 5.

g. The supplier's repair process including removing and replacing of one of each type of mounted device shall be submitted to verification testing.

h. <<deleted>>

i. <<deleted>>

j. <<deleted>>

k. Verification testing of commercial devices shall be performed for each lot in conformance with this clause.

l. A repair, not included in ECSS-Q-ST-70-28, shall be submitted to a verification test programme

m. Verification of the assembly by standard manual method shall also be undertaken when assembly by machine is performed.

NOTE Standard manual method can cover a range of processes in addition to hand soldering e.g. hot gas station, IR station.

n. The repair shall be demonstrated on the standard manual method.

o. The PCB verification test vehicle shall be representative of the FM pad configuration of the hardware.

p. Terminations to be microsectioned shall be connected to the internal PCB layers

q. The verification of area array devices shall meet the requirements of clause 14.9.

r. For each sensitive device the verification shall be performed on at least five devices per assembly configuration in accordance with the PID specified in DRD in Annex F.

s. For each type of device the repair shall be performed on the largest device.

t. The repair shall be performed only on the devices being assembled by standard manual method.

NOTE No repair verification is needed on the devices being assembled by machine method as this is covered under the standard manual soldering verification method.

u. The supplier shall maintain a list of sensitive devices.

v. Sensitive devices shall be submitted to verification every four years.

w. SMT line audit shall be conducted every four years by the approval authority

x. The verification sample shall be submitted to two standard machine method reflows when the assembly of the flight hardware is made on both sides.

NOTE The supplier has the option to flip the board for the second reflow to demonstrate the flight configuration.

y. Any pure tin device which has been pretinned shall have the pretinning process verified with respect to coverage and integrity

z. The device type classification shall be in accordance with Table 14-1

Table 14-1: Device type classification

Device type	Classification
End-capped and end-metallized devices	Leadless
Bottom terminated chip devices	Leadless
Cylindrical end-capped devices	Leadless
Castellated chip carrier devices	Leadless
Devices with round, flattened, ribbon, “L” and gull-wing leads	Leaded
Devices with “J” leads	Leaded
Area array devices	Leadless
Devices with ribbon terminals without stress relief	Leaded
L-Shape inwards devices	Leaded

14.2 Verification by similarity

a. <<deleted>>

NOTE <<deleted>>.

b. <<deleted>>

c. <<deleted>>

d. <<deleted>>

e. <<deleted>>

f. <<deleted>>.

g. <<deleted>>

h. <<deleted>>

i. <<deleted>>

j. <<deleted>>

k. <<deleted>>

14.2.1 General

a. A package shall be identified as the same family in case the following conditions are met:

1 the lead pitch, nominal thickness, nominal width and materials composition are identical,

2 the coated lead finishes on the termination are identical,

3 the bending dimensions and shape are identical,

4 the packages are constructed from the same materials.

NOTE 1 Glass to metal sealed, glass sealed side-brazed, top-brazed, and bottom-brazed packages are different families.

NOTE 2 Dual side pin arrangements are different to quad side pin families.

14.2.2 Conditions for similarity.

a. Verification by similarity shall not apply to commercial devices.

b. Verification by similarity shall not apply to castellated devices.

c. Verification by similarity for chip devices shall be valid in case the following conditions are met:

1 devices size is between the verified Lmin and Lmax as well as within the verified Wmin and Wmax,

2 thinner than the maximum height verified,

3 the ceramic material type identical,

4 the metallization of the termination and the barrier layers on devices is identical,

5 the device manufacturer is identical.

NOTE 1 For the requirement 14.2.2c.1: the dimension of device is length, L width, W.

NOTE 2 For the requirement 14.2.2c.1: for example 0402 – 2220 does not qualify 1825 as the width is outside the max 20 verified.

NOTE 3 For the requirement 14.2.2c.2: ceramic chip capacitors can be very sensitive to mounting conditions. Generally type 1 chip capacitors show less sensitivity to mounting constraints than Barium Titanate based type 2 chip capacitors. This sensitivity is design and process related and can therefore vary from one manufacturer to another. Within a manufacture type 2 range, one or more ceramic material can be used but one can say that generally the highest end of the capacitance ranges are the most sensitive to mounting conditions. In order to increase capacitance value for a given chip format with a specified maximum chip thickness, manufacturers increase the number of dielectric layers, thus increasing the volume ratio between electrode material and ceramic, which is not favorable in terms of sensitivity to mounting constraints.

NOTE 4 For the requirements 14.2.2c.2: it is therefore impossible to apply similarity rules between type 1 and type 2 ceramic chip capacitors as well as between different manufacturers. It is

also recommended to select in priority the highest capacitance values in a class or type 1 or type 2 ceramic capacitors range to be submitted to assembly verification.

NOTE 5 For the requirements 14.2.2c.3: type refers only to type 1 or type 2 capacitor.

d. Verification by similarity for leaded devices, shall be valid in case the following conditions are met:

1 the devices are from the same family in conformance with the requirements from the clause 14.2.1,

2 devices are smaller than the verified Lmax and Wmax.

NOTE The dimension L is the distance between the outermost leads of the device and W is the device width.

e. Verification by similarity for leadless device with thermal plane termination shall be valid in case the following conditions are met:

1 smaller than the verified Lmax and Wmax,

2 the construction of the device is identical to that verified,

3 the materials are identical.

NOTE The dimension of device is length, L width W.

f. Verification by similarity for area array devices shall be valid in case the following conditions are met:

1 lower number of columns,

2 the same pitch,

3 same column dimensions,

4 same column materials,

5 same column construction,

6 same column manufacturer,

7 same column assembly process,

8 lower mass

9 same material and same package construction

10 same shape

14.3 Verification test programme

a. The verification test programme as shown in Figure 14-2 shall consist of:

1 Visual inspection in conformance with clause 13.

2 Vibration and shock testing in conformance with clause 14.5.

NOTE Mechanical testing according to this standard gives an indication of the reliability of the product in actual applications. It is unlikely that the test vehicle represents every flight configuration (size of the board, damping of the board, stiffening of board, number of board layers). The deflections, amplitudes, transmissibility's, radii of curvature experienced by SMDs under shock and vibration are totally dependent on the board to which they are mounted. Because each space project has its own unique shock and vibration requirements it is impossible to determine appropriate test levels without testing actual electronic boxes.

3 Temperature cycling in conformance with clause 14.6 except for area array devices.

NOTE Temperature cycling is performed to ensure that the SMDs, substrates, solder alloys and associated staking compounds and conformal coatings are suitable for the operational lifetime of the spacecraft.

4 Microsectioning in conformance with clauses 14.7

5 For area array devices, temperature cycling in conformance with requirements from clause 14.9.

b. The supplier shall present a verification programme for approval.

NOTE Owing to the different modes of failure resulting from vibration and temperature cycling, the supplier can use any sequence of environmental testing.

c. For each assembly method and mounting configuration at least three devices shall be assembled, except the case specified in the requirement **Error! Reference source not found.**.

NOTE Machine reflow, hand soldering are examples of an assembly method.

d. For sensitive and leadless devices five devices shall be assembled.

e. Removal and replacement shall be verified on the standard manual assembly method.

f. The supplier shall demonstrate a minimum number of 50 cycles after vibration with no visual evidence of cracks in mechanical bonding, in accordance with requirement 14.10m.

NOTE The first inspection point is defined by the supplier for acceptance of cracks in mechanical joints.

Figure 14-1: <<deleted>>

Non sensitive devices: 3 devices with one to be submitted to repair. Total number of needed devices is therefore 4
Sensitive and leadless devices: 5 devices with one to be submitted to repair. Total number of needed devices is therefore 6.

- Assembly of verification sample with Standard manual assembly method 14.3C
- Visual inspection 13
- Bonding / conformal coating (if used)
- Visual inspection 13
- Removal of parts Selected for repair 14.3e
- Visual inspection of PCB 13
- Assembly of New part
- Visual inspection 13
- Bonding / conformal coating (if used)
- Visual inspection 13
- Vibration 14.6
- Visual inspection 13
- Shock (if Applicable)
- Visual inspection 13
- Thermal cycling $50 < N1 < 250$ 14.3f
- Visual inspection 13
- Thermal cycling $N2 = 500 – N1$
- Visual inspection 13
- Micro-sectioning 14.7

Non sensitive devices: 3 devices. Total number of needed devices is 3.
Sensitive and leadless devices: 5 devices. Total number of needed devices is 5

- Assembly of verification sample with relevant machine assembly method 14.3c
- Visual inspection 13
- Bonding / conformal coating (if used)
- Visual inspection 13
- Vibration 14.5
- Visual inspection 13
- Shock(if Applicable) 14.5
- Visual inspection 13
- Thermal cycling $50 < N1 < 250$
- Visual inspection 13
- Thermal cycling $N2 = 500 – N1$ 14.3f
- Visual inspection 13
- Micro-sectioning 14.7

Figure 14-2: Verification programme flow chart (standard flow)

14.4 Electrical testing of devices

a. <<deleted>>

14.4.1 General

a. The supplier may propose electrical monitoring in conformance with the test programme as shown in the Figure 14-3 except the cases specified in 14.4.1b and 14.4.1c.

b. Electrical monitoring shall be performed for ceramic hermetic area array devices in conformance with requirements in clause 14.9.

c. Capacitors and "SMD – xx" devices shall be excluded from electrical monitoring.

NOTE Capacitor and "SMD – xx" devices such SMD 0.5, 1, 2 and 5C are excluded as the failure mechanism is crack in ceramic.

d. For other device types, the supplier may propose electrical monitoring as an alternative method, for each assembly configuration, including the repair assembly method, to achieve verification providing the following conditions are met

1 one device for initial microsectioning except the case for sensitive and leadless devices,

2 for sensitive devices a minimum of five devices to be assembled and microsectioned in compliance with requirements 14.7.2d and 14.7.2e,

3 minimum number of 32 devices for electrical monitoring,

4 all solder terminations are continuously electrically monitored throughout the temperature cycling,

5 minimum of 1500 thermal cycles in accordance with requirements from the clause 14.6,

6 the number of completed cycles for each failed device is recorded.

e. First failure in case number of cycles < 1500 shall be identified as the device assembly capability.

f. As a minimum microsection of one failed device shall be performed in order to determine the root cause of failure.

g. The electrical value of devices shall be selected to ensure detection of electrical anomaly.

1 for resistors zero ohm or the lowest value in the procurement specification,

2 for other types custom daisy chain.

h. A drift of less than 10 % of resistance shall be accepted when the continuity tests are performed and referenced to the first five 5 cycle recorded values except the case specified in 14.4.1i.

i. Depending on application the acceptable drift of resistance may be adapted.

j. For each assembly method and type of devices at least 32 devices shall be assembled for electrical monitoring.

NOTE Machine reflow, hand soldering are the examples of assembly method.

k. The assembly of the capability and the electrical verification samples may be made on the same board.

l. Separation of capability samples and electrical monitoring may be made later, but before the microsectioning of the capability samples and before the environmental tests for the electrical verification samples.

NOTE Illustration is given in the flow diagram of Figure 14-3: Verification programme flow chart (Electrical Testing)

m. Capability samples may be excluded from the programme if it can be demonstrated through previous verification heritage.

n. Repair, removal and replacement shall be verified only for the standard manual assembly method.

o. Microsectioning shall be performed in accordance with requirements from clause 14.7.

p. Vibration and shock testing shall be performed in conformance with requirements from clause 14.5.

Sensitive Devices 37 + 1 repair total number of parts needed 38
Non sensitive 33 Devices
+ 1 repair therefore total number of devices 34

Assembly of capability and verification sample with relevant assembly method[14.4.1k]

Visual inspection [13]

Conformal coating/Bonding
(if used)

Visual inspection [13]

Separate capability samples from electrical verification samples[14.4.1n]

Sensitive and leadless 5 Parts (5 initial fit +1 repair ,total needed 6)
Non Sensitive 1 part (1 initial fit 1 for repair , total needed 2)

Capability verification sample

Removal of Selected part to Undergo repair
(1 part Sensitive , 1 part non Sensitive)

Visual inspection of PCB [13]

Assembly of Repair part with repair assembly method

Visual inspection [13]

Micro-sectioning[14.7]

32 Parts

Electrical verification sample

Vibration[14.5]

Visual inspection

Shock (If applicable) [14.5]

Visual inspection [13]

Thermal cycling with electrical monitoring
N = 1 to 500

Visual Inspection [13]

Thermal cycling with electrical monitoring
N = 501 to 1500

Visual Inspection [13]

Figure 14-3: Verification programme flow chart (Electrical Testing)

14.5 Vibration and Shock

a. ECSS-Q-ST-70-08 shall apply for "Vibration".

b. For area array devices the shock levels shall be set to meet the intended mission with margin, except the case specified in the requirement 14.5c.

c. For area array devices shock may be omitted when the mechanical design can demonstrate robust margin.

NOTE The use of dedicated mechanical stiffener is an example of such design.

d. For shock sensitive devices identified in ECSS-E-HB-32-25, shock testing shall be added to the verification programme flow.

e. When shock testing is required as defined in 14.5d then the shock levels shall be set to meet the intended mission with margin.

14.6 Temperature cycling test

a. ECSS-Q-ST-70-08, clause “Temperature cycling test” shall apply for the thermal profile.

b. The total number of temperature cycles shall be 500, except for area array devices and devices verified by electrical monitoring when clause 14.9 and,14.4 is applicable.

c. The monitoring temperature sensor shall be attached to the surface of the printed circuit board.

d. <<deleted>>

e. For devices under the electrical testing verification the total number of temperature cycles shall be 1500 in conformance with requirements from the clause 14.4.1

14.7 Microsection

a. <<deleted, moved to 14.7.2a. and modified>>.

NOTE <<deleted>>.

b. << deleted, moved to NOTE. and modified>>.

NOTE <<deleted>>.

c. <<deleted>>.

NOTE <<deleted>>.

d. << deleted, moved to 14.7.2i. and modified>>.

e. << deleted, moved to 14.7.2j. and modified>>.

NOTE <<deleted>>.

14.7.1 Microsection facilities

a. Approval authority should make available the list of laboratories to perform microsection.

b. Microsections shall be performed by a laboratory specified in the requirement 14.7.1a except the case specified in the requirement 14.7.1c.

c. When in-house or other non-listed microsection facilities are used, the company shall demonstrate the following:

1 the laboratory capability on a representative sample without conformal will be provided,

2 a report with associated microsections shall be sent to the approval authority for review and assessment of quality of microsectioning.

NOTE Representative sample include chips, LCCs, FP

14.7.2 Microsectioning

a. At least one microsection shall be made per assembly configuration after environmental testing on each type of device, size and process (machine assembly and standard manual assembly soldering) except the case specified in 14.7.2d.

NOTE Successive polishing planes can be performed.

b. In case the microsection shows a crack >25% a second device shall be microsectioned.

c. In case the second microsection shows a crack >25% a third device shall be microsectioned.

d. For sensitive devices three devices shall be microsectioned per assembly configuration.

e. For sensitive devices specified in the requirement 14.7.2d additional microsection may be requested in case of cracks or other features detected during the first microsection sample.

NOTE Examples of microsections are shown in clause 16.4.

f. The microsection shall be done on the device having the worst solder joint appearance as identified at MIP2.

g. Adhesive for thermal or mechanical purpose underneath a device shall be microsectioned.

h. The full integrity of the assembly shall be assessed by microsectioning.

i. The Approval authority shall have access to the microsection mould and picture.

j. The microsections and other devices shall be stored for a period of at least 10 years.

NOTE Stored samples can assist the analysis of in-service failures.

k. Additional microsections may be requested in case of cracks or other features detected during the first microsection sample or by request from the approval authority.

l. The microsection shall be inspected with a magnification of 50 to 200 times except the case specified in the requirement 14.7.2m.

m. The microsection for devices with small stand-off should be inspected with magnification up to 500 times.

NOTE Small stand-off devices are LCCs, chip resistors.

14.8 <<deleted>>

a. <<deleted>>.

NOTE <<deleted>>.

b. <<deleted>>.

NOTE <<deleted>>.

14.9 Special verification testing for hermetic ceramic area array packages

14.9.1 <<deleted>>

<<deleted>>

NOTE <<deleted>>

14.9.2 <<deleted>>

a. <<deleted>>.

b. <<deleted>>.

c. <<deleted>>.

d. <<deleted>>.

e. <<deleted>>.

14.9.3 General

a. The assembly verification of hermetic ceramic AADs shall be divided in the following two parts, as shown in Figure 14-4.

1 demonstration of capability, and

2 verification.

NOTE 1 The purpose of the capability samples is to show that the PCB integrity and the device are intact after the assembly and repair of AAD and environmental testing (vibration, mechanical shock and 500 temperature cycles). A crack in the columns or balls is not considered as reason for rejection.

NOTE 2 Once the capability samples show a satisfactory result the verification of AAD can commence.

NOTE 3 Capability samples may be excluded from the programme if the supplier can demonstrate through previous verification heritage

b. The verification shall be performed with daisy chain devices to demonstrate a reliable electrical function of the PCB and the package interface throughout the environmental test campaign

NOTE Environmental test campaign to include vibration, mechanical shock and 1500 temperature cycles.

2 Parts required, 2 parts initial l fit 1 part repair total parts needed 3

Assembly of capability sample with relevant assembly method
Visual inspection
X Ray
Bonding / Conformal coating (if used)
Visual inspection
Removal of part Selected to be repaired 14.9.4d
Visual inspection of PCB
Assembly of New device with repair assembly method
Visual inspection
X Ray
Bonding / Conformal coating (if used)
Visual inspection
Vibration 14.5
Visual inspection
Shock 14.5
Visual inspection
Thermal cycling 14.6 N = 500
Visual inspection
Micro-sectioning 14.7
Capability Review
Fail
Pass

4 Parts required, 4 parts initial fit 1 part repair, total parts needed 5

Assembly of verification sample with relevant assembly method
Visual inspection
X-Ray inspection
Bonding / Conformal coating (if used)
Visual inspection
Removal of Selected part to be repaired 14.9.5c
Visual inspection of PCB
Assembly of New device with repair assembly method
Visual inspection
X-Ray inspection
Bonding / Conformal coating (if used)
Visual inspection and daisy chain resistance measurement
Vibration 14.5
Visual inspection and daisy chain resistance measurement
Shock 14.5
Visual inspection and daisy chain resistance measurement
Thermal cycling with electrical monitoring, 14.6 N = 1500
Visual inspection and daisy chain resistance measurement

The verification program of AAD devices consists of two flows, one for the capability sample and one for the electrical verification sample.A review should be undertaken before starting the electrical verification flow

Figure 14-4 Verification programme flow chart (AAD)

14.9.4 Evaluation of capability samples

a. The supplier shall manufacture and demonstrate that the two capability samples are in conformance with the requirement 14.9.4j before the manufacture of the verification samples using daisy chain devices can be initiated.

b. The PCB material, PCB build-up and devices used as capability samples shall be representative for the FM of the hardware.

c. Two devices shall be assembled in the relevant reflow process.

d. The supplier may use daisy chain packages for the capability assessment with or without electrical monitoring.

e. One of the assembled devices shall be removed and replaced with a new device using the repair process.

f. The devices shall be inspected in conformance with requirements from the clause 11.5.8.

g. The two devices shall be submitted to vibration testing in conformance with requirements from the clause 13.2 of ECSS-Q-ST-70-08C.

h. The two devices shall be submitted to three mechanical shock pulses in conformance with requirements 14.5b and 14.5c.

i. The two devices shall be submitted to 500 thermal cycles in conformance with requirements from the clause 13.3 of ECSS-Q-ST-70-08.

j. After environmental tests completion, microsectioning of the both devices shall be performed to demonstrate PCB integrity in the AAD area with respect to:

   1 ECSS-Q-ST-70-10

   2 Damage to the device outside the procurement specification

   3 Pad lifts

   4 Cracks in laminate

   5 Cracks in via

   6 Cracks in track

   7 Delamination's in the PCB

   8 Measling in the PCB

   9 Cracks in bonding if used

14.9.5 Verification

a. The PCB material, PCB build-up and daisy chain devices used for the verification shall be representative for the FM of the hardware.

b. For each assembly method and mounting configuration four devices shall be assembled.

c. One of the assembled devices shall be removed and replaced with a new device using the repair process.

d. The devices shall be inspected in conformance with requirements from the clause 11.5.8.

e. The four devices shall be submitted to vibration testing in conformance with requirements from the clause 13.2 of ECSS-Q-ST-70-08.

f. The four devices shall be submitted to three mechanical shock pulses in each direction in conformance with requirements 14.5b and 14.5c

g. The four devices shall be submitted to 1500 thermal cycles with temperature conditions in conformance with requirements from the clause 13.2 of ECSS-Q-ST-70-08.

h. Resistance measurement should be done, at ambient, before and after any mechanical testing.

i. Electrical monitoring of the daisy chain shall be performed during the 1500 thermal cycling.

j. The electrical monitoring shall be continuous throughout all 1500 cycles

k. The sampling time of the electrical measurement shall be maximum 10 s throughout the 1500 cycles.

l. The maximum increase of each individual daisy chain resistance, across the entire temperature cycling range during 1500 thermal cycles, shall not be more than 10 % of initial resistance recorded during the first five cycles.

m. No interrupts in the electrical monitoring shall be detected throughout the thermal cycling.

n. The supplier may provide their own criteria for an electrical failure to approval authority for approval.

14.10 Verification acceptance and rejection criteria

a. Any electrical failures during or after testing shall invalidate the SMD verification.

b. In the case of visual failures, an analysis shall be performed to identify the cause: component or soldering process.

c. In the case of cracked joints, microsections shall be made to evaluate their depth and origin.

d. Surface and internal cracks that penetrate less than 33 % of the solder fillet critical zone (as defined in Figure 14-5), ball or column, shall be considered acceptable.

e. Cracks present outside the critical zone shall be considered acceptable.

f. <<deleted>>.

g. <<deleted>>.

NOTE 1 <<deleted>>.

NOTE 2 <<deleted>>.

h. The devices shall be in conformance with the assembly requirements of clause 11.5.

i. The devices shall be in conformance with the requirements of clause 13.2.

j. Any visual defects in conformance with requirements from clause 13.3 shall be defined as a failure.

k. Any damage to the device shall be identified as a verification failure.

l. Thermal and mechanical bonding shall not be cracked at the completion of the verification testing.

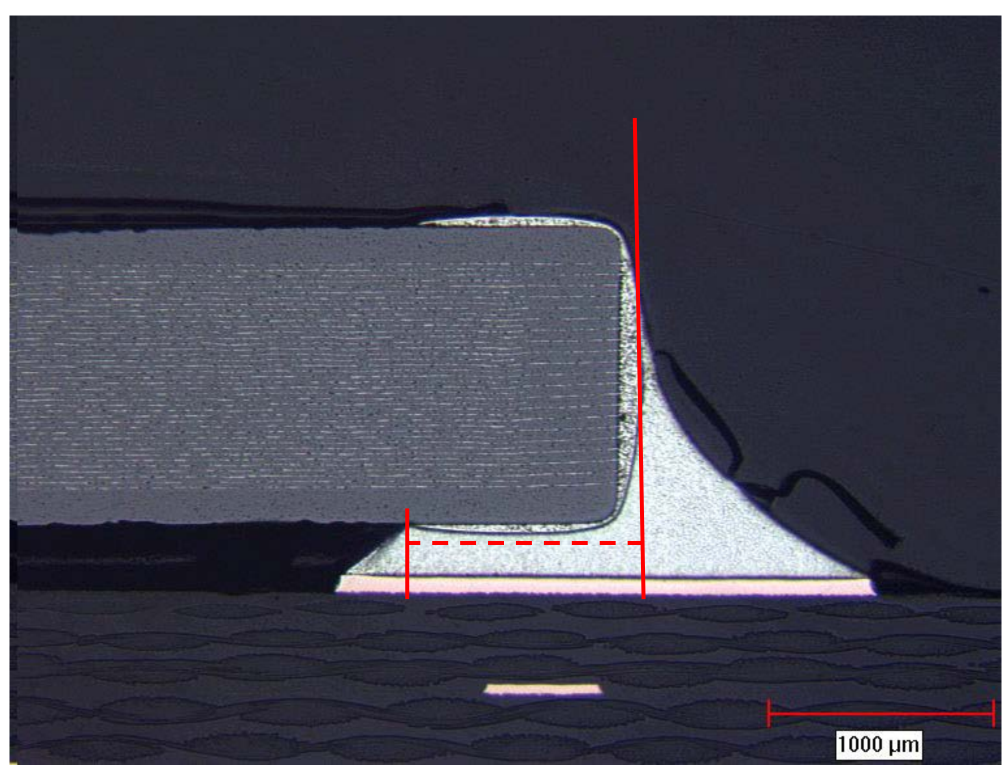
m. Cracks in the bonding used for mechanical purpose may be accepted in case the following conditions are met:

1 absence of cracks after vibration and completion of a minimum of 50 thermal cycles,

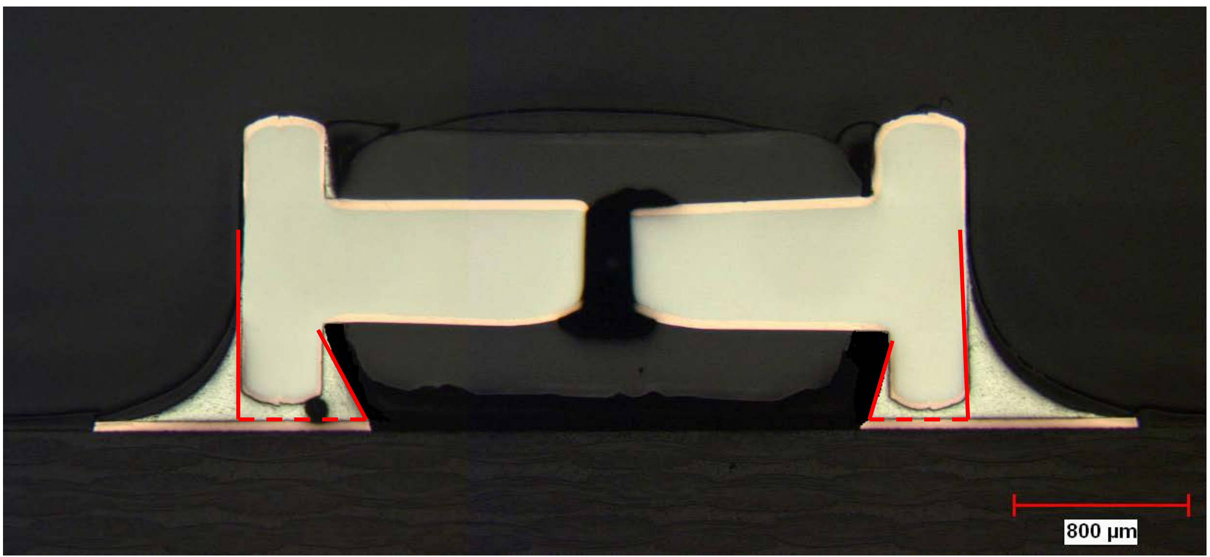
2 photos are provided in the verification report to demonstrate absence of cracks at 50 thermal cycles.

n. Cracks in the thermal bonding perpendicular to PCB may be accepted.

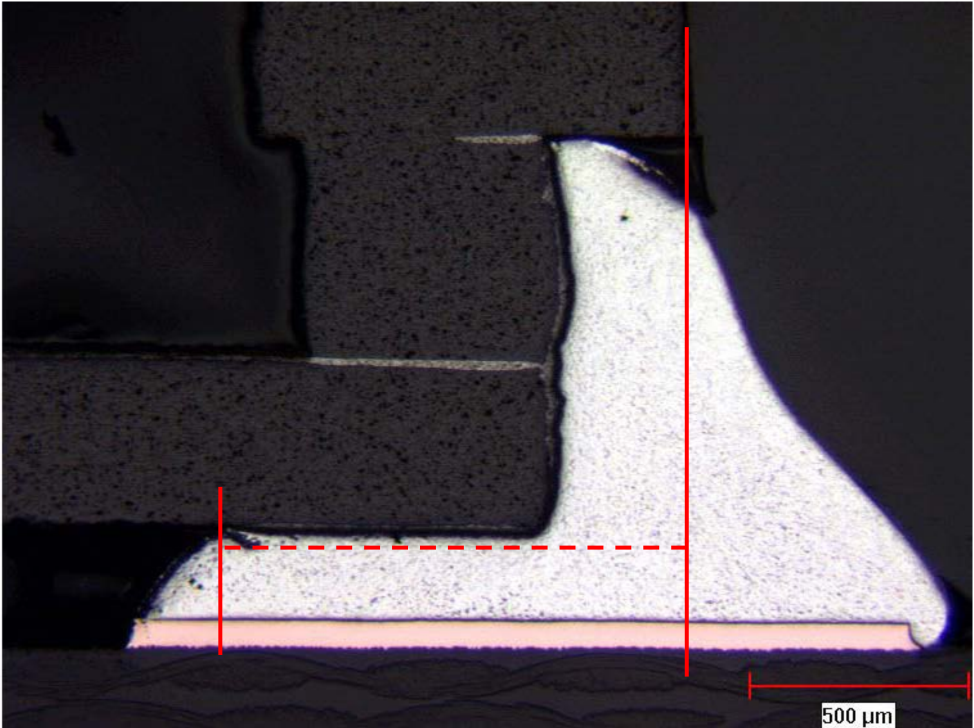
o. Defects, such as pad lifting, cracks in laminate, cracks in via, cracks of tracks, PCB delamination shall be identified as a verification failure as defined in 14.9.4j.



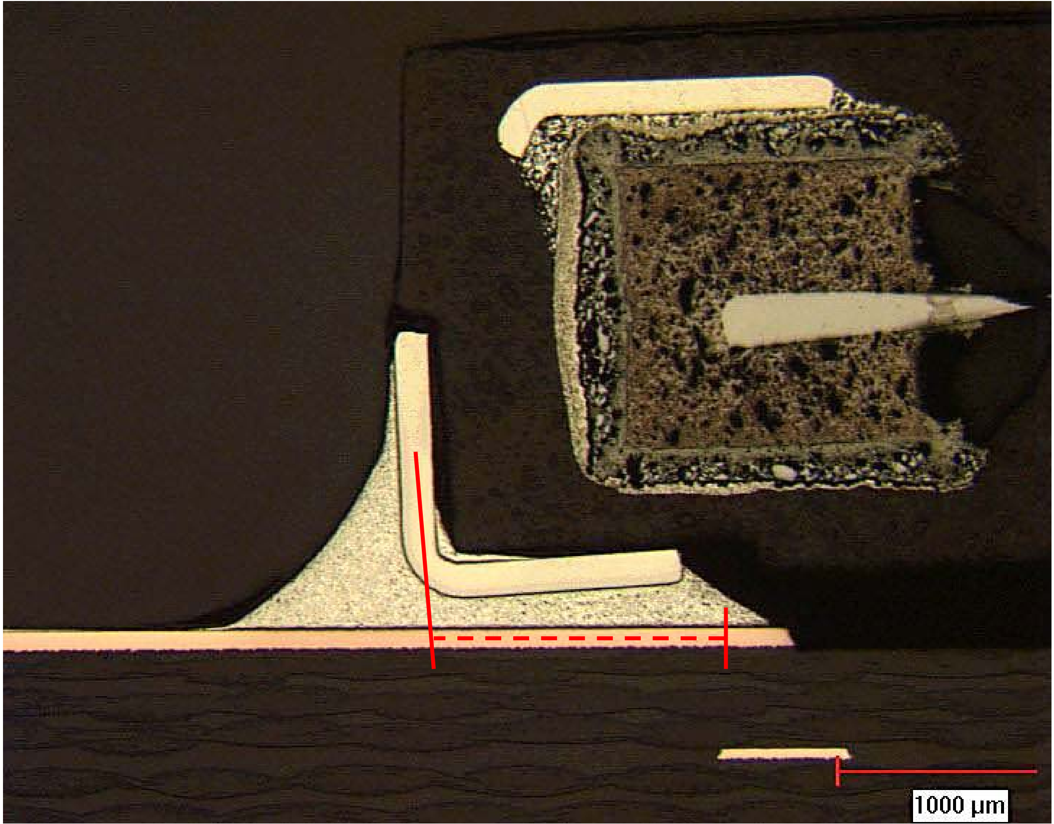
Chip Devices critical zone is shown by the dashed line



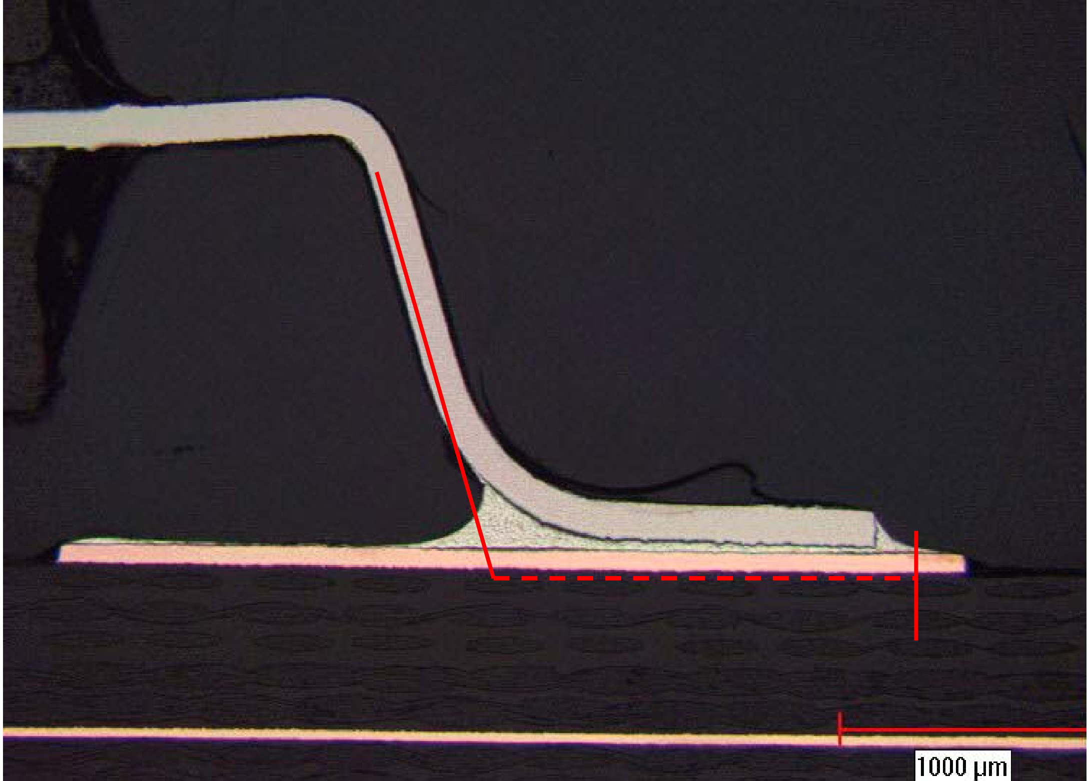
Diodes critical zone is shown by the dashed line



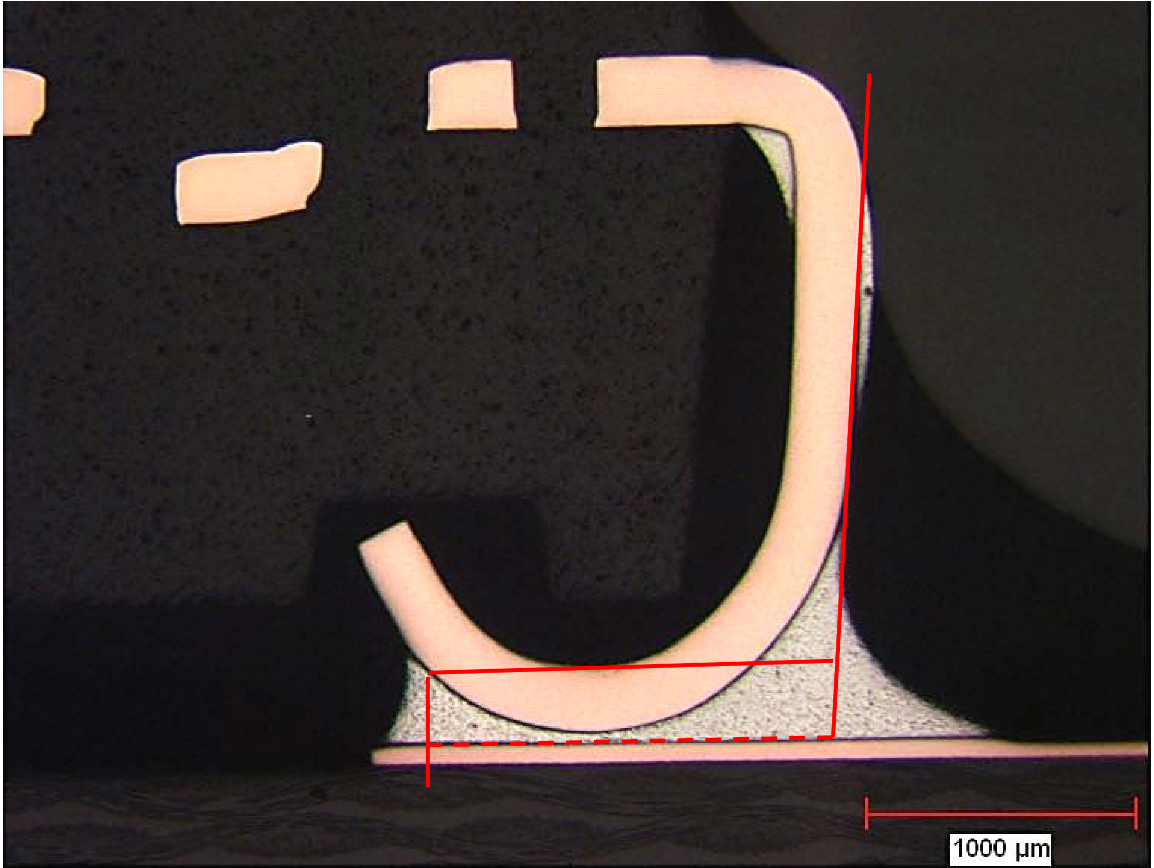
Castellated chip carriers critical zone is shown by the dashed line



CWR type of devices critical zone is shown by the dashed line



???????????????? is shown by the dashed line



J Leaded critical zone is defined by the dashed line

TSOP

For TSOP the fail criteria are any cracks detected in the critical zone.

The critical zone is shown for the three assembly configurations below

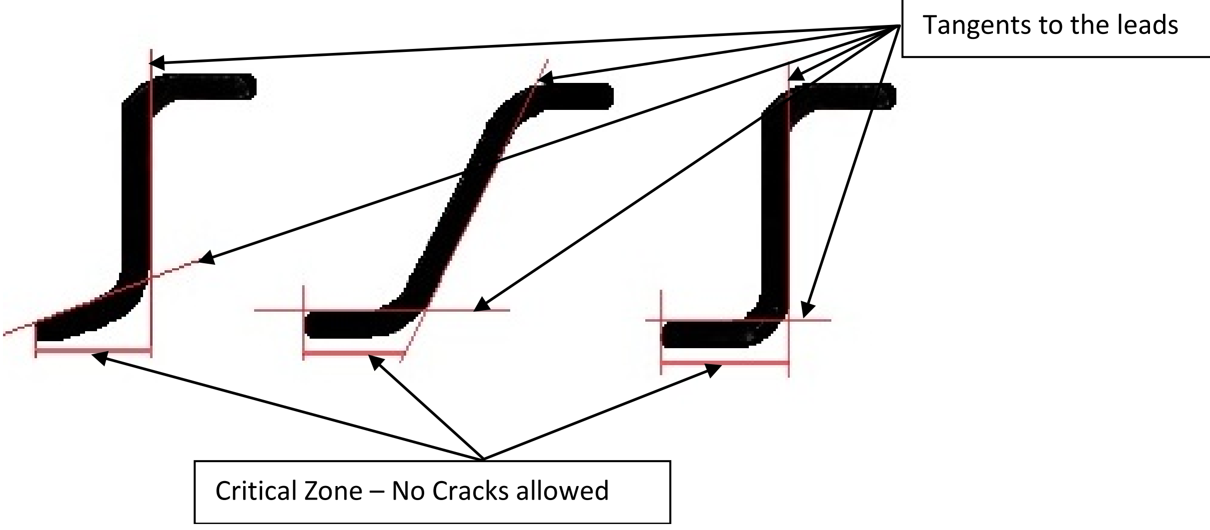


Figure 14-5 Illustrations defining critical zone in solder fillet

14.11 Approval of verification

a. A letter confirming the completion of a successful verification programme shall be sent to the contact person of the supplier from the approval authority, with the summary table specified in Annex I attached to it.

NOTE 1 The letter and the summary table provide evidence of the verification approval to a third party.

NOTE 2 The approval of verification applies to all space projects from the date of the approval until withdrawn.

NOTE 3 The summary table is prepared by the supplier and sent to the approval authority for approval

b. <<deleted>>

c. <<deleted>>

d. Reference to the summary table number shall be made on each space project declared processes list .

NOTE See ECSS-Q-ST-70, Table C-2.

14.12 Withdrawal of approval status

a. The approval status of the supplier shall be withdrawn when any of the following status justify its withdrawal:

1 Repetitive supply problems and manufacturing defects.

2 Undeclared changes to the PID.

3 Continuous non-compliance with the PID.

14.13 Conditions for delta verification

a. The supplier shall undertake a verification for any new configuration not covered by similarity rules in accordance with requirements from clause 14.2.

b. The delta verification shall be performed when changes are undertaken as specified in Table 14-2.

c. A delta-verification programme in accordance with the DRD from Annex H shall be submitted for approval to the approval authority.

Table 14-2: Conditions invoking verification

Changes	Test vehicles without any tests	Cleanliness tests (Ref 12.4)	Material compatibility with cleaning solvent	Full verification test programme
New device mounting configuration (example , already verified with conformal coating and now mounted without)				X
New SMD package size				X
New manufacturer of passive chips				X
New material of printed circuit board E.g. Epoxy, Polyimide, Ceramic, Aramid, mixed material build-up are different materials,				X
New thermal and/or mechanical adhesive				X
New conformal coating				X
New solder paste with same alloy, same powder size distribution, same flux activation type	X +microsections*	X		
New solder paste with new alloy, flux activation type and/or different physical-chemical characteristics				X
New flux activation type for hand solder	X +microsections*	X		
New cleaning solvent and or new cleaning process		X	X	
New reflow profile, Peak temp +/-5 , duration above liquids				X
New equipment to deposit soldering paste without change of process	X +microsections*			
New solder paste depositing process				X
New device placing equipment	X +microsections*			
New Device placing equipment of same process method	Visual inspection only			
New type of reflow equipment with process change				X
New reflow equipment without process change	X +microsections*			
Move Manufacture location outside the clean room approved in the PID	X +microsections*			
* for microsection, one part per family type from the summary table and or PID				

15 Quality assurance

15.1 General

a. ECSS-Q-ST-20 shall apply.

15.2 Data

a. ECSS-Q-ST-70-08 shall apply for "Data".

15.3 Nonconformance

a. ECSS-Q-ST-10-09 shall apply.

15.4 Calibration

a. ECSS-Q-ST-70-08 shall apply for "Calibration".

15.5 Traceability

a. ECSS-Q-ST-70-08 shall apply for "Traceability".

15.6 Workmanship standards

a. ECSS-Q-ST-70-08 shall apply for "Workmanship standards".

b. Visual standards consisting of work samples or visual aids that illustrate the quality characteristics of all soldered connections involved shall be prepared and be available to each operator and inspector.

NOTE The illustrations presented in clause 16 of this Standard can be included as part of the examples.

15.7 Inspection

a. During all stages of the process, the inspection points defined in the manufacturing flow chart shall be carried out.

b. The inspection shall be performed in conformance with clause 13 of this Standard.

c. <<deleted>>

15.8 Operator and inspector training and certification

a. ECSS-Q-ST-70-08 shall apply for "Operator and inspector training and certification".

b. A training programme for operators and inspectors performing all processes contained within the PID shall be developed, maintained and implemented by the supplier to provide excellence of workmanship and personal skill in SMTs.

NOTE Records of training, testing and certification status of the operators are maintained for at least 10 years.

c. Operators and inspectors shall be trained and certified at a school or in-house training authorised by the approval authority.

d. The operators performing X-ray inspection shall be trained and in-house certified to perform and assess X-ray results.

15.9 Quality records

a. The following documents, as a minimum, shall be made available;

1 PID.

2 Audit report established by the approval authority.

3 Verification report.

16 Visual and X-ray workmanship standards

16.1 Workmanship illustrations for standard SMDs

16.1.1 Chip components

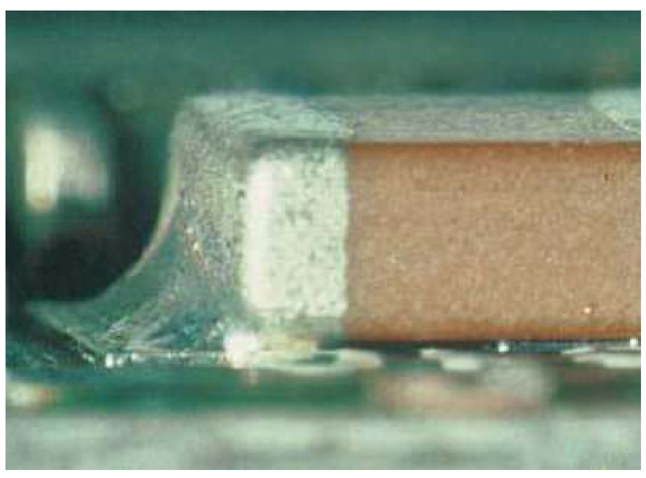


Figure 16-1: Preferred solder (see also Table 11-1)

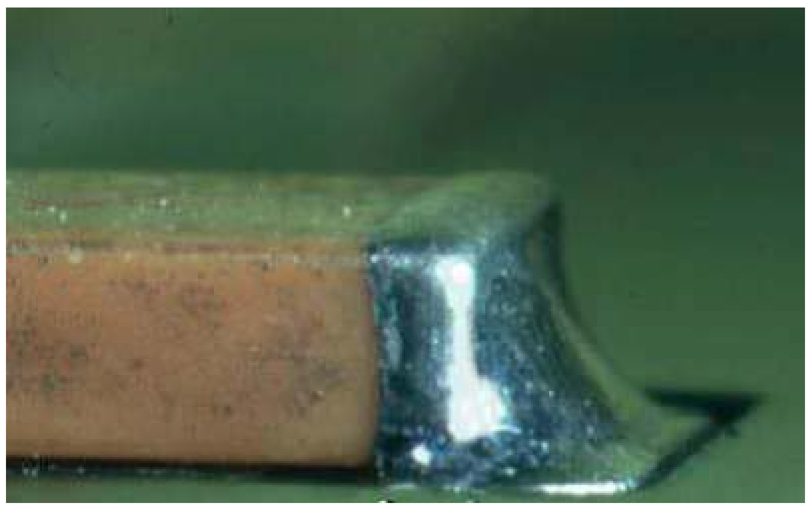


Figure 16-2: Acceptable, maximum solder (see also Table 11-1)

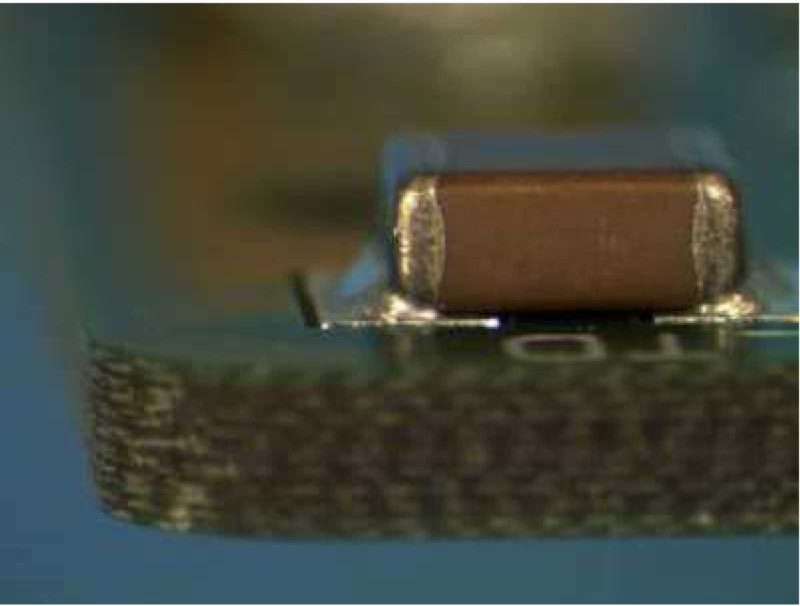


Figure 16-3: Acceptable, minimum Solder (see also Table 11-1)

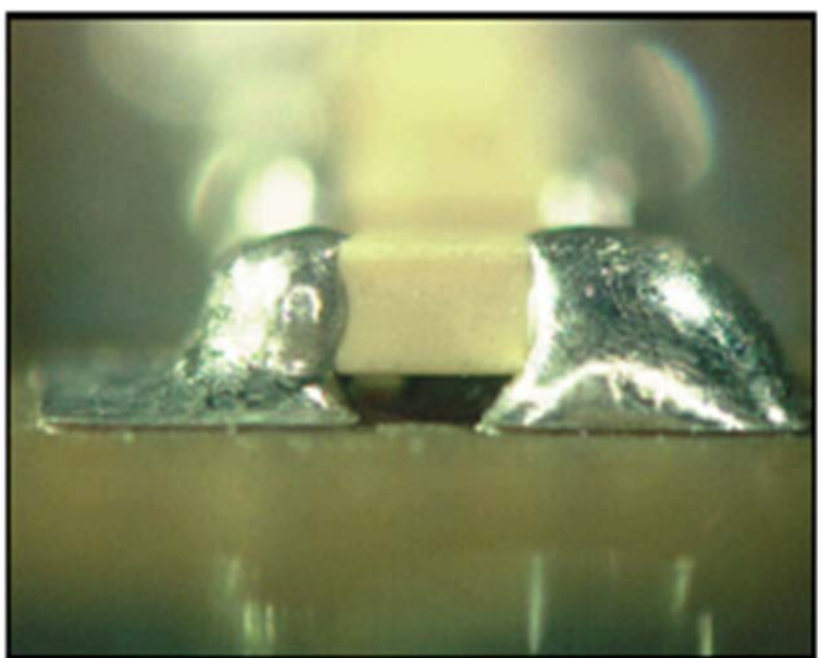


Figure 16-4: Unacceptable, excessive solder (see also Table 11-1)

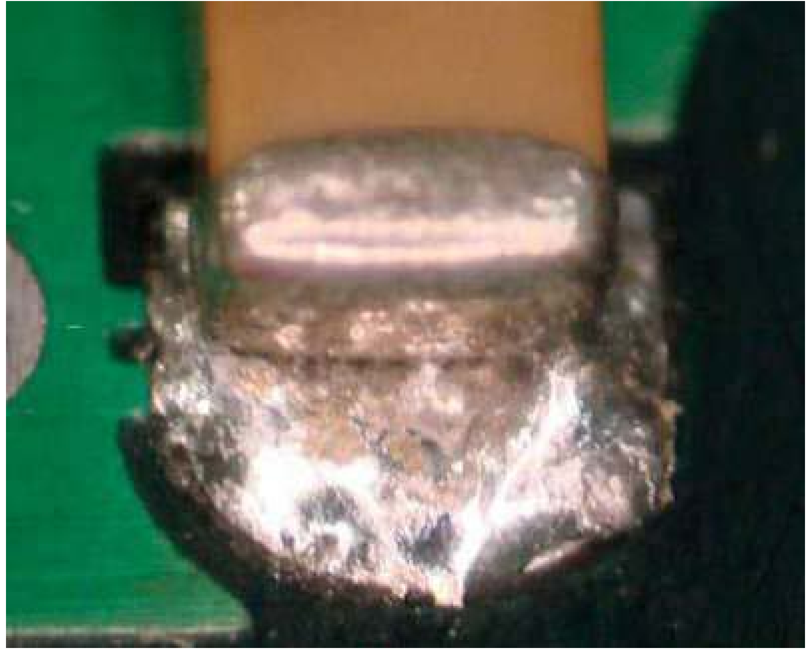


Figure 16-5: Unacceptable, poor wetting (see also Table 11-1)

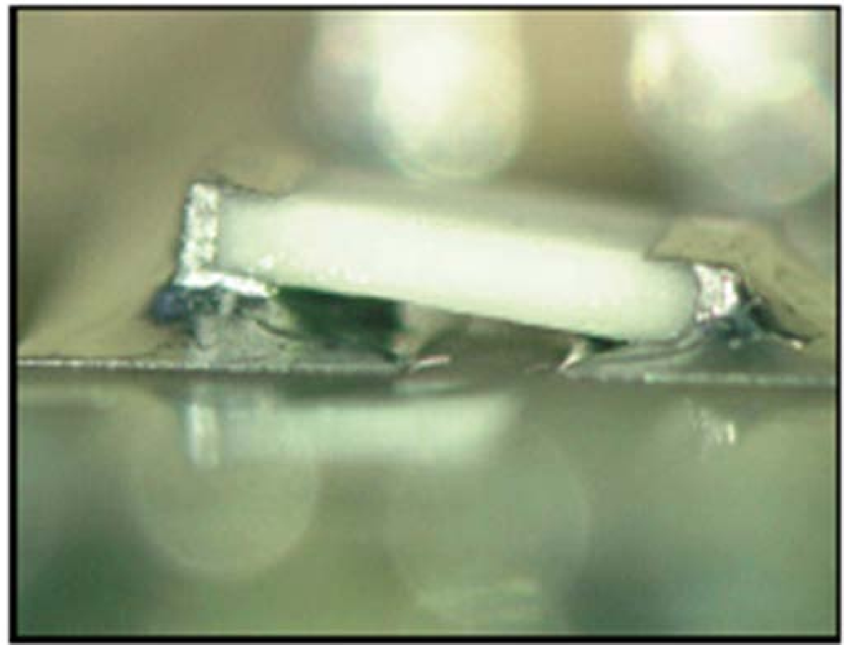


Figure 16-6: Unacceptable, excessive tilt (see also Table 11-1)

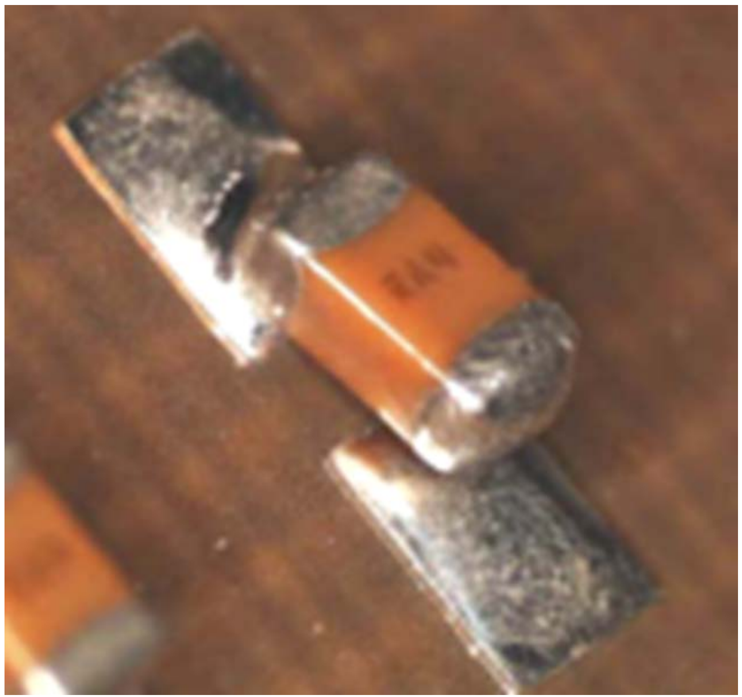


Figure 16-7: Unacceptable, tombstone effect

Figure 16-8: Examples of Unacceptable solder joints - (see also Table 11-1)

16.1.2 MELF components

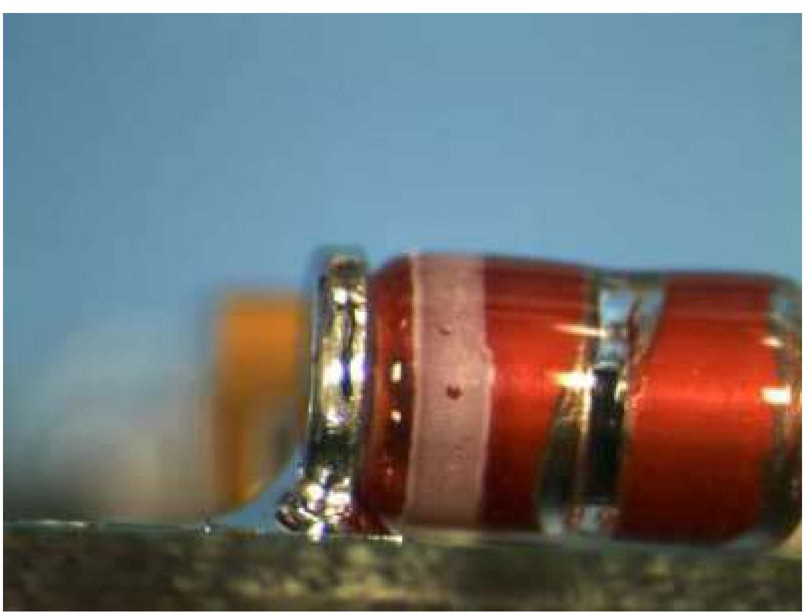


Figure 16-9: Acceptable-- Terminal wetted along end, face and sides (see also Table 11-1)

Figure 16-10: Acceptable maximum solder joint (see also **Table 11-3**)

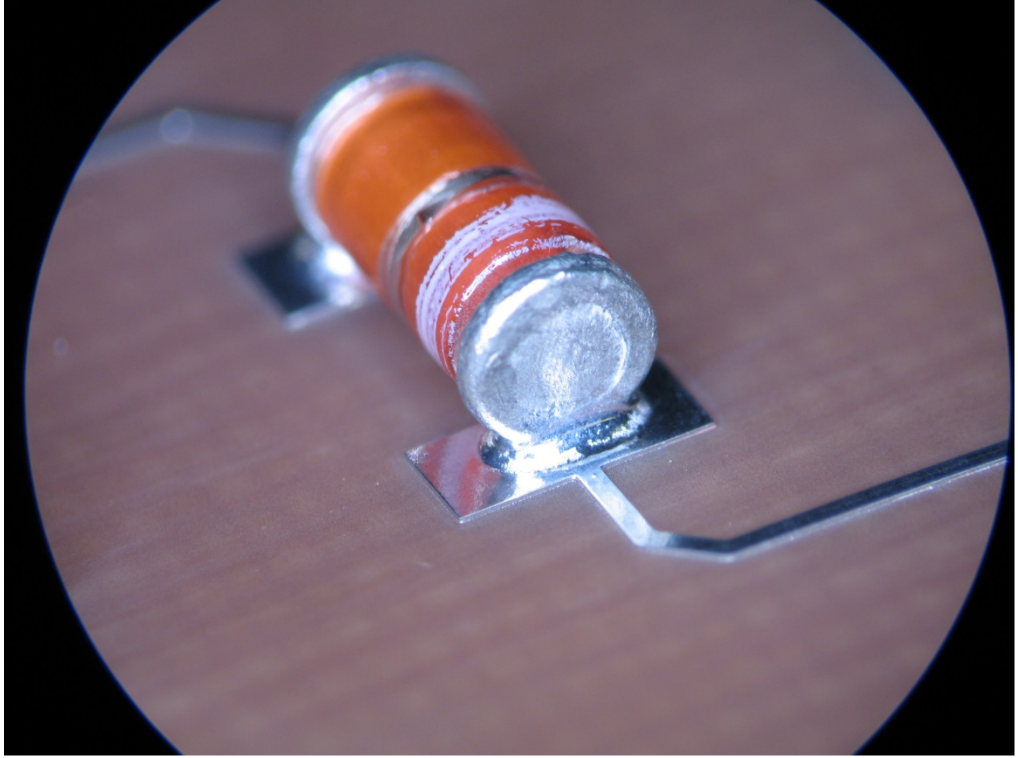


Figure 16-11: Not Acceptable insufficient solder joint (see also Table 11-3)

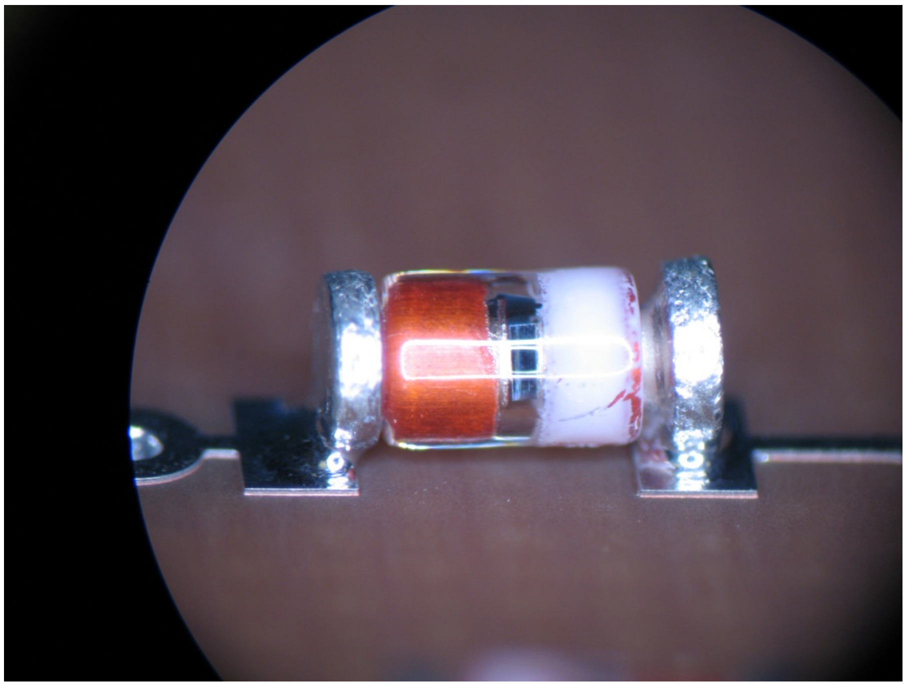
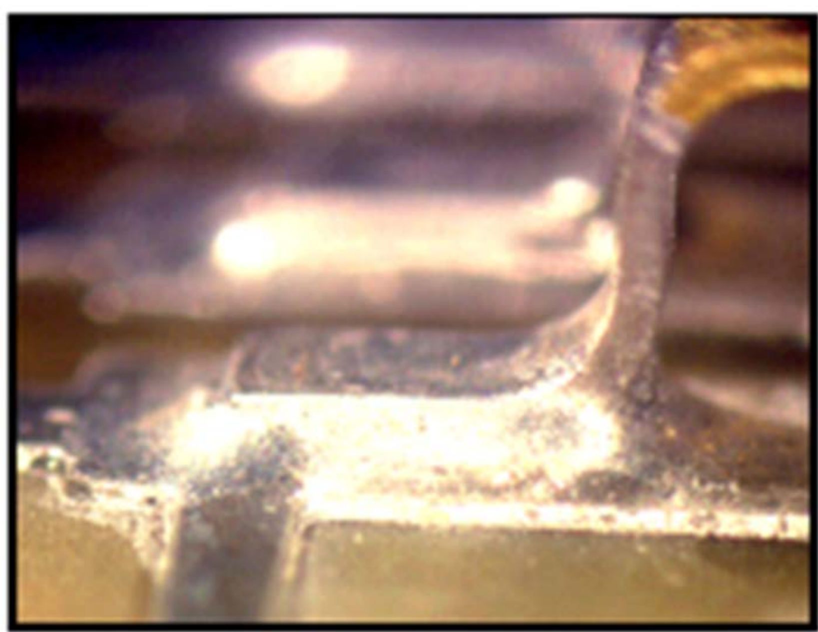


Figure 16-12: Unacceptable overhang

16.1.3 Ribbon, "L" and Gull-wing leaded devices



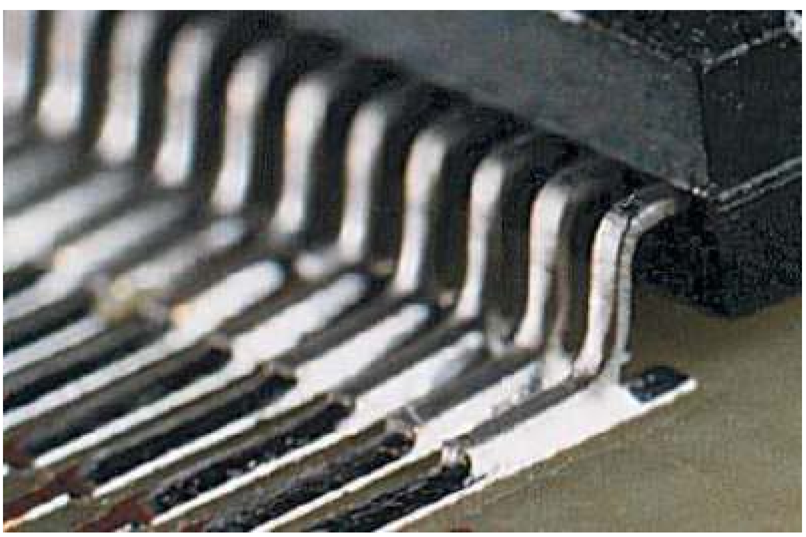


Figure 16-13: Examples of Gullwing leads: Acceptable

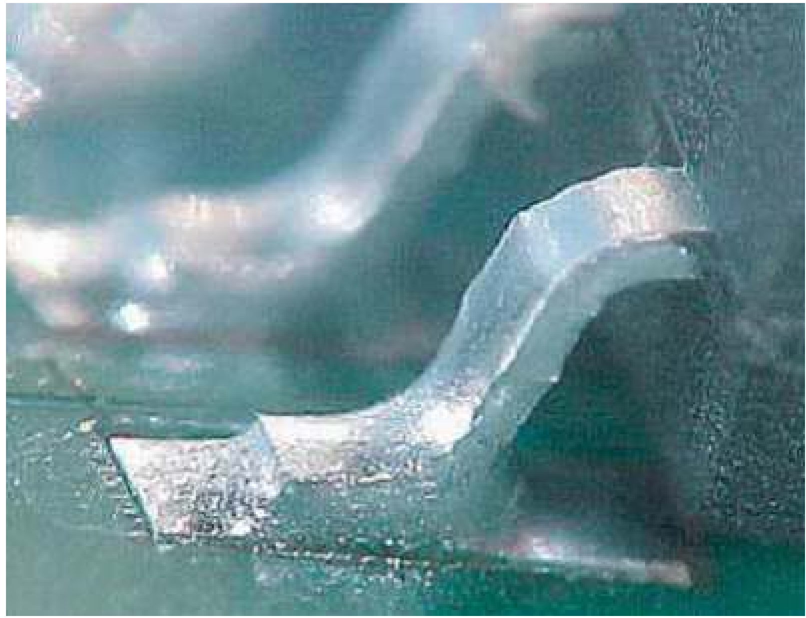


Figure 16-14: Examples of flattened leads: Acceptable

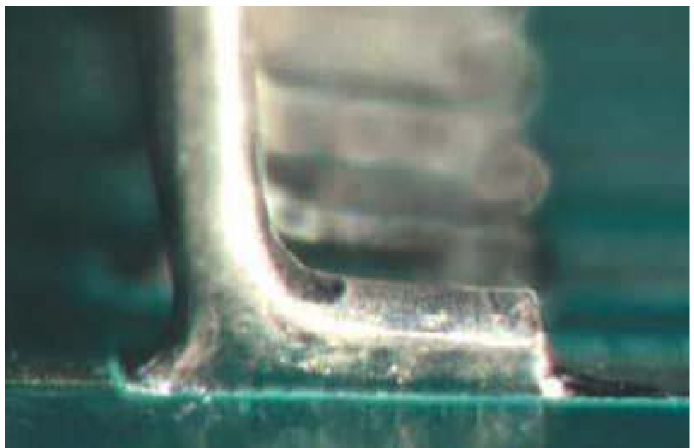


Figure 16-15: Acceptable, minimum solder joint

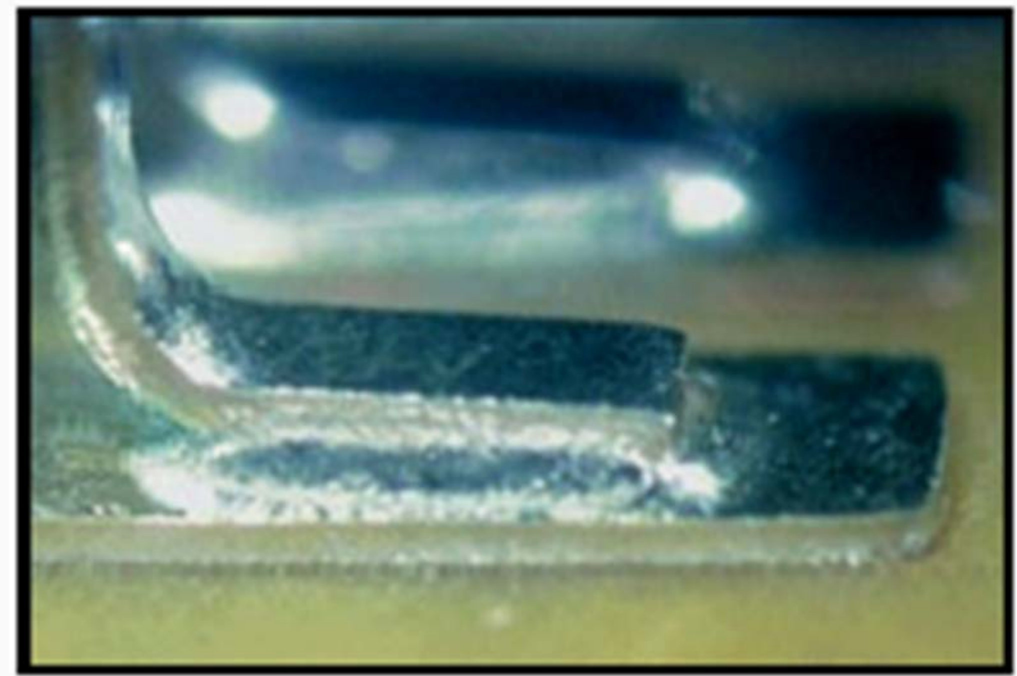


Figure 16-16: Unacceptable, insufficient heel fillet

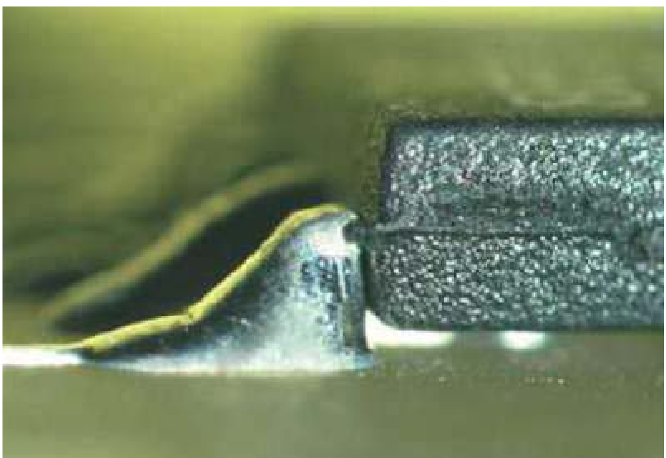


Figure 16-17: Unacceptable -- Excessive solder

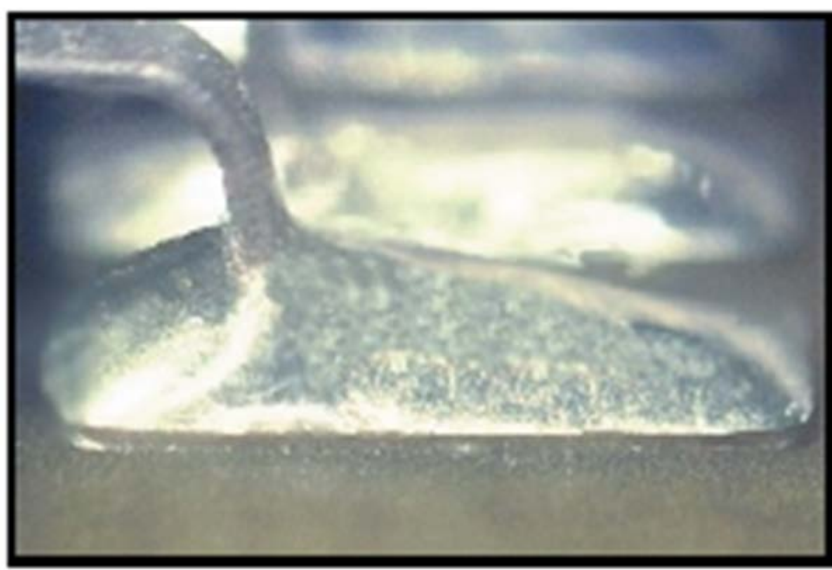


Figure 16-18: Unacceptable -- Excessive solder

16.1.4 “J” leaded devices

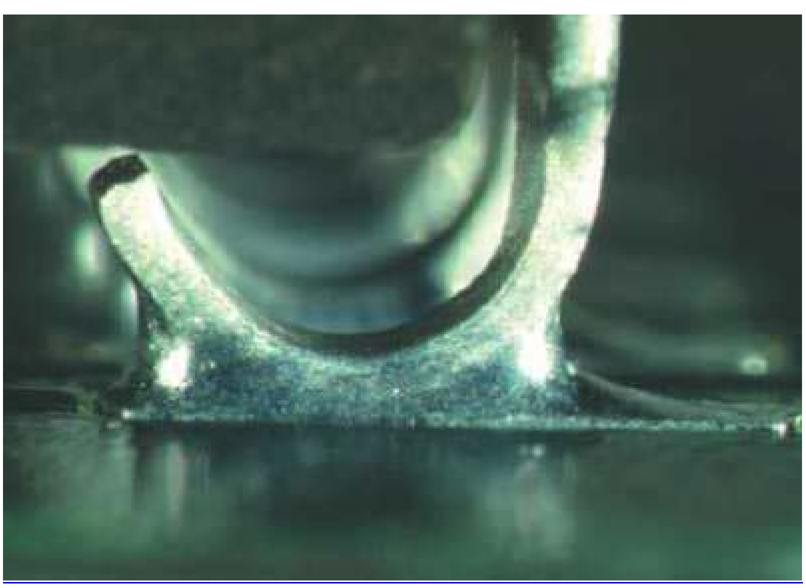


Figure 16-19: Preferred solder joint

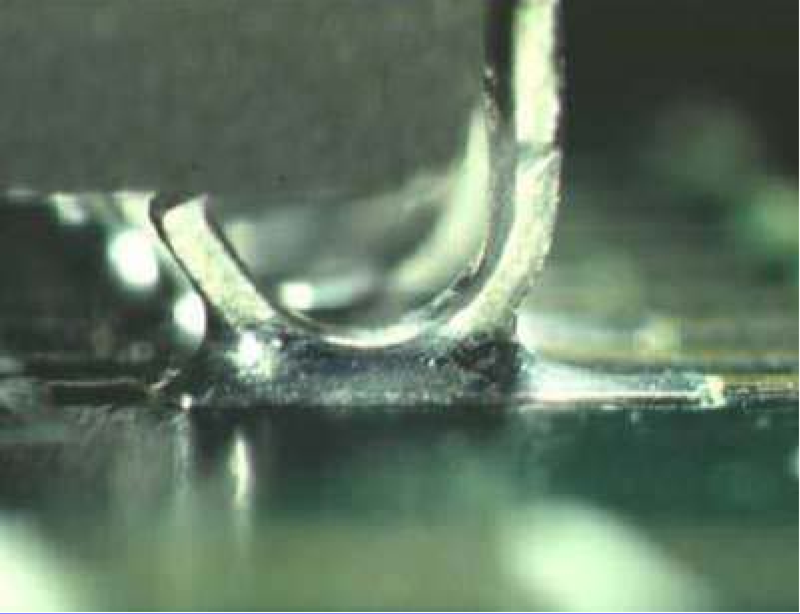


Figure 16-20: Acceptable solder joint

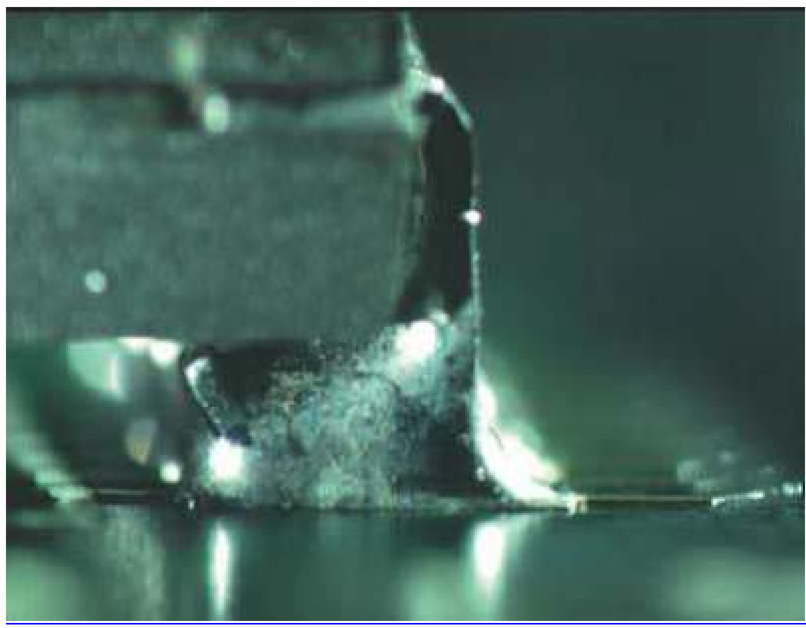


Figure 16-21: Unacceptable, excessive solder joint

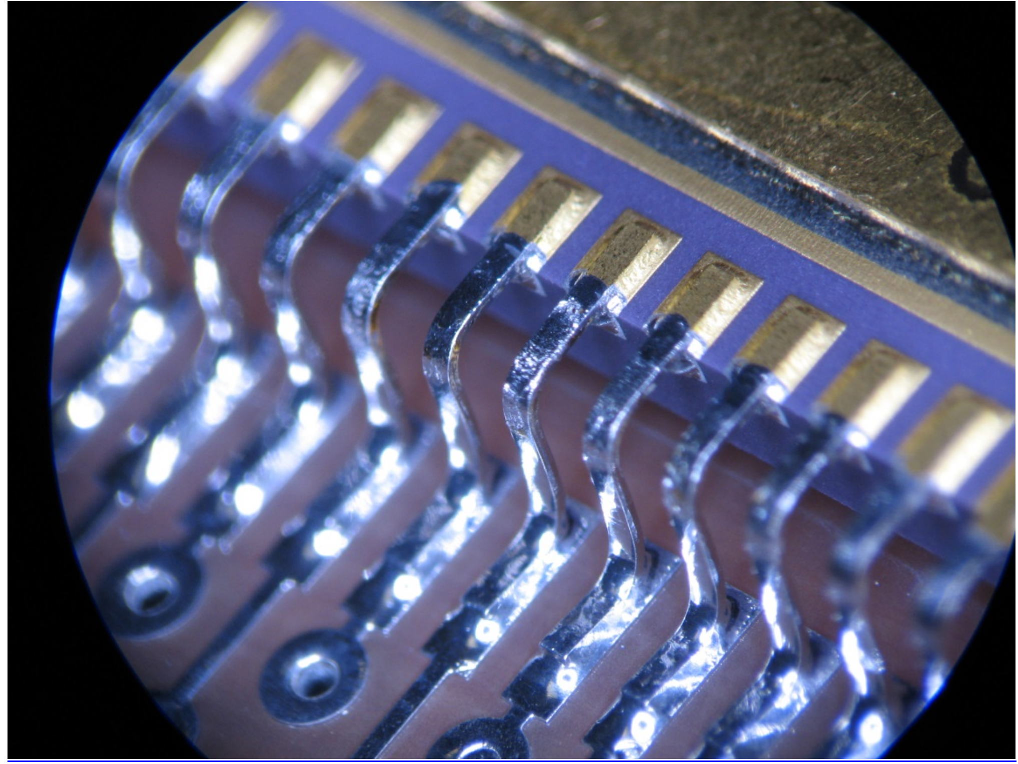


Figure 16-22: Unacceptable, excessive degolding

16.1.5 L-shape Inward leaded Component

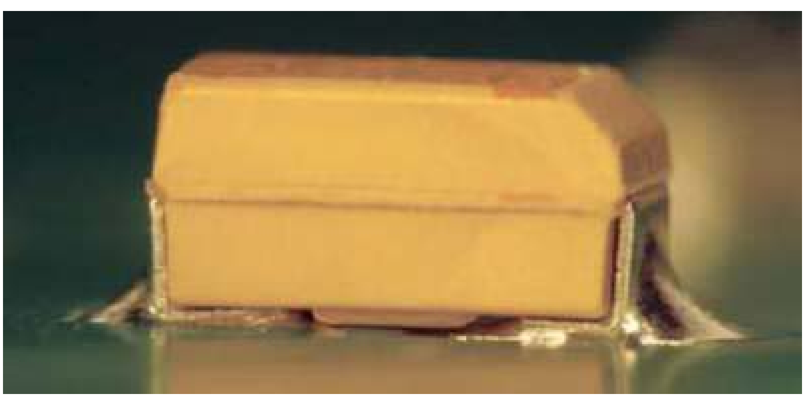


Figure 16-23: Acceptable, preferred solder joint

16.1.6 LCC devices

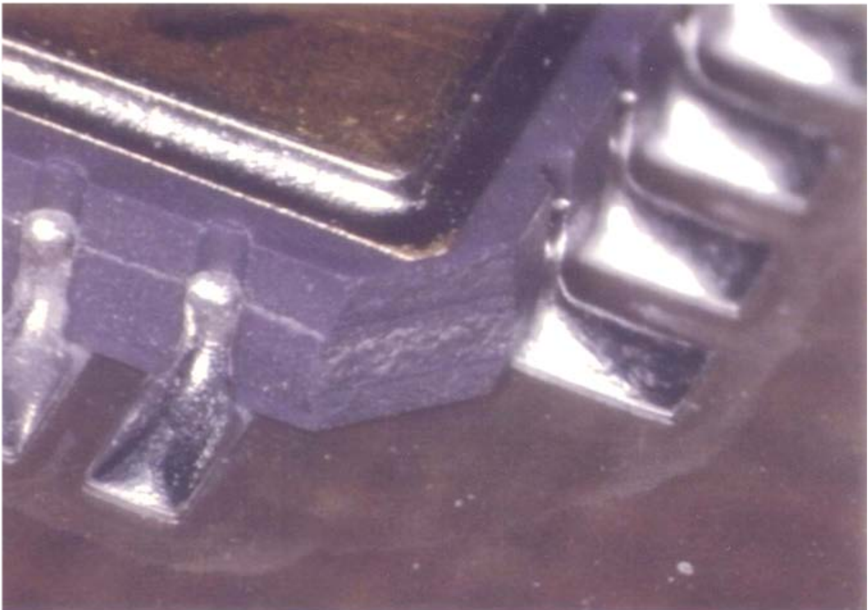
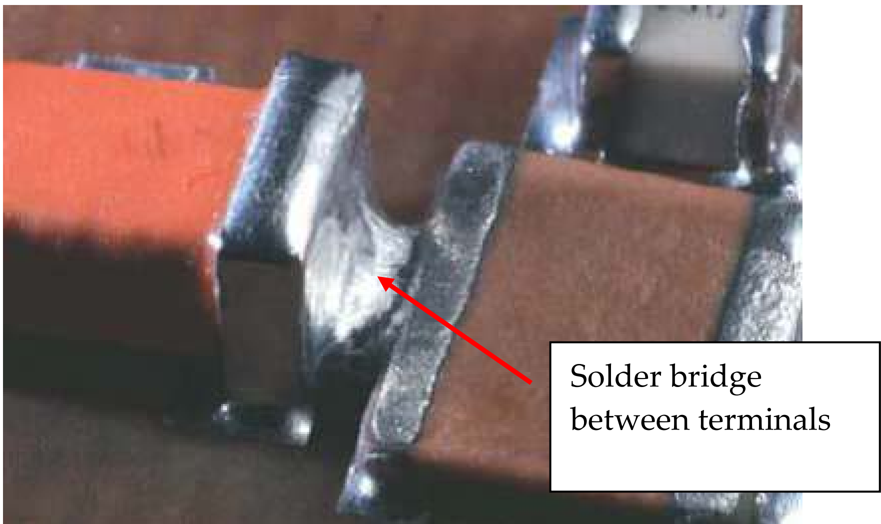
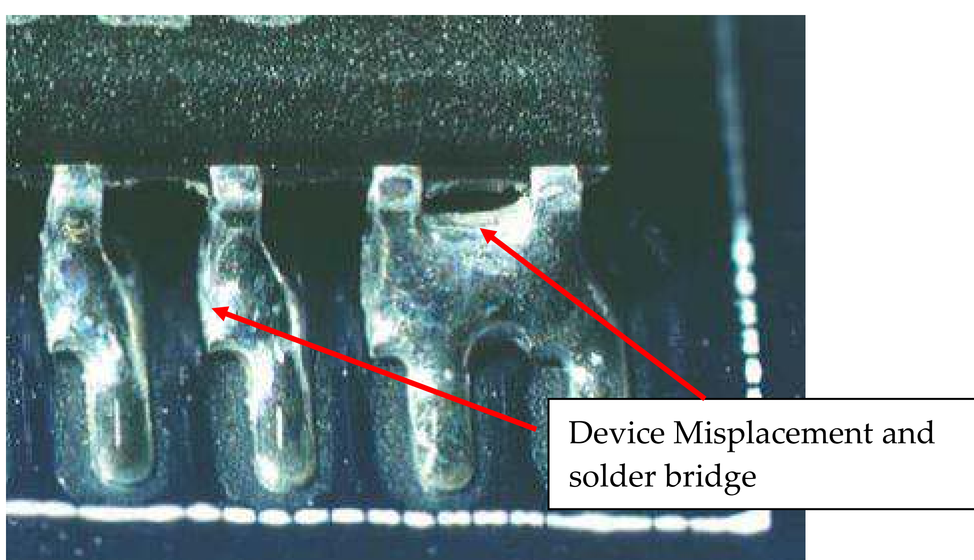


Figure 16-24: LCC General View Acceptable solder joints

16.1.7 Miscellaneous soldering defects





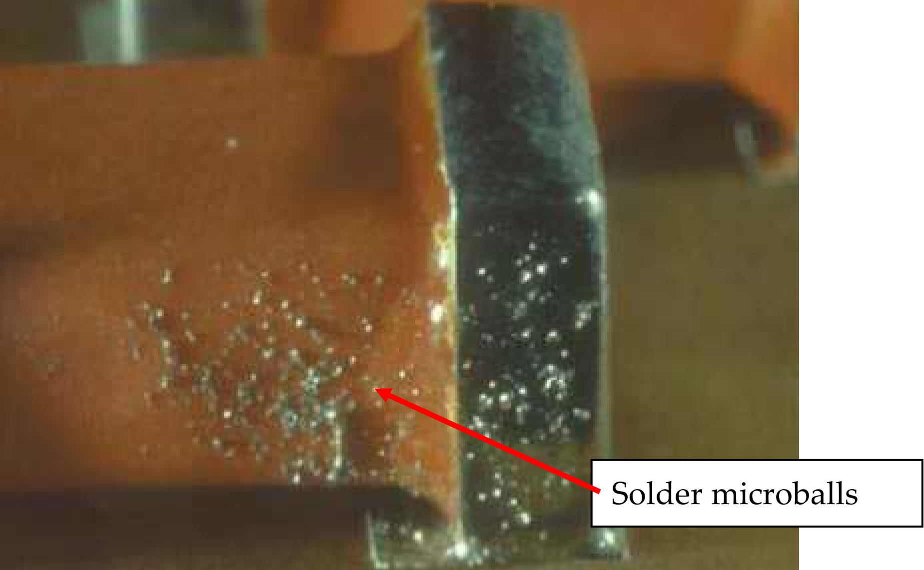


Figure 16-25: Examples of unacceptable soldering

16.2 Workmanship illustrations for ball grid array devices

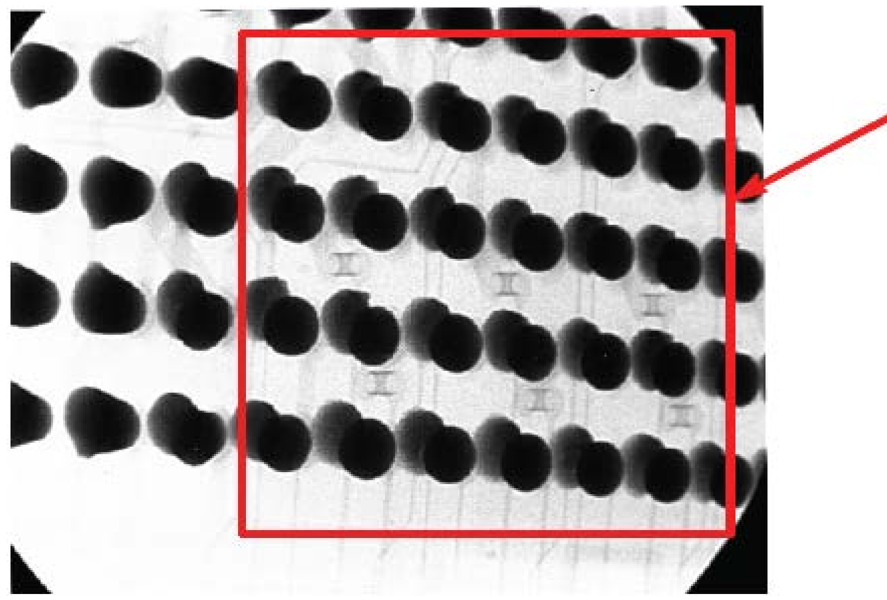
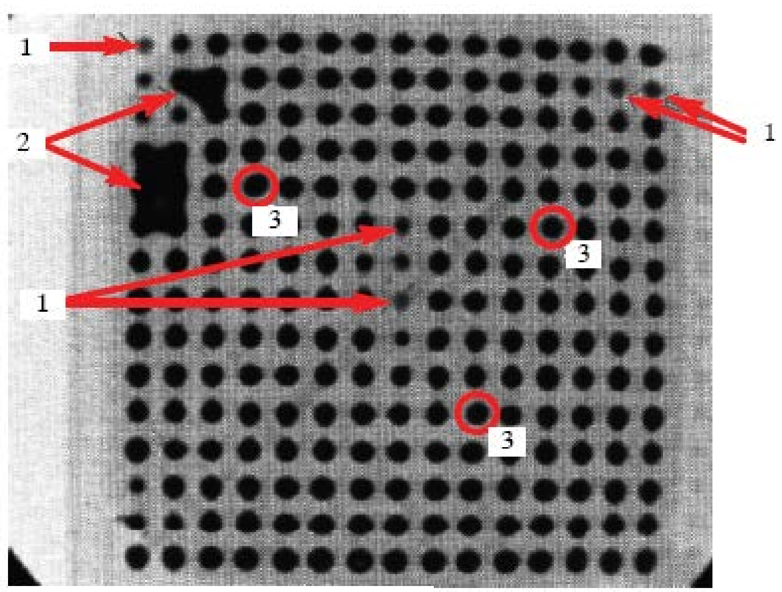


Figure 16-26: Angled-transmission X-radiograph showing solder paste shadow due to partial reflow: Reject

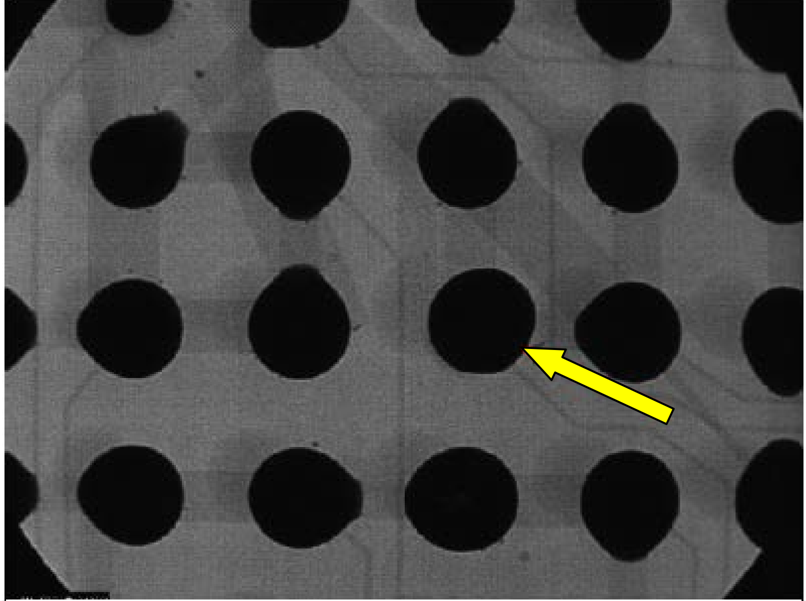
- non-reflow of solder paste: Reject

Figure 16-27: Micrograph showing



1. missing balls: Reject
2. bridges: Reject
3. non-wetted pads: Reject

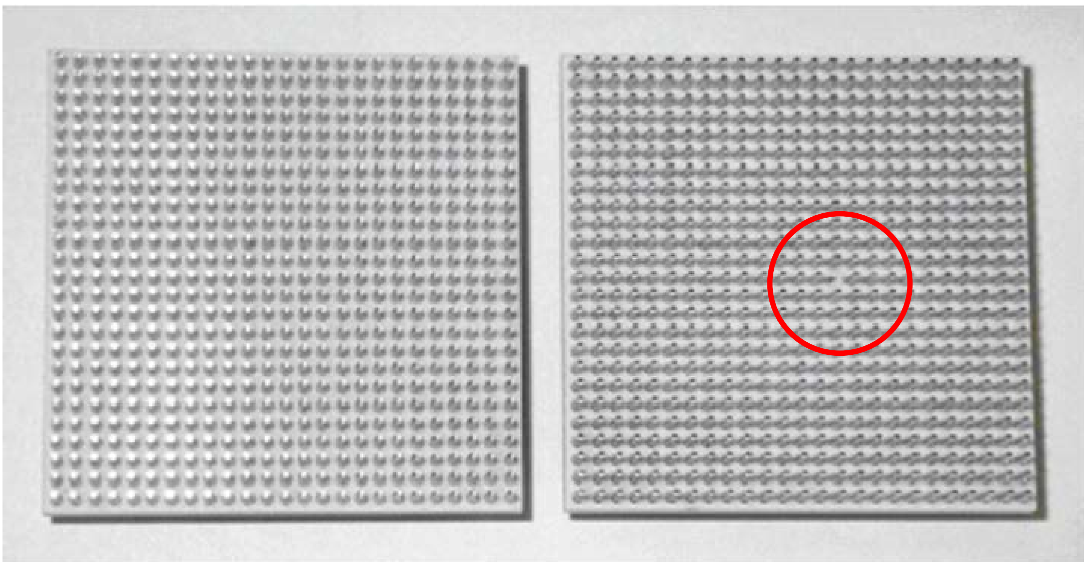
Figure 16-28: Perpendicular transmission X-radiograph showing unacceptable defects



Solder has not flowed to extent of teardrop pad: Reject

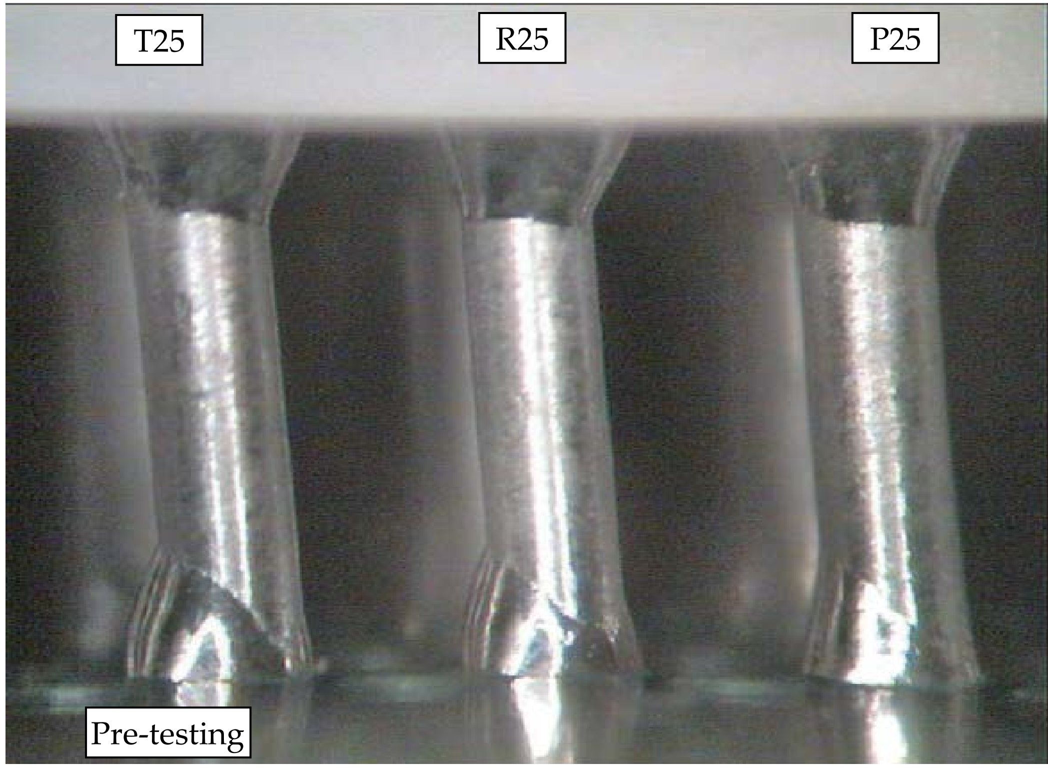
Figure 16-29: Perpendicular transmission X-radiograph showing non-wetted pad

16.3 Workmanship illustrations for column grid array devices



Good consistency of column alignment: Accept Missing column: Reject.

Figure 16-30: Underside view showing missing column



NOTE: Asymmetry of solder fillets at PCB is consequence of teardrop pads and is acceptable

Figure 16-31: CGA mounted on PCB showing columns tilted < 10°: Accept

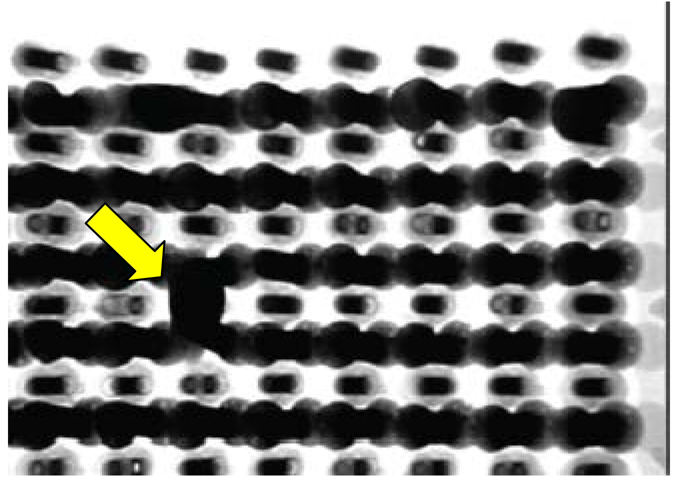


Figure 16-32: X-radiograph of CGA mounted on PCB showing solder bridge: Reject

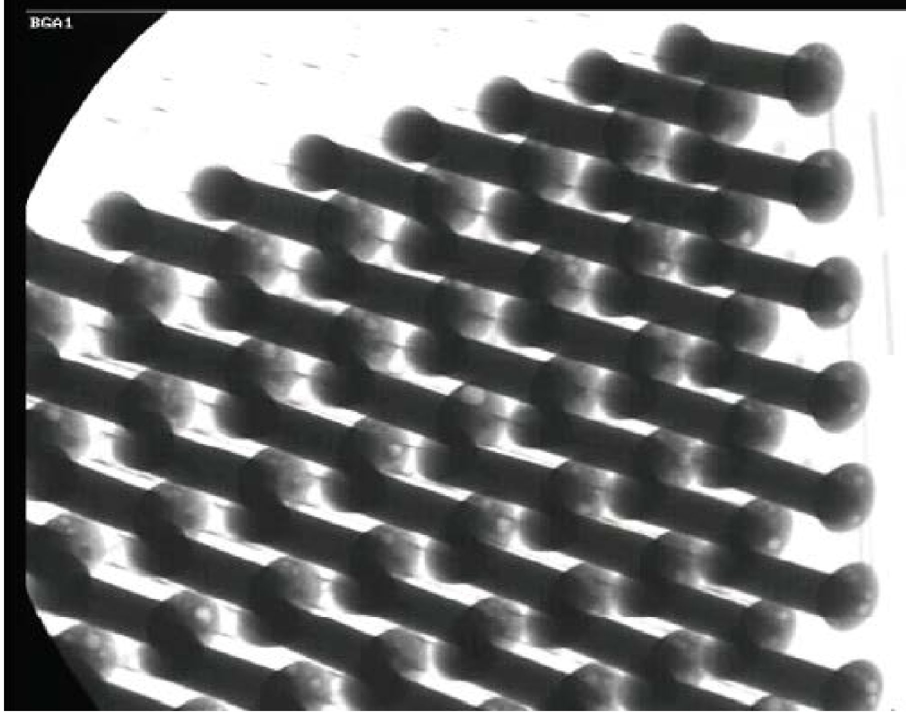
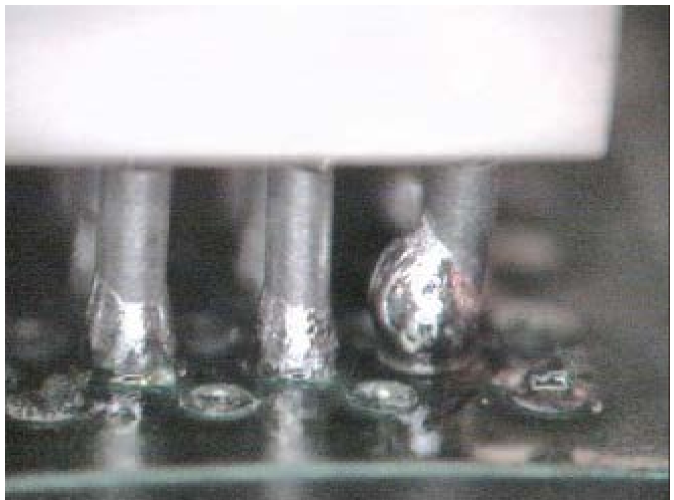


Figure 16-33: X-radiograph of CGA showing solder fillets at base of columns: acceptable

Figure 16-34: Micrograph of CGA mounted on PCB, bent column: reject



Unsoldered column: Reject.

Figure 16-35: Micrograph of CGA mounted on PCB

16.4 Micro section

<<Images deleted>>

16.4.1 Device microsection

SMD type	Cross sections planes	Example of views at min and max magnifications.
SOT23		x50
TO252 D2 Pak SOT 223		x200 X Ray+ micro section (lead + plane)
LCC3	With ground connection Without ground connection	x100 x200 x500
LCC6		

SMD type	Cross sections planes	Example of views at min and max magnifications.
LCC with termination on 4 faces		x100 x500
FP, SO, SOIC		x50 x200 x200
FP with spider leads		See FP

SMD type	Cross sections planes	Example of views at min and max magnifications.
Encapsulated Magnetics		x25 x100 x200
Chip resistor		x50 x200

SMD type	Cross sections planes	Example of views at min and max magnifications.
Array resistors		x20 x100 x200
CTC,CWR		x50 x200
Chip Capacitors	It is important to have microsection at edge and middle of the capacitor	x50 x200

SMD type	Cross sections planes	Example of views at min and max magnifications.
MELF Diode		x50 x100 x200

SMD type	Cross sections planes	Example of views at min and max magnifications.
SMDXX	+ X Ray	x25 x50 x100 x200 To check absence of cracks in the ceramic by visual inspection

SMD type	Cross sections planes	Example of views at min and max magnifications.
Tantalum chip capacitor		x25 x200
Leaded capacitors		
CQFP + MQFP	Centre Micro-section to be done only if device is bonded.	x50 x100 x200 Similar magnification to be applied for the assessment of the bonding lines.

SMD type	Cross sections planes	Example of views at min and max magnifications.
Area Array devices (Capability Phase only)		x25 x100 x200
Microsections plane		
Terminals to be microsectioned		

16.5 <<deleted>>

<<Images deleted>>

Annex A (informative) <<deleted>>

Annex B (informative) <<deleted>>

Annex C (informative) <<deleted>>

Annex D (informative) Example of an SMT audit report

ECSS-Q-ST-70-38C Rev1: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 1	**COMPANY DETAILS**					
1. NAME						
2. ADDRESS						
3. TEL						
4. FAX						
5. MANAGING DIRECTOR						
6. QUALITY MANAGER						
7. PRODUCTION MANAGER						
8. SMT CONTACT PERSON						
9. SMT PRODUCT RANGE AND HISTORY (brief summary)						
10. Numbers of SMT operators		Design Engineers			QA	

ECSS-Q-ST-70-38C Rev1: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 2	**QUALITY SYSTEM**					
1. QUALITY MANUAL* Reference:						
Issue:						
Date:					Viewed	Y ☐ N ☐
2. ORGANISATION OF THE QUALITY DEPARTMENT FOR SMT						
3. INTERNAL QUALITY AUDIT SYSTEM Reference:						
Date of last audit:						
Comments:					Viewed	Y ☐ N ☐
4. NON-CONFORMANCE SYSTEM Reference:						
	No. of NCRs in previous 12 months:		No. open at audit date:		Viewed	Y ☐ N ☐
5. CURRENT QUALITY APPROVALS Date of last assessment						
6. COMMENT ON COMMITMENT TO ECSS-Q-ST-70-38						
7. REFERENCE TO GENERAL ESA AUDIT & Date						

* Note: Request that a copy of the Contents List of the Quality Manual be appended to this report (See Attachment 1).

ECSS-Q-ST-70-38C Rev1: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 3	**PROCESS CONTROL**
1. SMT APPROVED (if any) Make reference to an existing list of SMT configurations considered already tested. Identify how the SMT was tested.	

2. Make reference to the procedures that have the following functions and identify current issue and date:	
Process Identification Document	
1. Process instructions	Viewed: Y ☐ N ☐
2. Workmanship acceptance/rejection criteria	Viewed: Y ☐ N ☐
3. Calibration of SMT tooling	Viewed: Y ☐ N ☐
4. Control of limited Shelf life materials	Viewed: Y ☐ N ☐
5. Material procurement control with CofC or CofTest	Viewed: Y ☐ N ☐

3. TRAINING Make reference to the procedure for operator and inspector training. Identify the number of certificated operators and inspectors.	Viewed: Y ☐ N ☐ Certificates viewed: Y ☐ N ☐

ECSS-Q-ST-70-38C Rev1: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

<table>
<tr><td>SECTION 4</td><td>FACILITIES</td></tr>
<tr><td colspan="2">CHECK LIST</td></tr>
<tr><td>Devices storage and kitting area.</td><td></td></tr>
<tr><td>Humidity and temperature control</td><td></td></tr>
<tr><td>ESD protection and control</td><td></td></tr>
<tr><td>Cleanliness in assembly areas</td><td></td></tr>
<tr><td rowspan="7">Calibration</td><td>ESD (floor, mat, chair, wrist, solder iron….):</td></tr>
<tr><td>Degolding, pretinning bath:</td></tr>
<tr><td>Lead forming:</td></tr>
<tr><td>Machine reflow:</td></tr>
<tr><td>Solder tip:</td></tr>
<tr><td>Repair station:</td></tr>
<tr><td>Ovens:</td></tr>
<tr><td rowspan="3">Lighting in Lux</td><td>Degolding:</td></tr>
<tr><td>Pretinning:</td></tr>
<tr><td>Lead forming:</td></tr>
</table>

	HS Assembly:
	Stacking, bonding:
	Conformal coating:
PCB drying ovens and procedure	Unpopulated:
	Populated without conformal coating:
	Populated with conformal coating:
Oven	Baking of naked PCB:
	Baking of populated PCB:
	Curing of adhesive:
	Curing of conformal coating:
	Repair prior conformal coating
	Repair after conformal coating:
Bending tools	
Magnification aids	Device preparation (degolding, pretinning, lead forming):
	After solder paste application:
	After assembly by machine reflow:
	During assembly by hand:
	Final inspection:
Degolding bath (250°C-280°C)	
Pretinning (210-260°C)	

Solder fluxes (internal and external) used. Flux activity and trademark.	Degolding, pretining:
	Solder paste:
	Hand soldering:
Cleaning Solvents	PCB cleaning:
	Degolding, pretinning:
	Soldering by machine reflow:
	Solder screen
	Soldering by hand:
	Prior to bonding, stacking:
	Prior to conformal coating:
Solder alloys (chemical composition, supplier, trademark and associated flux	-Dispensing:
	Screen printing:
	HS:
Solder paste application	Stencil:
	Dispensing:
	Repair station:
Pick and place machine	
Machine reflow	
Is the soldering equipment well controlled (temperature-time profile, speed	Machine reflow:
	Solder Iron:

control…). How is the temperature profile controlled on the flight hardware?	
Hand Soldering iron (280°C to 340°C max)	
Fume exhaust facilities	
Repair station	
Cleaning Equipment	Machine reflow
	Hand soldering:
Cleanliness Testing (< 1,6 µg/cm^2)	
Staking , bonding compounds	
Refrigerators: check expiration dates for staking compounds, conformal coatings	Solder paste:
	Adhesive:
	Conformal coating:
Conformal Coating used	Curing conditions:
Cleanliness in conformal coating facilities	
Areas for Non-Conforming Items (Quarantine)	
Laboratories exist for: - Temperature cycling - Vibration - Electrical testing - Microsectioning	

SMT Assembly Traveller (operator activities, inspector stamps)	

END OF SECTION 4

ECSS-Q-ST-70-38C Rev1: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 5	**FINAL ASSESSMENT**

AN ASSESSMENT OF THE SURFACE MOUNT TECHNOLOGY LINE AT THE FOLLOWING SUPPLIERS FACILITY HAS BEEN UNDERTAKEN AND THE FOLLOWING CONCLUSIONS MADE:

Supplier:
Address:

THE FACILITIES FOR THE ASSEMBLY OF SURFACE MOUNT TECHNOLOGY (ACCORDING TO ECCS-Q-ST-70-38C AT THE ABOVE SUPPLIER'S SITE ARE CONSIDERED:

SUITABLE CONDITIONALLY SUITABLE NOT SUITABLE

SUMMARY OF FINDINGS/CONDITIONS OF APPROVAL/SUMMARY OF CORRECTIVE ACTIONS NECESSARY:

Actions	**Findings**	**Due date**

NAME SIGN

PROCESS ASSESSMENT CARRIED OUT BY (Approval Authority):

IN PRESENCE OF (CONTRACTOR):

DATE:

Approval Authority: DATE:

END OF DOCUMENT

Annex E (informative) Additional information

E.1 <<deleted>>

<<deleted>>

E.2 Melting temperatures and choice

Table E-1: Guide for choice of solder type

Solder type	Melting range (□		Uses
	Solidus	Liquidus	
63 tin solder (eutectic)	183	183	Soldering printed circuit boards where temperature limitations are critical and in applications with an extremely short melting range. Preferred solder for surface mount devices.
62 tin silver loaded	179	190	Soldering of terminations having silver and or silver palladium metallization. This solder composition decreases the scavenging of silver surfaces.
60 tin solder	183	188	Soldering electrical wire/cable harnesses or terminal connections and for coating or pretinning metals.
96 tin silver (eutectic)	221	221	Can be used for special applications, such as soldering terminal posts.
75 indium lead	145	162	Special solder used for low temperature soldering process when soldering gold and gold-plated finishes. Can be used for cryogenic applications.
70 indium lead	165	175	For use when soldering gold and gold-plated finishes when impractical to degold.
50 indium lead	184	210	This solder has low gold leaching characteristic.
10 tin lead	268	290	For use in step-soldering operations where the initial solder joint must not be reflowed on making the second joint (e.g. CGA columns, connections internal to devices)

Annex F (normative) Process identification document (PID) - DRD

F.1 DRD identification

F.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-38, requirement 5.1.2a.

F.1.2 Purpose and objective

The purpose of the PID is to consolidate the overall management, process and facilities utilised during the manufacturing and verification of the SMD.

F.2 Expected response

F.2.1 Scope and content

<1> SECTION 1: Document Format

a. The PID shall contain the following information about the Document Format:

1. Cover page: document title, document reference, revision number and date, page numbering, signing of Production and Quality representatives,
2. Follow-up of PID updates: registration of PID updates indicating the nature of the update and the sections and pages updated,
3. Purpose and scope of the document,
4. Table of contents.

<2> SECTION 2: Manufacturing control

a. The PID shall contain the Manufacturing control flow chart of the verified SMT.

NOTE 1 This illustrates the various stages of procurement, manufacturing and inspection operations specific to this technology in a flow chart format.

NOTE 2 It can be used to identify, among others:

- the operation,
- the body responsible for its implementation,
- related documents: (only their reference),
- procurement specifications (for materials),
- acceptance inspection procedures (for materials and devices),
- manufacturing procedures,
- manufacturing and quality control procedures during and at the end of production.

<3> SECTION 3: Specifications

a. The PID shall contain the following information about Specifications:

1 List of procurement specifications, assembly procedures and inspection procedures concerning the technology dealt within the PID.

2 Printed circuit design rules in compliance with requirements from ECSS-Q-ST-70-12.

3 General Quality Assurance documents relating to the technology.

4 For each document referred in **Error! Reference source not found.**, **Error! Reference source not found.** this list will include: its precise title, its reference or number, its revision number and date.

<4> SECTION 4: Organisation

a. The PID shall contain the following information about Organisation:

1 Represented as a flow chart: organization of the company, organization of production department and organization of the quality Department.

2 Focal point and PID responsible,

3 Operators and inspectors certification methodology.

<5> SECTION 5: Manufacturing traveller or log file

a. The PID shall contain as a minimum the following information about the Manufacturing traveller or log file:

1 The sequencing of the various operations in their logical order of execution,

2 The references of the documents referred to and used during these operations,

3 The references of the Quality documents to ensure traceability of the various batches of material used (record reference), together with the work stations and tools employed,

4 The signatures of the various actors with the date on which the task was completed.

<6> Section 6: List of verified technology

a. The PID shall contain as a minimum the following information about the List of verified technology:

1 List of materials,

2 Temperature and time profiles for the machine reflow used in the verification,

3 List of verified devices per assembly configuration,

4 List of sensitive devices,

5 List of devices with limited project verification.

<7> SECTION 7: Description of production line

a. The PID shall contain as a minimum the following about the Description of production line:

1 Layout of premises with associated surface area, with indication of location of production machines and quality inspection,

2 Working environment; cleanliness class, ambient temperature limits, humidity and positive pressure limits for each type of activities.

<8> SECTION 8: List of equipment

a. The supplier shall identify a list of all machines and tools utilised during the SMT activity.

<9> SECTION 9: List of laboratory services

a. The supplier shall identify range and capability of supporting laboratory services.

<10> SECTION 10: Project SMT heritage

a. The supplier shall list heritage of board SMT assembly by year manufactured in accordance with the PID.

F.2.2 Special remarks

None.

Annex G (normative) Verification approval procedure - DRD

G.1 DRD identification

G.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-38, requirement 14.1a.

G.1.2 Purpose and objective

The Verification approval procedure defines what the supplier has to put in to place to engage with the approval authority prior to undertake any activity to verify his SMT capability. It also identifies key aspects and controls necessary for verification to be achieved.

G.2 Expected response

G.2.1 Scope and content

<1> Methodology of approval

<1.1> Request for verification

a. Each supplier should assign a contact person to be the single point contact for all SMT matters.

b. The following items shall be submitted to the approval authority:

1. A letter from the supplier signed by the contact person and the quality assurance organization of the supplier addressed to the approval authority, describing his experience in SMT and making the request for verification.

2. One technology-sample of SMT taken from the assembly line, to be verified, not carrying conformal coating for the approval authority to inspect.

   NOTE Conformal coating to be omitted to enable detailed inspection to be undertaken by approval authority.

<2> Technology sample

a. The technology sample shall be inspected by the approval authority in accordance with the requirements from clause 13.

b. The qualifying authority may waive the need for technology sample.

<3> Audit of assembly processing

a. The approval authority shall inform the supplier on the result of inspection of a technology sample specified in the requirement G.2.1<2>a.

b. The approval authority shall inform the supplier on acceptance regarding the start of the next stages of the approval process.

c. The audit of the supplier's assembly line shall be performed prior to verification programme.

NOTE Guidelines to audit report is given in Annex D.

d. The findings of the audit shall remain confidential between approval authority and the supplier.

<4> Verification programme

a. A verification programme shall be submitted to the approval authority for acceptance prior to the start of assembly of the test SMT in accordance with DRD from Annex H.

<5> Final Verification Review

a. The verification test report shall contain the following information:

1 Applicable documents for verification

2 Manufacturing traveller including devices traceability

3 Vibration profile and responses

4 Shock input if applicable

5 Thermal cycle

6 Visual inspection and MIP reports

7 Microsection

8 Nonconformances reports.

b. The verification test report shall be made available to the approval authority.

c. Following the completion of the final verification review, the PID shall be approved and summary tables agreed.

G.2.2 Special remarks

None.

Annex H (normative) Verification programme - DRD

H.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-38, requirement 14.1a.

H.1.1 Purpose and objective

The purpose of the Verification programme DRD is to detail the requirements of the verification programme.

H.2 Expected response

H.2.1 Scope and content

<1> General

a. The verification programme shall contain as a minimum the following:

1. Indication of method of the assembly
2. PCB information
3. Materials used
4. List of devices
5. Environmental test conditions and facility
6. Verification method Microsection or Electrical monitoring
7. Microsection laboratory
8. PID and Manufacturing document process references
9. Verification by similarity
10. Certification status of the operators and inspectors
11. Compliance status of the operators and inspectors
12. Compliance of the manufacturing room
13. Additional information.

b. The content may be tailored for companies having already an ECSS SMT approval.

c. Any nonconformances or major changes with reference to the verification plan shall be notified to the approval authority within one week.

H.2.2 Detailed requirement for Verification programme

<1> Indication of the method of assembly

a. The soldering method and repair methods shall be identified.

NOTE When machine reflow is used then the verified hand soldering or other method is used.

<2> PCB information

a. PCB information shall include:

1 PCB material and manufacturer

2 PCB pad surface finish

3 Number of layers

4 Thickness

5 Built up with identification of signal and full copper plane

6 Connection of the pads to the internal layer representative of the flight hardware

7 Location of the devices on the PCB

8 Location of the mechanical fixation or stiffeners if any.

9 Number of PCB used for the verification programme.

<3> Materials used

a. The supplier shall identify materials to be used:

1 Solder paste and wire designation, commercial trade mark, and composition with associated flux class

2 Flux class used for pretinning and soldering

3 Conformal coating

4 Adhesive for mechanical, and for thermal

5 Solvent

6 Others.

<4> List of devices

a. The devices used for the verification shall be in compliance with list of devices from the Table I-1.

NOTE It is under the responsibility of the company to ensure that the soldering method and temperature is compliant with the manufacturer datasheet and or technical notes.

b. The devices assembled by machine reflow shall not be reworked.

c. Reworking shall be decided during the MIP1 referenced below.

<5> Environmental test conditions

a. The environmental conditions of the mission including ground testing shall be reviewed to ensure the verification programme envelops the mission conditions.

b. Supplier shall ensure that the conditions associated with long term storage, extensive ground testing, mechanical stress after launch, high temperature application with or without thermal cycles are assessed.

c. Compliance from -55 °C to +85 °C for mission shall be stated.

d. The levels and duration of the vibration shall be provided.

NOTE It is the responsibility of the contractor to ensure that the levels applied are sufficient to cover the mission.

e. The levels and duration of the shock shall be provided.

f. The mounting configuration of the PCB for the vibration tests shall be identified.

g. The PCB shall be mounted such that the deflection and acceleration is representative of the flight hardware.

h. The accelerometers shall be placed on the PCB as well as on the base plate in order to determine the acceleration of the PCB.

<6> Microsections

a. The microsections shall be performed at the completion of the environmental test and in compliance with the requirements from clause 14.7.

<7> Verification work flow

a. The supplier shall organise a Verification review (VR) with the approval authority.

b. During the VR the PCB design shall be reviewed to ensure compliance with clause from **Error! Reference source not found.**

c. Prior to start of verification assembly the supplier shall organise a Manufacturing readiness review (MRR) with the approval authority.

NOTE During the review the approval authority can check that the verification programme is approved by all parties and that all open actions are closed.

d. The supplier shall organise a Mandatory inspection point (MIP1) with the approval authority prior to any conformal coating with five days notification.

NOTE The approval authority can delegate the MIP1 to the supplier.

e. Prior to any environmental testing the supplier shall organise with the approval authority an action review during which the MIP and outstanding actions are reviewed, with five days notification.

NOTE The approval authority can delegate the action review to the supplier.

f. The supplier shall organise with approval authority a Mandatory Inspection Point (MIP2) at the completion of the environmental test with five days notification.

NOTE The approval authority can delegate the MIP2 to the supplier.

g. The supplier shall organize with the approval authority a Test review board (TRB) during which the environmental tests results are reviewed.

NOTE The approval authority may delegate the TRB to the supplier.

h. The supplier shall organise with the approval authority a final verification review in conformance with Annex F.

NOTE The Assembly processes can be reviewed during the meeting in order to have the PID issued. Verification of closure of the actions identified during the audit of the manufacturing line.

<8> NCRs

a. Any NCRs related to the assembly shall be reported to the approval authority.

b. NRBs shall be organised by the supplier.

<9> Training and Certification status of the operators and inspectors

a. The compliance with this standard shall be identified.

<10> Compliance of the manufacturing room

a. The compliance with the ECSS-Q-ST-70-08 shall be identified.

<11> Additional information

a. The schedule of the verification activities shall be provided and maintained.

H.2.3 Special remarks

None.

Annex I (normative) SMT summary tables - DRD

I.1 DRD identification

I.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-38, requirement 14.1b and 14.1e.

I.1.2 Purpose and objective

The purpose of the summary table is to consolidate the approval status of the boundary conditions for the verification activity.

I.2 Expected response

I.2.1 Scope and content

a. The summary table shall include the following data

1. Assembly processes
2. PID reference with issue
3. Solder type: For machine reflow and for hand assembly
4. Conformal coating
5. Substrate type: Polyimide
6. Device data as shown in Table I-1.

NOTE Examples of assembly processes are VP and hand soldering or convection reflow + hand soldering or hand soldering.

I.2.2 Special remarks

None.

Table I-1: Device type preparation and mounting configuration

Device family	**Package**	**Manufacturer**	**Package dimensions**	**Bonding material (under device)**	**Staking material (edge or corner)**	**Terminal material**	**Lead finish**	**Pitch (mm)**	**Nominal Terminal thickness (mm)/ Nominal width**	**In-House degolding / pretinning**	**In-house lead forming Yes/No/NA**	**Artificial stand off Yes/No**	**Final report**
Ceramic chip	C0603 Type 1		Length, width	NA	NA		Sn/Pb	NA	NA	No	N/A	No	
Ceramic	C0603 Type 11										N/A		
Ceramic resistor	R0805			NA	NA		Sn/Pb	NA	NA	No	N/A	No	
Diode	D5-B										N/A		
Tantalum capacitors													
IC	FP10 Bottom brazed.			yes	One the side	Alloy42	Gold	1,27	0,25	yes	yes	NA	
CQFP	CQFP196 top brazed					Kovar					No		

Bibliography

[1] *ESA STM-261*, An Investigation into Ball Grid Array Inspection Techniques.

[2] *ESA STM-265*, Evaluation of Thermally Conductive Staking Compounds during the Assembly of Spacecraft Electronics.

[3] *ESA SP-1173*, Evaluation of Conformal Coating for Future Spacecraft Applications.

[4] *ESA STM-266*, Assessment of the Reliability of Solder Joints to Ball and Column Array Packages for Space Applications

[5] *IPC-7095*, Design and Assembly Process Implementation for BGAs, IPC, August 2000.

[6] *P.-E. Tegehall and B. D. Dunn*, Impact of Cracking Beneath Solder Pads in Printed Board Laminate on Reliability of Solder Joints to Ceramic Ball Grid Array Packages, ESA STM-267, ESA Publications Division, Noordwijk, 2003.

[7] *P.-E. Tegehall And B.D Dunn*, Assessment of the Reliability of Solder Joints to Ball And Column Grid Array Packages for Space Applications, ESA STM-266, ESA Publications Divisions, Noordwijk, 2003.

[8] *P. Wood and H. Rupprecht*, BGA and CSP Rework: What is involved? K. Gilleo (Ed.) Area Array Packaging Handbook, McGraw-Hill, Inc., 2001, Chapter 19.

[9] *M. Wickham, C. Hunt, D.M. Adams and B.D. Dunn*, An Investigation into Ball Grid Array Inspection Techniques, ESA STM-261, ESA Publications Divisions, Noordwijk, 1999.

[10] *ECSS-E-ST-10-03*, Space engineering — Testing.

[11] *ECSS-Q-ST-70-22*, Space product assurance — Control of limited shelf-life materials.

[12] *ECSS-Q-ST-70-28*, Space product assurance — Repair and modification of printed circuit board assemblies for space use.

[13] *ISO 9453*, Soft solder alloys - Chemical compositions and forms