ECSS-Q-ST-70-60C DIR 1
30 June 2017

Space product assurance

Qualification and procurement of printed circuit boards

This draft is circulated to the ECSS community for Public Review.

Start of Public Review: 30 June 2017
End of Public Review: 29 September 2017

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Foreword

This Standard is one of the series of ECSS Standards intended to be applied together for the management, engineering and product assurance in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards. Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

This Standard has been prepared by the ECSS Executive Secretariat, endorsed by the Document and Discipline Focal Points, and approved by the ECSS Technical Authority.

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Published by: ESA Requirements and Standards Division
ESTEC, P.O. Box 299,
2200 AG Noordwijk
The Netherlands

Change log

ECSS-Q-70-10A ECSS-Q-70-11A 23 November 2001	First issue
ECSS-Q-70-10B ECSS-Q-70-11B	Never issued
ECSS-Q-ST-70-10C ECSS-Q-ST-70-11C 15 November 2008	Second issue Redrafting according to ECSS drafting rules and template. Reorganization of the content to separate descriptive text and requirements and creation of DRD.
ECSS-Q-ST-70-60C DIR 1 30 June 2017	First issue Revision and merging of ECSS-Q-ST-70-10C and ECSS-Q-ST-70-11C

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Introduction

PCBs are used for the mounting of electronic components to produce PCB assemblies that perform electrical functions. The PCBs are subjected to thermo-mechanical stress during assembly such as soldering of components, rework and repair under normal terrestrial conditions. In addition, the assembled PCBs are exposed to the launch and space environment. The reliability of the circuit depends on the robustness of the manufacturing processes, for which this standard specifies requirements. PCB technology needs detailed inspections to verify its reliability, which is specified by at qualification and procurement phases of the PCB technology.

1
Scope

This standard specifies the requirements for the PCB manufacturer, the procurement authority and the qualification authority for qualification and procurement of PCB technology.

ECSS-Q-ST-70-60 is applicable for all types of PCBs, including sequential, rigid and flexible PCBs, sculptured flex, HDI and RF PCBs.

This standard can be made applicable for other products combining mechanical and electrical functionality using additive or reductive manufacturing processes, as used in PCB manufacturing. Examples of such products are slip-rings, bus bars and flexible flat cables.

This standard may be tailored for the specific characteristics and constraints of a space project in conformance with ECSS-S-ST-00.

2
Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revision of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the more recent editions of the normative documents indicated below. For undated references, the latest edition of the publication referred to applies.

ECSS-S-ST-00-01	ECSS system — Glossary of terms
ECSS-Q-ST-10-09	Space product assurance — Nonconformance control system
ECSS-Q-ST-20	Space product assurance — Quality assurance
ECSS-Q-ST-70	Space product assurance — Material, mechanical parts and processes
ECSS-Q-ST-70-02	Space product assurance — Thermal vacuum outgassing test for the screening of space materials
ECSS-Q-ST-70-08	Space product assurance — Manual soldering of high-reliability electrical connections
ECSS-Q-ST-70-12	Space product assurance — Design rules for printed circuit boards
ECSS-Q-ST-70-21	Space product assurance — Flammability testing for the screening of space materials
ECSS-Q-ST-70-22	Space product assurance — Control of limited shelf-life materials
ECSS-Q-ST-70-29	Space product assurance — Determination of offgassing products from materials and assembled articles to be used in a manned space vehicle crew compartment
IEC 60326-2-am 1 (1992-06)	Printed boards. Part 2: Test methods
IEC 60194 (1999-04)	Printed board design, manufacture and assembly — Terms and definitions
IPC-A-600J (2016)	Acceptability of Printed Boards
IPC-T-50M (2015)	Terms and definitions for interconnecting and packaging electronic circuits

IPC-TM-650	Test methods manual
IPC-1710A (2004)	OEM Standard for Printed Board Manufacturers' Qualification Profile
IPC-4101E (2017)	Specification for base materials for rigid and multilayer printed boards
IPC-4103A-WAM1 (2014)	Specification for Base Materials for High Speed/ High Frequency Applications
IPC-4203A (2013)	Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Circuitry and Flexible Adhesive Bonding Films
IPC-4204A-WAM1 (2014)	Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Circuitry
IPC-6012D (2015)	Qualification and performance specification for rigid printed boards
IPC-6012DS (2015)	Space and military avionics applications addendum to IPC-6012D
IPC-6013C (2013)	Qualification and Performance Specification for Flexible Printed Boards
IPC-6018C (2016)	Qualification and Performance Specification for High Frequency (Microwave) Printed Boards
IPC-6018CS (2016)	Space and Military Avionics Applications Addendum to IPC-6018C

3
Terms, definitions and abbreviated terms

3.1 Terms from other standards

a. For the purpose of this Standard, the terms and definitions from ECSS-S-ST-00-01 apply, and in particular the following terms:

1. customer
2. supplier

NOTE See clause 4.2 for a description of roles of customer and supplier.

b. For the purpose of this Standard, the terms and definitions from ECSS-Q-ST-70-12 apply, and in particular the following terms:

1. annular ring
2. area array device (AAD)
3. aspect ratio
4. basic copper
5. blind via
6. bond ply
7. build-up
8. buried via
9. conductor
10. FR4
11. hole wall pull away
12. heat sink
13. high density interconnect (HDI)
14. interlayer
15. intralayer
16. laminate
17. microvia
18. no-flow prepreg
19. non-functional pad

20. non-pated hole
21. normal pitch
22. panel
23. plated through-hole (PTH)
24. prepreg
25. printed circuit board (PCB)
26. resin starvation
27. serialization
28. spacing
29. stack
30. track
31. via
32. X,Y direction
33. Z direction

3.2 Terms specific to the present standard

3.2.1 automated optical inspection (AOI)

inspection method using an automated equipment to verify the pattern on an etched layer

3.2.2 back-drilled via

type of via with part of its metallisation removed on one side by depth controlled mechanical drilling with a larger diameter drill

3.2.3 batch

group of PCBs and coupons that are covered by the same CoC and the same traveller

NOTE 1 A batch is processed approximately at the same time. See 6.7a.

NOTE 2 The terms “lot” and “work order” are synonymous.

3.2.4 blister

delamination in the form of a localized swelling and separation between any of the layers of a laminated base material, or between base material and conductive foil or protective coating

[IPC-T-50M]

3.2.5 cap lift

separation between resin in blind via and copper cap plating on surface

NOTE Cap lift can be shown as bulging and as thin line separation, as shown in Table 10-18.

3.2.6 contamination

<CONTEXT: Qualification and procurement of PCBs>

foreign material embedded in dielectric material

NOTE 1 Synonyms are: FOD, inclusion, foreign material, debris, pollution.

NOTE 2 Contamination can be organic, metallic, particulate or fibres.

3.2.7 coupon

small piece of test circuitry that is used for quality conformance evaluation by specific tests and inspection

NOTE 1 The coupon is manufactured as part of a panel and at the final manufacturing stage it is separated from it. The coupon is thus associated with the PCBs within the panel, with which it was simultaneously manufactured.

NOTE 2 The term 'coupon' refers to a generic pattern, whereas the term 'IST coupon' refers to the specific IST pattern.

[adapted from IPC-T-50M]

3.2.8 coverlay

thin dielectric material used to encapsulate circuitry, most commonly for flexible circuit applications

NOTE The terms 'cover layer' and 'cover material' are synonymous.

3.2.9 crazing

condition that occurs in reinforced laminate base material whereby glass fibre bundles are separated from the resin not limited to the weave intersections

NOTE 1 This condition manifests itself in the form of connected white spots or crosses that are below the surface of the base material. It is usually related to thermally or mechanically induced stress. Crazing is a more severe defect than measling. Delamination is a further worsening of crazing.

NOTE 2 See also "measling".

3.2.10 delamination

separation between plies within a base material, between base material and a conductive foil, or any other planar separation with a PCB

NOTE See also 'blister', which is a local delamination.

[IPC-T-50M]

3.2.11 destructive physical analysis (DPA)

analysis method using sampling, potting, grinding, polishing and inspection which, thus, destroys the test vehicle

NOTE The term 'microsectioning' is approximately synonymous.

3.2.12 dewetting

condition that results when molten solder coats a surface and then recedes to leave irregularly-shaped mounds of solder that are separated by areas that are covered with a thin film of solder and with the base metal not exposed

[IPC-T-50M]

3.2.13 dross

oxide and other contaminants that form on the surface of molten solder

[IPC-T-50M]

3.2.14 etchback

distance from resin of hole wall to innerlayer foil

3.2.15 fine pitch

spacing of tracks or pads that is more dense than for normal pitch

NOTE Pitch is specified in clause 7.4 of ECSS-Q-ST-70-12.

3.2.16 flexible

PCB technology that uses only flexible layers in its build up

NOTE The term 'flex' is synonymous.

3.2.17 glass compression

deformed glass fibre bundles of prepreg causing absence of resin between glass and copper due to profiled copper pattern

NOTE See also 'resin starvation'.

3.2.18 haloing

mechanically-induced fracturing or delamination, on or below the surface of a base material, that is usually exhibited by a light area around holes or other machined features

[IPC-T-50M]

3.2.19 inclusion

foreign particle, metallic or non-metallic, that can be entrapped in an insulating material, conductive layer, plating, base material or solder connection

[IPC-T-50M]

3.2.20 interconnect defect (ICD)

separation at the interface between internal layer and through-hole plating

NOTE 1 The term 'innerlayer separation' is synonymous.

NOTE 2 See 'smear' for additional explanation.

[IPC-6012D]

3.2.21 interconnect stress test (IST)

test method using a specific IST coupon and a specific IST equipment

3.2.22 IST coupon

specific coupon for IST

NOTE The term 'coupon' refers to a generic pattern, whereas the term 'IST coupon' refers to the specific IST pattern.

3.2.23 key personnel

personnel with specialist knowledge responsible for defined production or product assurance areas

3.2.24 lay-out

design of the conductive pattern on a layer

3.2.25 measling

condition that occurs in laminated base material whereby glass fibre bundles are separated from the resin limited to the weave intersection

NOTE 1 This condition manifests itself in the form of discrete white spots or "crosses" that are below the surface of the base material. It is usually related to thermally-induced stress or humidity.

NOTE 2 See also "crazing", which is a further worsening of measling.

[IPC-T-50M]

3.2.26 metal core

layer or local insert of thick metal embedded inside the PCB usually used as a heat sink, grounding layer or restriction of thermal expansion

3.2.27 milling

mechanical method that removes a portion of the material outlining a PCB using a cutting bit

NOTE See also 'routing'.

3.2.28 multilayer

PCB technology that uses lamination of several copper layers and plated holes for interconnection

NOTE PCBs that are not multilayer, are double-sided or single-sided PCBs. See also "sequential".

3.2.29 plated hole

hole that is used as an interlayer connection

NOTE Types of plated holes are PTH and vias.

3.2.30 PCB manufacturer

entity that manufactures the PCB

NOTE The PCB manufacturer is supplier to the procurement authority.

3.2.31 PCB technology

category of manufacturing processes, materials and design for PCBs

NOTE Examples of PCB technology are:

- Polyimide sequential rigid
- Polyimide sequential rigid/flex
- Epoxy sequential rigid
- Epoxy non-sequential rigid/flex
- HDI with microvias
- RF
- Flexible and sculptured flex

3.2.32 procurement authority

entity that procures the PCB

NOTE 1 The procurement authority is customer of the PCB manufacturer.

NOTE 2 The procurement authority can be supplier to the prime contractor.

3.2.33 qualification authority

entity that qualifies the PCB technology and PCB manufacturer

3.2.34 radio frequency (RF)

electronic functionality that requires specific design precautions on dielectric materials and copper pattern to maintain time dependant signal integrity

NOTE 1 The term 'high speed' is synonymous.

NOTE 2 The term 'RF PCB' identifies the PCB technology.

3.2.35 rigid

PCB technology that uses only rigid layers in its build-up

3.2.36 rigid/flex

PCB technology that uses a combination of rigid and flexible layers in its build-up

3.2.37 routing

the lay-out and connection of conductors between plated-holes and pads

NOTE The term 'routing' is also used for 'milling'. This second meaning is not used in ECSS-Q-ST-70-60 to avoid confusion.

3.2.38 scratch

narrow furrow or grove in a surface

NOTE It is usually shallow and caused by the marking or rasping of the surface with a pointed or sharp object.

[IEC 60194 (1999-04)]

3.2.39 sculptured flex

flexible PCB technology that uses profiled copper tracks

NOTE Aviflex is a commercial identification of sculptured flex.

3.2.40 sequential

PCB technology that uses more than one lamination or drilling step

NOTE The term 'sequential' also implies that the PCB is of type 'multilayer'. The opposite is 'non-sequential'.

3.2.41 sequential via

via type that interconnects layers within the same plating sequence

NOTE Examples of sequential vias are blind vias and buried vias.

3.2.42 skip plating

local missing deposition of plating

NOTE Skip plating can occur on electroless copper plating on glass in the hole wall. Skip plating can also occur on surface finish.

3.2.43 smear

base material resin that covers the interface between the exposed edge of an innerlayer pad and through-hole plating

NOTE 1 The resin transfer is usually caused by the drilling operation and removed during the desmear process. The term 'resin smear' or 'smearing' are synonymous.

NOTE 2 The aspect of smear can be mistaken for interconnect defect, or vice versa. Smear is the presence of resin, whereas interconnect defect is an adhesive separation of copper plating.

[adapted from IPC-T-50M]

3.2.44 test pattern

part of the PCB or coupon that refers to the copper pattern for a specific test

[adapted from IPC-T-50M]

3.2.45 traveller

documentation kept with the batch during the manufacturing processes in which the order of specific processes are recorded

3.2.46 through-going via

type of via that is drilled through the entire thickness of the PCB

3.2.47 via-in-pad

type of via directly underneath a SMT pad

3.2.48 waiver request

written agreement between PCB manufacturer and procurement authority to deliver PCBs with a non-conformance to a requirement from a specification

NOTE 1 The following terms are synonymous: “request for concession”, “demande de derogation”, “request for waiver”, “request for deviation”.

NOTE 2 In space projects the terms RFW and RFD have specific meaning as specified in ECSS-Q-ST-70. This specific meaning does not strictly apply in the context of PCB procurement.

3.2.49 weave exposure

a base material surface condition in which unbroken fibres of woven glass are not completely covered by resin

NOTE See also ‘weave texture’.

[IPC-T-50M]

3.2.50 weave texture

a surface condition of base material in which a weave pattern of cloth is apparent although the unbroken fibres of woven cloth are completely covered by resin.

NOTE See also ‘weave exposure’.

[IPC-T-50M]

3.2.51 wicking

infiltration of copper plating into the dielectric of the hole wall

NOTE The terms "copper infiltration" and "copper ingress" are synonymous.

3.2.52 work instruction

quality document that describes the technical details about processes, material usage, inspection and acceptance criteria

NOTE 1 The terms 'manufacturing procedure' or 'control procedure' or 'process instruction' are synonymous.

NOTE 2 Work instructions can include process flow charts, production documents (e.g. manufacturing plans, travelers, routers, work orders, process cards) and inspection documents.

3.3 Abbreviated terms

For the purpose of , the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
AAD	area array device
AC	alternating current
AOI	automated optical inspection
AR	as received
CDR	critical design review
CIC	copper-invar-copper
CoC	certificate of conformance
CTE	coefficient of thermal expansion
Cu	copper (element)
CVCM	collected volatile condensable material
DC	direct current
DML	declared materials list
DPA	destructive physical analysis
DR	design review
DRB	delivery review board
DRD	document requirements definition
DSC	differential scanning calorimetry
DWV	dielectric withstanding voltage
EBB	elegant breadboard

Abbreviation	Meaning
ECM	electrochemical migration
EM	engineering model
EOL	end of life
EQM	engineering qualification model
FAI	first article inspection
FCSI	final customer source inspection
FM	flight model
FOD	foreign article debris
FR4	type of epoxy resin for PCBs
FS	flight spare
HDI	high density interconnect
ICD	interconnect defect
IMC	intermetallic compound
IPA	isopropanol
IPC	association connecting electronic industries
IST	interconnect stress test
KPI	key performance indicator
max	maximum
min	minimum
MIP	mandatory inspection point?
MPCB	material and processes control board
MRR	manufacturing readiness review
n. a.	not applicable
NCR	nonconformance report
NRB	nonconformance review board
OTD	on time delivery
PCB	printed circuit board
PCN	process change notice
PDR	preliminary design review
PFM	proto flight model
PID	process identification document
PTH	plated-through hole
PTFE	polytetrafluoroethylene
QA	quality assurance
QM	qualification model
QML	qualified manufacturers list
QPL	qualified product list
r. m. s.	root-mean-square

Abbreviation	Meaning
R&D	research and development
Ref	reference (for tables in clause 10)
RF	radio frequency
RFA	request for approval
RML	residual mass loss
RW	rework simulation
SB	solder bath float
SMT	surface mount technology
SPC	statistical process control
sq	square (in unit Ω/sq)
TBD	to be defined
TDR	time domain reflectometry
T288	time to delamination at 288°C
Td	temperature of decomposition
Tg	temperature of glass transition
TGA	thermogravimetric analysis
TMA	thermomechanical analysis
wk	week

3.4 Nomenclature

The following nomenclature applies throughout this document:

a. The word "shall" is used in this Standard to express requirements. All the requirements are expressed with the word "shall".

b. The word "should" is used in this Standard to express recommendations. All the recommendations are expressed with the word "should".

NOTE It is expected that, during tailoring, recommendations in this document are either converted into requirements or tailored out.

c. The words "may" and "need not" are used in this Standard to express positive and negative permissions, respectively. All the positive permissions are expressed with the word "may". All the negative permissions are expressed with the words "need not".

d. The word "can" is used in this Standard to express capabilities or possibilities, and therefore, if not accompanied by one of the previous words, it implies descriptive text.

NOTE In ECSS "may" and "can" have completely different meanings: "may" is normative (permission), and "can" is descriptive.

e. The present and past tenses are used in this Standard to express statements of fact, and therefore they imply descriptive text.

4
Principles

4.1 General

This standard specifies requirements for the manufacture, qualification, procurement, test and inspection of PCBs.

4.2 Roles

In the context of ECSS-Q-ST-70-60 the roles “PCB manufacturer”, “procurement authority” and “qualification authority” were explicitly introduced and defined in clause 3.2 to allow proper allocation of requirements.

4.3 List of conditions

The formulation ”in case the following conditions are met” indicates that all of the listed conditions are met, except when it is stated that only one or some of the conditions can be met.

4.4 References to acceptance criteria

Clause 10 includes tables to specify acceptance criteria for certain technological features. The technological features can be further subdivided in each table. This is indicated with a reference letter in the first column and abbreviated as “Ref x”. This allows cross referencing to specific line items in the table, rather than to an entire table. An example of this is “internal annular ring on an inner layer at the end of a blind via” which is cross referenced as Ref b in Table 10-1.

5
QA for qualification

5.1 Qualified PCBs

a. Qualified PCBs for space applications shall meet the following conditions:

1. the PCB is procured in conformance with clauses 6 and 8,
2. the PCB is procured from a PCB manufacturer that is qualified in conformance with clauses 5 and 7 and as specified in the PID,
3. the PCB design is in conformance with the requirements of ECSS-Q-ST-70-12.

NOTE Some specific PCB technologies can be used that are not covered by a valid PID or by a company qualification. Procurement can be done under RFA, including tests for (delta) qualification and tests for procurement but it can exclude the qualification of the company. Examples of specific PCB technology are complex HDI, complex RF and flex technology that are under development. This is described in clauses 5.2 and 7.7.

b. The qualification of PCBs in conformance with this standard shall cover for a maximum operational temperature of 85 °C.

NOTE 1 This is also described in clause 1 "Scope" of ECSS-Q-ST-70-08 and clause 1 "Scope" of ECSS-Q-ST-70-38.

NOTE 2 This is in conformance with current rating requirements from clause 13.6.2 of ECSS-Q-ST-70-12.

NOTE 3 PCBs are not qualified for a specific voltage as this is depending on PCB design in conformance with ECSS-Q-ST-70-12.

5.2 Special PCB technology

a. PCBs manufactured using conventional PCB processes and ceramic filled laminate shall be in conformance with ECSS-Q-ST-70-60.

NOTE This is opposed to ceramic substrates using thick film or thin film processes that conform to ESCC-2566000.

b. Flexible flat cables manufactured using conventional PCB processes shall be in conformance with ECSS-Q-ST-70-60.

NOTE 1 This is opposed to heaters that conform to ESCC-4009 or cables that conform to ESCC-3901.

NOTE 2 This technology can also be called "flexprint" or "ribbon flex".

NOTE 3 Conventional PCB processes include etching of copper clad flexible laminate and lamination of coverlay, among others. Encapsulation of separate copper strings or wires to form a flexible ribbon is not a conventional PCB process.

5.3 Qualification process

a. The process for PCB qualification shall contain the following stages:

1. request for qualification and associated documentation in conformance with clause 5.4,
2. evaluation of a technology sample in conformance with clause 5.7,
3. audit of the manufacturing facility in conformance with clause 5.8,
4. qualification programme in conformance with clause 5.9.

b. The approval from the qualification authority of the completed qualification shall be in conformance with clause 5.11.

5.4 Request for qualification

a. The PCB manufacturer shall send a formal request for qualification to the qualification authority.

b. The PCB manufacturer shall provide the company profile including the following information:

1. description of the manufacturer capabilities,
2. business plan with basic financial figures for sales and R&D

NOTE The business plan demonstrates a healthy economical business and a strong commitment to quality assurance for space products.

c. The PCB manufacturer shall demonstrate the heritage on the PCB technologies for which qualification is requested, by providing the types of technology and quantity of PCBs produced for non-space customers, industrial space customers and space agencies.

NOTE This is in particular important for the approved surface finishes, such as hot oil reflowed tin-lead.

d. The PCB manufacturer shall provide a letter of support from the main industrial space customers.

e. The PCB manufacturer shall provide a preliminary strategic planning, indicating the following:

1. the space projects for which qualified PCBs are foreseen to be provided,
2. which current customers can benefit from possible qualification,
3. which new customers or orders can be gained in case qualification is achieved,
4. what technologies are foreseen to qualify initially and in the medium and longer term,
5. the internal resource estimate for achieving qualification,
6. a target schedule for all activities related to achieving qualification.

f. The PCB manufacturer shall provide the completed survey for assessment of the PCB manufacturer's capabilities in conformance with IPC-1710.

g. The PCB manufacturer shall demonstrate that it meets the requirements for quality assurance in conformance with clause 5.5.

5.5 Quality standards

a. The quality assurance requirements specified in ECSS-Q-ST-20 shall apply.

b. The PCB manufacturer shall manage nonconformances in accordance with ECSS-Q-ST-10-09.

c. The PCB manufacturer shall hold certification for its quality management system in conformance with ISO-9001:2016 and EN9100:2017 or demonstrate that he has a quality management system in line with the above standards.

5.6 Description of qualification vehicle

a. The PCB manufacturer shall provide the PCB definition dossier, in conformance with the DRD in Annex A of ECSS-Q-ST-70-12, to the qualification authority for approval of the qualification vehicle.

b. The qualification vehicle shall be representative of the highest technological complexity for which qualification is requested.

c. The design of the qualification test vehicle shall accommodate the tests specified in clause 7.

NOTE Examples of test patterns are shown in IPC-2221B.

d. The design of the qualification vehicle shall be in conformance with requirements from ECSS-Q-ST-70-12.

e. The coupons that are included in the qualification vehicle shall be in conformance with the clauses 8.2.2 and 8.2.3.

f. Initial qualification of a PCB manufacturer or PCB technology in conformance with requirement 7.2a shall be performed on at least 3 PCBs and the coupons in conformance with Figure 7-1.

g. Initial qualification of a PCB manufacturer or PCB technology in conformance with requirement 7.2a should include a spare PCBs and spare coupons in conformance with Figure 7-1.

h. Delta qualification and qualification renewal in conformance with requirement 7.2 shall be performed on at least 1 PCB and associated coupons.

5.7 Evaluation

a. The requirements of clause 5.6 shall apply to the evaluation samples.

b. The submission of evaluation samples shall include PCB, coupons, microsections and documentation in conformance with requirement 5.14a.

c. A first set of evaluation samples should be evaluated by a third-party.

NOTE It is beneficial to request a third-party evaluation by a company with knowledge on evaluation in conformance with ECSS-Q-ST-70-60.

d. The test flow for evaluation shall be in conformance with requirements from clause 7.5.

NOTE 1 This test flow includes DPA of PCB and coupons and IST.

NOTE 2 The evaluation phase is intended as a relatively fast assessment of the quality to gain confidence in the product before initiating the full qualification programme.

e. The qualification authority shall perform the evaluation and issue the test report.

f. The qualification authority shall provide to the PCB manufacturer the authorization to proceed with the qualification in case the following conditions are met:

1. Evaluation is acceptable.

2. Assessment of the request for qualification, in conformance with the clause 5.4, is acceptable.

NOTE It is the intention to perform a PCB evaluation only once. In case the first attempt fails, a second final opportunity for passing the evaluation successfully can be offered. The qualification process can be discontinued in case the evaluation fails or in case the schedule as agreed in the strategic planning is exceeded.

5.8 Audit

a. The qualification authority shall audit the manufacturing line.

b. The audit shall occur when PCB production is in progress.

c. Before the audit, the PCB manufacturer shall make the following documents available to the qualification authority for review and approval:

   1. PID in conformance with the DRD in Annex D;

   2. Qualification test plan in conformance with clause 7.1 including test description, test vehicle and schedule.

d. The qualification authority shall submit to the PCB manufacturer an audit checklist that verifies the requirements from ECSS-Q-ST-70-60 and its normative references one month prior to the date of the audit.

e. The PCB manufacturer shall provide the response to the audit checklist to the qualification authority at least one week prior to the date of the audit.

f. The response from the PCB manufacturer in the audit checklist shall include the following:

   1. compliance level as follows:

      (a) “compliant” or

      (b) “non-compliant” or

      (c) "partial compliant” or

      (d) “not applicable”,

   2. a comment explaining any non-compliance, partial compliance or non-applicability,

   3. references to work instructions that specify the verified requirement.

g. During the audit, the PCB manufacturer shall make the following documents available to the qualification authority:

   1. Documented information in conformance with EN9100:2017 clause 4.2.2

   2. Business process procedures, in conformance with EN9100

   3. Work instructions, in conformance with EN9100.

      NOTE 1 Quality manual is one possible type of Documented information from 5.8g.1.

NOTE 2 See definition of work instructions in clause3.2.52.

h. In case of an audit for qualification renewal, the PCB manufacturer shall provide the following:

1. A collection of the QA reports in conformance with clause 5.13.

2. Lists of PCBs per PID supplied in conformance with ECSS-Q-ST-70-60 since the previous audit.

i. The qualification authority shall issue the audit report and any findings, in conformance with clause 5.8j.

NOTE The minutes of meeting can be the audit report.

j. Findings from the audit shall be categorised by the qualification authority as follows:

1. "Major non-conformance" is a non-conformance against ECSS-Q-ST-70-60 that is evaluated by the qualification authority as mandatory to disposition by a corrective action for successful audit closure.

2. "Minor non-conformance" is a non-conformance against ECSS-Q-ST-70-60 that is a longer term action for continuous improvement and therefore not preventing successful audit closure according to the qualification authority.

3. "Observation" is a recommendation or observation that does not prevent successful audit closure and that is not a non-conformance against ECSS-Q-ST-70-60.

k. The audit report and any findings shall be approved and signed by the PCB manufacturer and qualification authority.

l. Corrective actions from findings shall be added to the updated audit report or minutes of meeting of a delta audit.

m. The final conclusion of the audit process shall be provided in the final audit report or minutes of meeting.

5.9 Qualification test programme

a. The requirements of clause 5.6 shall apply to the qualification vehicle.

b. The PCB manufacturer shall perform the qualification tests as specified in the qualification test plan in conformance with requirement 7.2a and approved by the qualification authority in conformance with requirements 5.8c and 5.8k.

NOTE The PCB manufacturer can use labs from a third-party or from the customer to perform tests.

c. The PCB manufacturer shall issue the qualification test report in conformance with the DRD in Annex C.

d. The PCB manufacturer shall provide the qualification test report to the qualification authority for review and approval.

e. The qualification authority may request to the PCB manufacturer an additional test vehicle or microsections for evaluation.

5.10 PID

a. The PCB manufacturer shall issue the PID in conformance with the DRD of Annex D.

b. The specific parts of the PID shall be issued, in conformance with D.2.1.2, for the following PCB technologies in separate documents:

1. Polyimide rigid
2. Polyimide rigid/flex
3. Epoxy rigid
4. Epoxy rigid/flex
5. HDI
6. RF
7. Flexible
8. Sculptured flex

5.11 Qualification approval

a. Upon successful qualification, the qualification authority shall issue a qualification letter in conformance with the DRD in Annex A.

b. The qualification authority shall publish the qualification status.

c. The reason for a change or updated qualification status shall be published as a comment to the qualification status.

NOTE The term "qualified" can be used to indicate a valid qualification status. The term "not qualified" can be used to indicate an invalid qualification status, for instance as a result of nonconformances during qualification renewal or as a result of an expired qualification period. The status is not definite and can be updated when new results are available. A comment is included to clarify the reason for the qualification status. A definite disqualification or discontinuation of PCB technology or PCB manufacturer can be indicated by deletion from the published list or by the terms "disqualified" or "discontinued".

d. The qualification authority shall grant qualification approval to the PCB manufacturer based on the acceptance of the evaluation in conformance with clause 5.7, the audit in conformance with clause 5.8 and the qualification programme in conformance with clause 5.9.

e. The qualification approval shall be valid for a period of maximum two years.

f. In case nonconformances have been encountered, the qualification authority may grant a period of validity for the qualification that is shorter than two years.

NOTE One year is a commonly used qualification period to ensure a more frequent verification of the process control for a critical technology.

5.12 Process change

a. Process changes shall include process parameters, chemistry, material, equipment, process flow and inspections.

b. Process changes shall be categorised by the PCB manufacturer as “major” or “minor” in the PID.

c. Requests for major process changes shall be submitted to the qualification authority for approval.

d. The implementation of a major change shall be submitted to the qualification authority for approval.

e. Minor process changes may be implemented by the PCB manufacturer without prior approval of the qualification authority.

NOTE The PCN for a minor change includes the acceptable evaluation of the affected acceptance criteria in conformance with E.2.1b1.

f. For major and minor process changes, the PCB manufacturer shall issue a process change notice in conformance with the DRD in Annex E to the qualification authority.

g. All process change notices should be submitted to the procurement authority for information.

h. Major process change notices should be submitted to the procurement authority for approval.

5.13 QA report

a. The PCB manufacturer shall issue a QA report to the qualification authority in conformance with the DRD in Annex F.

b. The QA report shall be issued quarterly.

5.14 Qualification renewal

a. The PCB manufacturer shall submit to the qualification authority the following items for qualification renewal at least two months prior to expiration of the qualification:

1. A PCB from a normal production batch that is representative of the highest technological complexity that is qualified,
2. CoC in conformance with requirement 6.4b.1,
3. Coupons and microsections in conformance with clause 8.2,
4. The description, drawing and review items from the PCB definition dossier in conformance with clauses A.2.1<2> , A.2.1<4> A.2.1<6> of ECSS-Q-ST-70-12.
5. The PCB manufacturer's test report on a second identical PCB.

NOTE The coupons from 5.14a.3 include an IST coupon if this is specified for the technology in accordance with requirement 8.2.3a. The coupons from 5.14a.3 also include several coupons that are untested by the PCB manufacturer, in conformance with Table 8-2. It is important that these coupons are included, as it is common practice to perform, for instance, peel strength testing for qualification renewal.

b. In case requirement 5.14a is not achieved because the sample is sent late, the qualification status shall be "not qualified" after the expiration date until completion of qualification renewal, including a comment to the qualification status in conformance with the requirement 5.11c.

NOTE It is good practice that the PCB manufacturer sends the sample earlier than 2 months before expiration. If the PCB manufacturer sends multiple samples at the same time, it is good practice to allow for more than 2 months for evaluation.

c. The qualification authority shall issue a qualification renewal test report.

d. An audit of the PCB manufacturer shall be performed by the qualification authority at least every second year.

e. Upon successful qualification renewal, the qualification authority shall approve the qualification in conformance with the clause 5.11 and issue a new qualification letter in conformance with requirement 5.11a.

f. The qualification authority may decide to initiate a new qualification in the following cases:

1. the manufacturing was interrupted or qualification was expired for more than 2 years,
2. major changes in production line and its location.

5.15 Nonconformances during qualification renewal

a. In case nonconformances are observed during qualification renewal, the PCB manufacturer shall perform the following:

1. Investigate root cause, implement corrective actions on associated processes and materials, demonstrate repeatability,
2. Investigate why nonconformance was not detected by outgoing inspection and perform training,
3. Verify how the nonconformance affects the running orders and inform customers.
4. Evaluate a new PCB and provide test report in conformance with 5.14a.5.
5. Have a new PCB sample evaluated by a third-party lab and provide test report.
6. Upon approval from the qualification authority, submit a new sample for qualification renewal.

NOTE Third-party evaluation from requirement 5.15a.5 is also specified in requirement 5.7b.

b. In case the PCB manufacturer demonstrates that nonconformances observed during qualification renewal are of a one-time occurrence, the qualification authority should indicate for a maximum period of 6 months the qualification status as "qualified" with a comment to identify the failed and ongoing qualification renewal.

NOTE 1 A one-time occurrence of a nonconformance does not invalidate the qualification of other orders in case the efficiency of outgoing inspection has been scrutinized. A one-off nonconformance is relatively straightforward to correct for and the qualification renewal of a second sample is, therefore, done within the maximum period of 6 months.

NOTE 2 Since the PCB manufacturer re-submits the sample for qualification renewal 2 months prior to the expiration of the qualification status in conformance with requirement 5.14a, this provides him with 4 months to complete remanufacture of the sample, third-party evaluation and all other actions specified in 5.15a.

c. In case nonconformances are observed during qualification renewal, the qualification authority should indicate the qualification status as "not qualified" until acceptable completion of the qualification renewal, including a comment to the qualification status in conformance with the requirement 5.11c.

d. The qualification authority may withdraw the qualification in case:

1. Repeated nonconformances are observed during evaluation of a PCB during qualification renewal,
2. Repeated nonconformances are observed during audits,
3. Repeated nonconformances are observed with respect to the quality requirements from ECSS-Q-ST-70-60.

6
QA for manufacture and procurement

6.1 Overview

This clause describes requirements on quality assurance during the procurement and the manufacturing stages of the PCB.

6.2 Procurement process

6.2.1 Overview

This clause describes various steps in the procurement process of PCBs. This is followed by the manufacturing and inspection. Table 6-1 provides an estimation of typical lead time for the various phases for a typical batch size.

Table 6-1: Example of lead time for various phases of PCB procurement, manufacture, test and inspection.

	Rigid non sequential	Rigid sequential	Flex rigid	HDI
Tooling including design review and MRR	2-3 wk	2-3 wk	2-3 wk	2-3 wk
IST coupon design data	2 wk	2 wk	2 wk	2 wk
MRR approval	0.5-1 wk	0.5-1 wk	0.5-1 wk	0.5-1 wk
Manufacturing & inspection	4 wk	5-6 wk	5-6 wk	6-7 wk
IST	2.5-4 wk	2.5-4 wk	2.5-4 wk	2.5-4 wk
Total	11-14 wk	12-16 wk	12-16 wk	13-17 wk

6.2.2 Procurement specification

a. ECSS-Q-ST-70-60 shall be used as the PCB procurement specification.

NOTE It is not good practice that the procurement authority issues his own procurement specification in which he refers to ECSS-Q-ST-70-60 as an applicable or a reference document. A reason for this is because traceability of compliance to ECSS-Q-ST-70-60 can be lost. Another reason for this is because the PCB manufacturer issues its CoC against the procurement standard and he categorises his KPIs according to the used procurement standard. In case the procurement authority desires specific additional requirements that are not covered by ECSS-Q-ST-70-60, it is good practice to include these in the PCB definition dossier or in the purchase order.

6.2.3 Quotation

a. The procurement authority shall start the procurement process by requesting the quotation and lead time from the PCB manufacturer for tooling, production and test of a specified quantity based on the provided PCB definition dossier.

NOTE The provided PCB definition dossier can be in a draft form, as specified in requirement 5.2.e of ECSS-Q-ST-70-12.

b. The procurement authority shall maintain the PCB definition dossier under configuration control.

c. The procurement authority should specify in the PCB definition dossier the reporting of work in progress, content and frequency.

d. The procurement authority shall record double insulation in the PCB definition dossier.

NOTE Double insulation is specified for critical nets in conformance with requirement 13.9.2.a from ECSS-Q-ST-70-12.

e. The presence of blind-via-in-pad for soldering shall be recorded in the PCB definition dossier.

NOTE This can be done by a tick box.

f. In case the procurement authority does not define the tolerances in the PCB definition dossier, the following tolerances shall be used:

1. external dimension: ± 0,2 mm,
2. thickness over dielectric: ± 10 %,
3. diameter of all hole types: ± 0,1 mm,
4. external dimension for flex PCB: ± 0,4 mm;

5. thickness for flex PCB: ± 20 %;
6. clearance in coverlay for flex PCB: ±0 ,50 mm;

NOTE Tolerance of ±0,1mm on hole diameter is equal to Δ maximum of 0.2mm.

6.2.4 Purchase order

a. The procurement authority shall issue the purchase order including the reference to the quotation, the ordered quantity of PCBs, the contact persons and the completed MRR checklist in conformance with Annex G of ECSS-Q-ST-70-12.

b. The PCB manufacturer shall acknowledge the purchase order, confirm the delivery date and start the tooling activities.

6.2.5 Design review (DR)

a. The PCB manufacturer shall initiate the DR, as specified in requirement 5.2.a to 5.2.g from ECSS-Q-ST-70-12 and provide compliance of the provided PCB definition dossier to the PID.

NOTE 1 This is also done at MRR which is at a later stage in the procurement. It is important that this information is available at the quotation phase.

NOTE 2 Design review includes design rule check (DRC).

NOTE 3 Design review is included within the tooling process.

6.2.6 MRR

a. The PCB manufacturer shall complete the MRR checklist.

b. The PCB manufacturer shall perform the MRR in conformance with the requirements 5.2.h to 5.2.k from ECSS-Q-ST-70-12.

c. The PCB manufacturer and procurement authority shall review during the MRR as a minimum the following aspects:

1. Design review of PCB definition dossier including review items
2. Traceability of any design modifications
3. Build-up
4. Panelisation, placement of coupons and PCBs in the panel
5. Risk assessment
6. Compliance to ECSS-Q-ST-70-12
7. Compliance to ECSS-Q-ST-70-60
8. Compliance to PID recorded in PCB approval sheet part 2 from Annex G.2.1b.

NOTE For the risk assessment, it is good practice to use a risk rating from 1 to 5. At a risk rating until 3 it is typical that the PCB manufacturer endorse the responsibility of the risk. At a risk rating of 4 or 5 it is typical that the procurement authority endorses the responsibility of the risk. At a risk rating from 3 to 5 it is good practice to involve the project for acceptance of the risk, because there can be a potential schedule impact.

d. In case more than three prepreg sheets are used between layers, it shall be a review item in the MRR.

NOTE More than three prepreg sheets can be used in case a large volume to be filled with resin while maintaining a specific dielectric thickness, such as for thick copper layers or blind vias.

6.3 Final and in-process inspection

a. The PCB manufacturer shall demonstrate that the available manpower and equipment are able to perform the final and in-process inspection.

NOTE The verification of this requirement is performed during the audit.

b. The PCB manufacturer shall include coupons on the panel for in-house quality control.

NOTE The panel also includes coupons for batch release and spare coupons. These are described in clause 8.

c. Visual standards that specify the quality characteristics shall be available to each inspector.

NOTE Visual standards for final inspection can consist of photos or drawings of microsections, which are given in clause 10.

d. Work instructions shall specify the processes for which an in-process inspection is performed.

e. Work instructions shall specify the methodology for final inspection in conformance with clause 8.

f. In-process inspection shall be performed, but not be limited to, the following processes:

1. Microvia laser drilling to verify the diameter to the capture pad in conformance with requirement 11.4.2.g of ECSS-Q-ST-70-12;
2. Microvia cleaning to verify its efficiency;
3. Etching to verify the tolerances on track width and spacing;
4. AOI to verify its efficiency;

5. Coverlay bonding to verify the aspect of flex laminate and coverlay in conformance with Table 10-51 and the absence of overlap of coverlay and pads in conformance with Table 10-16 Ref c.
6. Thickness measurements after lamination on all panels;
7. Comparison of lay-out to the drawing from the PCB definition dossier to verify presence of plated and non-plated holes and milling.

NOTE 1 For process 1 and 2, a homogeneous dielectric thickness in microvia layers is necessary to avoid nonconformances such as interconnect defect. The local thickness of dielectric can be affected by the designed footprint and the tolerances of prepreg thickness.

g. The PCB manufacturer shall specify in its PID an approach for TMA measurements to determine Tg and CTE in Z-direction, including frequency of test and material and technology of test vehicle.

NOTE This test is specific for a build-up and for the used process equipment.

h. The PCB manufacturer shall specify in its PID the range of etchback.

i. In-process control by IST testing shall be in conformance with clause 9.5.5.2.1.

6.4 Quality records for manufacture and procurement

a. The PCB manufacturer shall retain the quality records for at least ten years or in accordance with business agreement requirements.

b. The quality records shall be composed of the following:

1. Documentation of the final inspection of manufactured PCBs, including CoC and lab reports in conformance with Annex B;
2. Nonconformance reports and corrective actions in conformance with ECSS-Q-ST-10-09;
3. Qualification test reports, in conformance with requirement 5.9c;
4. Traveller;
5. Batch summary statistics;
6. Process records.

NOTE Process record typically include SPC of chemical processes, maintenance and calibration records.

c. Non-nominal performance of equipment, materials or processes shall be documented including the following topics:

1. Root cause investigation;
2. Corrective action;

3. Effect on previous, ongoing and future manufacturing batches;
4. Assessment by QA personnel.

NOTE These topics are the same as for an NCR in conformance with ECSS-Q-ST-10-09.

d. The PCB manufacturer shall maintain a database for calibration of electrical and mechanical manufacturing and test equipment.

e. The PCB manufacturer should provide to the procurement authority the list of nonconformances specific to them, as reported quarterly in the QA report in conformance with F.2.1.3.

6.5 Control of materials and chemistry

a. The base materials shall be in conformance with clause 5 from ECSS-Q-ST-70.

b. The base materials shall be in conformance with IPC-4101E for rigid laminates, IPC-4103A for RF laminates, IPC-4204A for flexible laminates and IPC-4203A for coverlay.

c. In case of double insulation in conformance with requirement 6.2.3d, the base materials for rigid laminates and prepreg shall be in conformance with IPC-4101E Appendix A.

NOTE Double insulation is specified in clause 13.9 of ECSS-Q-ST-70-12. Annex I describes the more stringent cleanliness requirements for prepreg and laminate from IPC-4101E Appendix A.

d. Base materials in conformance with IPC-4101E Appendix A shall be manufactured by a laminate supplier that is listed in the IPC QPL or that passed a specific audit from the PCB manufacturer.

e. Prepreg, laminate, flex laminate, coverlay, bondply, copper foil, heat sinks and metal core shall be selected, inspected and tested in conformance with the work instruction as specified in the PID.

NOTE Tests can include chemical and physical testing.

f. The PCB manufacturer shall separate, and prevent the use of raw materials and semi-finished products that are awaiting completion of test results.

g. The PCB manufacturer shall segregate, mark and record noncompliant materials and PCBs.

h. The PCB manufacturer shall control the storage conditions and duration of materials and chemistry with limited shelf-life and verify the validity of the relevant material for use.

i. The verification and relife procedure of limited shelf-life materials shall be in accordance with ECSS-Q-ST-70-22, except for prepreg in conformance with requirement 6.5j.

j. The verification and re-life procedure of prepreg shall be performed by the raw material supplier and documented in a new CoC for the prepreg.

NOTE 1 The new prepreg CoC include a new shelf-life. Shelf-life and storage conditions are important for the flow factor of prepreg, particularly for no-flow prepreg.

NOTE 2 It is good practice to allow for the lead time for relife tests when anticipating supply of material for PCB manufacture.

k. Pure tin finish with > 97 % purity shall not be used, in conformance with the requirement 5.2.2.a of ECSS-Q-ST-70.

l. Electrolytic copper plating shall have a purity of ≥ 99.5 % copper.

m. Electrolytic soft gold plating shall have a purity of ≥ 99.8 % gold, except for the case of electrolytic hard gold plating.

n. Electrolytic hard gold plating may contain 0.3% cobalt.

o. For solderless connection hard gold shall be used.

p. For wire bonding or adhesive bonding soft gold shall be used.

NOTE For wire bonding bright aspect is preferred but matt aspect can be used.

q. Electrolytic pure nickel plating shall have a purity of ≥ 99.95 % nickel, except in the case of electrolytic nickel alloy plating.

r. Electrolytic gold plating shall have ≤ 0.2% silver.

6.6 Cleanliness of PCB processes

6.6.1 Overview

PCBs can fail due to latent short circuits, which can be caused by random contamination inside the dielectric PCB material. Contamination can comprise of fibres in laminate or on prepreg layers and can originate from the PCB manufacturing processes or from the base material supply chain.

Cleanliness of base materials is addressed to the base material supply chain as described in requirements 6.5c and 6.5d.

High resistance electrical test is specified on final PCBs with the aim to identify leakage current that can be caused by contamination, as specified in 9.3.7.

THB test on coupons is specified in 9.7.2 with the aim to determine the effects of contamination on ECM.

The clause 6.6.2 specifies requirements for the PCB manufacturing processes. The processes after innerlayer etching until lay-up are considered critical with respect to cleanliness. The PCB manufacturing processes are mostly taking place in rooms with controlled environment. This environment can, however, include the risk of collecting dust particles on materials processed or stored in these rooms. The lay-up process is the final process during which innerlayers can be inspected. This process is also the most critical one for introducing

unwanted contamination. The requirements specified in this clause address this risk. This can be referred to by the term "FOD prevention".

Another risk can be created by contaminants, such as agglomerations of solvent residue, that can be embedded and remain invisible on raw materials. High temperature during lamination can cause these contaminants to carbonise. This risk is not specifically addressed or mitigated by this clause.

6.6.2 Cleanliness control

a. The PCB manufacturer shall treat all processes from innerlayer etching until lay-up as critical processes with respect to cleanliness.

b. The PCB manufacturer shall have a cleanliness control procedure that includes at least the following:

   1. cleanliness of prepreg sheets until the lay-up process and any cleaning methods in conformance with requirement 6.6.2f;

   2. cleanliness of etched innerlayers until the lay-up process and any cleaning methods in conformance with requirement 6.6.2f;

   3. verification of the efficiency of cleaning on innerlayers and prepreg and its acceptance criteria;

   4. restrictions of the use of materials that charge statically and attract fibres;

   5. clean room practices in lay-up area in conformance with requirements 6.6.2c, 6.6.2d, 6.6.2e, 6.6.2g and 6.6.2h;

   6. reference to work instructions for the general cleaning of the room;

   7. reference to work instructions to segregate epoxy resin dust from polyimide in conformance with requirement 6.6.2i.

      NOTE 1 Materials used with innerlayers that show static charging are, for instance, separator sheets or transport trays.

      NOTE 2 Verification of cleanliness of innerlayers or prepreg can be done by inspection under UV light and bright light. Dust particles are UV fluorescent. Epoxy resin dust is UV fluorescent. Polyimide resin dust is typically not UV fluorescent.

c. The room for the lay-up process shall include the following:

   1. overpressure;

   2. filtered air supply;

   3. protective clothing that do not release fibres for operators;

   4. prevention of sticky surfaces or cavities in furniture where fibres collect.

      NOTE Protective clothing can include shoes, hat, coat, and gloves.

d. The room for the lay-up process should include the following:

1. monitoring of airborne contamination;
2. general clean room class 8 or better, in accordance with ISO-14644-1.

NOTE A formal cleanroom class as per ISO specification is difficult to obtain because of handling prepreg inside the room that creates dust. The objective is to reduce the risk of foreign contaminants in the room.

e. Local measures for cleanliness at the lay-up area should include the following:

1. laminar flow bench;
2. de-ionisation equipment;
3. local monitoring of particulate contamination;
4. local cleanliness class 6 or better, in accordance with ISO-14644-1.

f. Prior to lay-up, cleaning of prepreg sheets and etched inner layers should be performed by using vacuum hovering or by use of tacky rollers or wipes.

g. Motor parts for any vacuum hovering should be located outside of the room for lay-up.

NOTE A vacuum hose can be brought into the room through the wall.

h. The use of particle counters at the lay-up area should allow for the presence of prepreg dust.

NOTE Measurements can be taken on Monday morning prior to the first operation in the room. As soon as prepreg sheets are handled, measurements are compromised by the prepreg dust that is not a breach of cleanliness as long as it is similar material used for the lay-up.

i. Segregation of polyimide and epoxy materials in the lay-up area shall prevent inclusion of epoxy prepreg dust in the lay-up of polyimide.

NOTE This is done because epoxy can decompose and carbonise during the processing of polyimide. This can also be important for other materials combinations.

j. The PCB manufacturer shall provide instructions to operators on the measures specified in its cleanliness control procure.

NOTE Examples of instructors to operators can include labels on the work floor, photographic instructions on best practices, identification of critical areas, and training.

6.7 Traceability

a. The PCB manufacturer's records shall identify for all batches of PCBs the traceability of all raw materials and semi-finished products listed in the traveller and the individual process steps mentioned herein.

NOTE 1 In most cases a batch of PCBs is manufactured using raw materials from the same production batch. But it is also common practice to mix raw material from various production batches within the same PCB batch. This requirement provides this traceability.

NOTE 2 Traceability to raw materials does not need to be included in the CoC, since the procurement authority is not able to evaluate this information. Instead, the QA documentation of the PCB manufacturer is subject to audit or to specific enquiry from its customers.

b. All panels within a batch shall be laminated on the same day and plated on the same day, except the case in requirement 6.7c.

c. In case panels within a batch are not laminated on the same day or not plated on the same day, it shall be reported on the CoC.

d. In case panels within a batch are not laminated on the same day or not plated on the same day, the reason for it should be reported on the CoC.

e. Each PCB and coupon shall have a unique marking for traceability to batch and panel number.

f. The marking on PCB and coupon shall be resistant to tests and processes.

g. Marking on coverlay for flexible PCB and sculptured flex PCB shall not lift after tape test in conformance with clause 9.4.5.

h. The marking shall be in conformance with the PCB definition dossier.

i. The outgassing of marking shall be in conformance with ECSS-Q-ST-70-02.

j. Conductive marking shall be treated as a conductive element on the PCB.

k. The traceability from the PCB manufacturer shall enable localisation of PCBs and coupons on the panel.

l. The PCB manufacturer shall issue a CoC in conformance with the DRD from Annex B for delivered PCBs within the batch.

m. In case some PCBs within the batch are delivered later, the PCB manufacturer shall at least issue a new declaration of conformance from the CoC in conformance with B.2.1.2.

NOTE Spare PCBs can be stored by the PCB manufacturer and delivered to the customer at a later time if re-ordered. In case the lab reports from the original delivered CoC covers the spare ones, a new lab report does not need to be

issued. The new declaration of conformance is sufficient to ensure traceability.

6.8 Operator and inspector training

a. All operators and inspectors shall be trained for their task and for the understanding of the applicable quality assurance requirements.

6.9 Repair of bare PCBs

6.9.1 Overview

Repair are operations done on a PCB at the end of the manufacture. They are usually the consequence of the visual inspection.

6.9.2 General

a. Repair operations shall be documented and justified in a work instruction by the PCB manufacturer and referenced in the PCB manufacturer's PID.

b. The capability of operators performing repair operations shall be validated by the PCB manufacturer.

NOTE This is the case for all operations, but is specifically mentioned here because of the criticality of the repair operation.

c. The repaired area shall be re-submitted to visual inspection in conformance with clause 9.3.1 by the PCB manufacturer by a different operator than the one who performed the repair.

d. The CoC shall provide traceability of all repair operations.

NOTE This traceability includes the location on the PCB.

e. The repaired area shall be submitted to visual inspection in conformance with clause 9.3.1 by the procurement authority during incoming inspection.

f. In case SnPb is missing on the surface, it may be added with a solder iron and flux on bare surface copper in case the following conditions are met:

1. the documented repair operation includes limits for temperature, duration and flux in conformance with ECSS-Q-ST-70-08;

2. the PCB manufacturer has inspected plated holes to verify the absence of missing SnPb inside them;

3. the PCB manufacturer has verified that the copper is non-etched in the area of missing SnPb.

NOTE Non-etched copper has a flat surface, whereas etched copper has a concave surface. In case

copper is affected by etching, the missing SnPb is a process indicator of a problem that can affect plated holes, which cannot be repaired.

g. In case dual surface finish of SnPb and electrolytic gold is used, oxidation of SnPb may be removed with a solder iron and flux.

h. Excess surface copper may be removed in case it is submitted to visual inspection for the absence of weave exposure in conformance with Table 10-43, Table 10-44 and other nonconformances.

NOTE Copper removal can be done with a scalpel or laser.

i. The total number of repairs in conformance with the requirements 6.9.2f, 6.9.2g and 6.9.2h may be performed maximum once per PCB surface area of 10x10cm.

j. Haloing exceeding the requirements of Table 10-50 and Table 10-45 may be repaired using adhesive in case the following conditions are met:

1. the haloing is not in contact with conductors on surface layer and the underlying layer;
2. the length of PCB edge for a single repair does not exceed 1 cm;
3. the total number of repairs on the PCB edges do not exceed 4.

NOTE Depaneling can cause haloing if an inadequate cutting method is used.

k. In case a PCB exceeds warp or twist requirements from clauses 9.3.3.2 or 9.3.3.3, it may be flattened using pressure and elevated temperature in case the following conditions are met:

1. The initial warp and twist does not exceed 1,6 %;
2. The customer accepts the responsibility for a PCB submitted to repair for improving flatness when this risk has been identified in the MRR.

NOTE This is specified because the PCB can increase its non-planarity after storage, bake out or assembly processes. These processes are not under control of the PCB manufacturer. The main cause for non-planarity is asymmetric build-up or shape, which is driven by the design from the procurement authority.

l. Nodules that reduce the diameter of PTH to below the requirement may be removed in case the following conditions are met:

1. The nodules are caused by fibres connecting to only 1 side of the hole wall;
2. The nodules are removed by applying slight mechanical force by probing with a gauge;
3. The integrity of the hole wall after repair is not compromised;
4. The integrity of the hole wall after repair is verified by inspection by the PCB manufacturer using a prismatic ocular;

5. SnPb is not reflowed after removal of nodule;
6. The number of repairs of nodules does not exceed 2 per PCB.

m. Other repairs that are not specified in this clause shall not be performed.

NOTE Examples of such repairs are:

- repair of burrs;
- brushing of overhang of Ni/Au or Au;
- repair of PTH with too small diameter due to excessive SnPb thickness.

6.10 Packaging

a. The PCBs shall be clean and dry before packaging.

NOTE Drying by PCB manufacturer is specified in requirements 9.2.2a and 9.2.2c.

b. The PCBs and the coupons shall be packed to prevent corrosion or physical damage.

c. The PCBs shall be individually packed.

d. The packaging material shall be non-corrosive and not leave residue on the PCB.

e. The packaging shall consist of sealed antistatic plastic bags.

f. PVC packaging shall not be used.

g. Packaging materials shall be in conformance with requirement 5.5.3.f of ECSS-Q-ST-70-08.

NOTE This requirement states that pink-polyethylene (pink-poly) bags, film, bubble wrap or foam near any ESD-sensitive item or within an ESD protected area are not used.

h. One of the following packaging methods shall be used:

1. Desiccant using plastic bags;
2. Dry nitrogen filling using moisture barrier bags;
3. Vacuum packing using moisture barrier bags.

i. If desiccant is used, precautions shall be taken to prevent damage due to contact between desiccant and PCB.

NOTE Damage can include mechanical damage due to pressure or friction. Damage can include chemical damage to the surface finish.

j. If desiccant is used, means for indication of moisture content shall be provided.

k. The PCBs and coupons shall be packed avoiding pressure on, or friction between the PCBs.

l. Tissue or paper may be used to wrap PCBs.

m. Each shipping container shall be marked according to requirements from the procurement authority.

6.11 Storage and baking of PCB and coupons

a. The procurement authority shall retain the quality records, coupons and microsection for at least ten years or in accordance with business agreement requirements.

b. PCBs shall be stored in a dry environment until they are soldered.

NOTE Dry storage can be performed in a nitrogen-purged cabinet or in a sealed bag with desiccant.

c. Spare coupons may be stored in an uncontrolled environment.

NOTE This is acceptable because it is considered worse-case.

d. Baking of PCBs prior to soldering, after short or long storage, shall be performed in conformance with requirement 9.2.2a.

6.12 Shelf-life and relife testing

a. Shelf-life of PCBs with SnPb finish shall be 2 years.

NOTE The term shelf-life refers to the period of storage of the bare PCB to the start of the soldering process.

b. Shelf-life shall include storage at the procurement authority and storage at the PCB manufacturer.

c. Shelf-life should be calculated from the date code on the CoC.

NOTE The date code on CoC corresponds approximately to the date of manufacture.

d. In case shelf-life is exceeded, the following shall be performed to relife the PCB:

1. evaluate solderability in conformance with clause 9.4.11 on the coupon in conformance with requirement 8.2.3d;
2. visual inspection on PCB in conformance with 9.3.1;
3. solder bath float test on spare coupon in conformance with 9.5.2.

NOTE 1 The effect of moisture ingress and efficiency of bake out is verified by the solder bath floating test. However, moisture removal occurs at a faster rate in small coupons compared to large PCBs. Moisture removal is particularly important for rigid-flex technology.

NOTE 2 No specific inspection of IMC is necessary as it is not expected to change significantly in the specified storage conditions. SnPb coverage in

compliance with Table 10-12 is essential to pass the solderability test and the SnPb coverage has been verified at outgoing (and incoming) inspection.

e. The relife period of a PCB shall be 6 months after successful relife testing.

NOTE 1 This is different from relife testing as described in ECSS-Q-ST-70-22, which allows a relife period from the date of expiration.

NOTE 2 Relife testing of PCBs up to 5 years of storage is performed with acceptable results on specific PCB technology from specific PCB manufacturers. The maximum storage duration depends on the initial solder coverage, among other things.

6.13 QA for PCB procurement in space projects

a. ECSS-Q-ST-70-60 shall be applicable for procurement of PCBs for flight models and for qualification models.

NOTE 1 Flight models include FM, FS, PFM. Qualification models include QM, EQM.

NOTE 2 There is no requirement to apply ECSS-Q-ST-70-60 to EM and EBB. However, nothing prevents to do it if so decided.

NOTE 3 This requirement is specified to ensure that the PCB manufacturer has feedback on meeting the requirements of ECSS-Q-ST-70-60 prior to manufacturing the flight batch and to avoid nonconformances due to lower quality levels for the referenced models.

b. The same PCB manufacturer should be used for PCB manufacture for flight models and qualification models.

c. In case a different PCB manufacturer is used for flight models and for qualification models, the impact on the following items shall be evaluated:

1. Electrical performance;
2. Mechanical performance;
3. Thermal performance;
4. Assembly approval status;
5. Any modifications of the PCB definition dossier.

NOTE It is not typical that change of PCB manufacturer impacts electrical, mechanical or thermal performance in case the PCB definition dossier is identical and the application is not critical. Examples of critical technology can be

impedance control, RF, specific mechanical stress applied during assembly.

d. The procurement authority shall ensure that all procured PCBs meet the project requirements.

NOTE Examples of projects with specific requirements are human spaceflight, long-term storage, detector technology, planetary exploration.

e. The procurement authority shall list each PCB technology, in conformance with the requirement 5.10b, in the DML as a separate item.

f. Individual raw materials and PCB manufacturing processes need not to be listed in the DML and DPL.

NOTE This is specified, because raw materials and manufacturing processes are covered by the PCB technology listed in conformance with 6.13e.

g. The procurement authority shall specify for each PCB technology the following:

1. PCB manufacturer;
2. PCB procurement specification;
3. PCB technology description in conformance with the requirement 5.10b;
4. traceability to individual PCBs and their PCB approval sheet.

NOTE The acronym or name of the PCB in the DML can provide the traceability to the PCB approval sheet.

h. The procurement authority shall complete a PCB approval sheet part 1 for each individual PCB type in conformance with requirementG.2.1a of the DRD in Annex G.

i. PCB approval sheet part 1 shall be submitted prior to the PDR and subject to approval during MPCB.

j. The procurement authority shall complete a PCB approval sheet part 2 for each individual PCB type in conformance with requirement G.2.1b of the DRD in Annex G.

k. PCB approval sheet part 2 shall be submitted prior to the CDR and subject to approval during MPCB.

NOTE 1 The reviewed PCB approval sheets 1 and 2 are available during equipment MRR.

NOTE 2 The PCB MRR provides input for PCB approval sheet part 2.

l. The procurement authority may reuse PCB approval sheets part 1 and part 2 from previous procurement in case the PCB design is recurrent.

NOTE A description of ‘recurrent’ designs is given in clause 4.1 of ECSS-Q-ST-70-12.

m. The procurement authority shall provide the PCB approval sheet part 1 and part 2 to its customer for review and approval during MPCBs.

n. During the MPCB, the customer may request to the procurement authority the review of the PCB definition dossier.

o. Customer approval shall be based on the compliance of technology parameters to the PID, as declared on the PCB approval sheet part 2.

p. In case of non-compliance of a technology parameter to the PID, a delta qualification plan shall be submitted to the customer in conformance with requirement 6.13q.

NOTE Clause 7.6 specifies the requirements of tests, inspections and specimen for delta qualification.

q. The delta qualification shall be covered by an RFA in conformance with clause 7.7 and reviewed during MPCB.

r. The documentation of FAI on PCB in conformance with clause 8.5 shall be available for review during MPCB.

s. The approval of the item in the DML shall be based on the review of PCB approval sheets of all PCBs covered by the item of the DML.

NOTE Approval by RFA in the DML is indicated by 'X' with the RFA reference number as described in table A-4 of ECSS-Q-ST-70.

t. The CoC of the PCB, its records of incoming inspection and any associated RFA shall be made available by the procurement authority at the equipment MRR.

NOTE In the context of space projects, the term "equipment MRR" is not the same as MRR for PCB manufacture, as specified in requirement 6.2.6b. The latter is referred to in this clause 6.13 as "PCB MRR" to distinguish from "equipment MRR".

7
Test and inspection for qualification

7.1 Overview

The matrix of selected tests for various qualification activities is shown in Table 7-1.

The tests included in each test group (group 1 to group 6) and the test vehicle is shown in Figure 7-1.

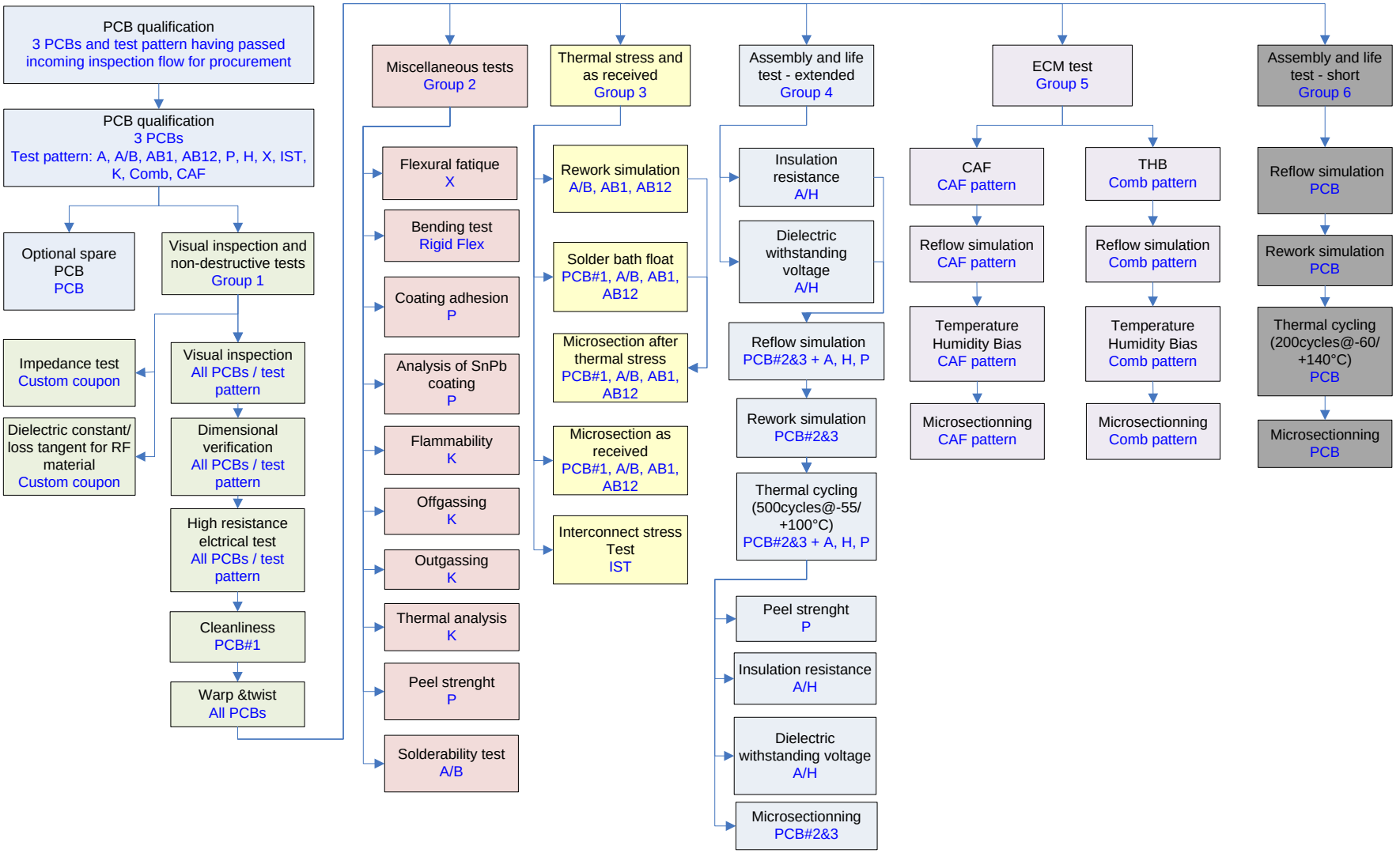


Figure 7-1 Test flow for qualification

7.2 Test selection for qualification activities

a. For all qualification activities, the PCBs and coupons shall be submitted to outgoing inspection and documentation in conformance with clauses 8.1, 8.2 and 8.3.

b. For initial qualification of a PCB manufacturer or a PCB technology, all tests of groups 1, 2, 3, 4, and 5 shall be performed on PCB and coupon.

c. For qualification renewal of a technology the following test shall be performed on PCB and coupon:

   1. Group 2: peel strength and solderability;

   2. Group 3: all.

d. For delta qualification of a process or equipment change that affects the properties of the dielectric material, the following tests shall be performed on PCB and coupons:

   1. Group 1, 3, 5: all;

   2. Group 4 or 6: all;

   3. Group 2: peel strength, flexural fatigue, bending test, internal short circuit, water absorption, outgassing, thermal analysis.

e. For delta qualification of a process or equipment change that affects the properties of the copper plating or surface finish, the following tests shall be performed on PCB and coupons:

   1. Group 1: visual inspection;

   2. Group 3: all;

   3. Group 4 or 6: all;

   4. Group 2: peel strength, solderability, analysis of SnPb coating, coating adhesion of non-fused SnPb.

f. For delta qualification of PCB design features, the following tests shall be performed on PCB and coupons, except for track width and spacing as specified in requirement 7.2g:

   1. Group 1, 3: all;

   2. Group 4 or 6: all.

      NOTE PCB design features include hole size, aspect ratio, number of layers, lamination or drilling sequences, thickness of Cu or PCB.

g. For delta qualification of track width and spacing, the following tests shall be performed on PCB and coupons:

   1. Group 1: visual inspection;

   2. Group 3: microsectioning as received including at least the following aspects:

      (a) track width on foot and tolerances;

(b) insulation distance and tolerances;

(c) undercut;

(d) etching efficiency and absence of spurious copper;

(e) encapsulation of track by resin.

h. For qualification of HDI technology, the following tests shall be performed on PCB and coupons:

1. Group 1, 3, 4, 5: all;

2. Group 2: peel strength.

Table 7-1: Test matrix for qualification and procurement

Scope of testing	Group 1 Visual inspection and non-destructive tests	Group 2 Miscellaneous tests	Group 3 Thermal stress and as-received	Group 4 Assembly and life test -extended	Group 5 ECM test	Group 6 Assembly and life test - short
Y - indicates test group to be included P - indicates part of test group to be included						
Initial qualification **requirement 7.2a**	Y	Y	Y	Y	Y	N
Qualification renewal **requirement 7.2c**	Y	P peel strength, solderability	Y	N	N	N
Delta qualification **requirement 7.2d** **Process or equipment change affecting dielectric material**	Y	P peel strength, flexural fatigue, bending test, microsection, internal short circuit, water absorption, outgassing, thermal analysis	Y	Y	Y	Y
Delta qualification **requirement 7.2e** **Process or equipment change affecting plating**	P visual inspection	P peel strength, solderability, analysis of SnPb coating, coating adhesion of non fused SnPb	Y	P microsection	-	Y
Delta qualification **requirement 7.2f** **PCB design features**	Y	-	Y	P microsection	-	Y

Scope of testing	Group 1 Visual inspection and non-destructive tests	Group 2 Miscellaneous tests	Group 3 Thermal stress and as-received	Group 4 Assembly and life test -extended	Group 5 ECM test	Group 6 Assembly and life test - short
Y - indicates test group to be included P - indicates part of test group to be included						
(hole size, aspect ratio, number of layers, lamination or drilling sequences, thickness of Cu or PCB)						
Delta qualification **requirement 7.2g** **PCB design features (track width and spacing)**	P visual inspection	-	-	Y	-	-
Qualification of HDI Technology **requirement 7.2h**	Y	P peel strength	Y	Y	Y	Y
Project qualification **clause 7.7**	Y	-	Y	P microsection	-	Y
FAI **clause 8.5**	Y	-	Y	P microsection	-	-
Procurement **clause 8**	Y	-	Y	P microsection covered by RW sample from group 3	-	-

7.3 Initial qualification of PCB manufacturer

a. Initial qualification of a PCB manufacturer shall be in conformance with clause 5.

b. The test selection for initial qualification of PCB manufacturer shall be in conformance with requirement 7.2a.

7.4 Initial qualification of PCB technology

a. The test selection for initial qualification of PCB technology shall be in conformance with requirement 7.2a.

b. The PCB manufacturer of the new technology shall already hold a qualification in conformance with clause 5.

c. The PCB manufacturer shall issue a new PID for the new technology to be qualified, in conformance with the requirement 5.10b.

d. The preparation of the microsection for the qualification of the rigid-to-flex interface shall be performed using UV fluorescent resin and vacuum potting and inspected using polarised light.

NOTE See example in Figure 8-4

7.5 Qualification renewal

a. The test selection for qualification renewal shall be performed by the qualification authority in conformance with requirement 7.2c.

7.6 Delta qualification

a. The test selection for delta qualification of materials, processes, design or equipment shall be performed by the PCB manufacturer in conformance with requirements 7.2d, 7.2e, 7.2f and 7.2g.

b. The baseline test flow may be tailored and supplemented by additional tests to cover the delta qualification.

c. The delta qualification shall be in conformance with clause 5.12 and documented in the process change notice.

d. Upon approval of the delta qualification test report in conformance with requirements 5.9c and 5.9d, the PCB manufacturer shall document the qualified changes in the PID.

e. Delta qualification of track width and spacing shall include records of AOI and visual inspection on etched inner layer to check for top and bottom of track, etch definition and spurious copper in clearance.

NOTE This is performed to evaluate the efficiency of the AOI processes for its ability to detect all dimensions under delta qualification.

f. In case delta qualification is initiated in the context of a space project, the procurement authority shall handle it through an RFA, in conformance with clause 7.7.

7.7 Project qualification and RFA

7.7.1 Overview

It is preferred to use PCB technology and PCB manufacturers that are qualified in conformance with ECSS-Q-ST-70-60. Project qualification can be necessary for the use of technology that is not available from qualified sources, for instance in case innovative technology is needed. Such project qualification includes a risk to the project because the PCB technology is not widely used and because the project qualification may fail.

In case project qualification is needed, it is preferred to perform it at a PCB manufacturer that is already qualified for other technology in conformance with ECSS-Q-ST-70-60 because QA and capability has been reviewed during periodic auditing.

In case delta qualification is initiated for a space project and it is handled through an RFA, in conformance with the requirement 7.6f, it is recommended that the delta qualification for a project results in an update of the PID of the qualified PCB manufacturer. In this case, upon future procurement of the same technology, a new project qualification is not needed.

Project qualification provides approval of a PCB technology for the batch used on that project only. In case of recurrent PCB procurement, a new project qualification of the new batch is needed if the PID does not include the technology.

Project qualification typically uses a group 6 test flow which is designed to be a fast test flow on a limited number of test vehicles. This can be insufficient justification for an update of the PID depending on the technology under evaluation. Delta qualification can ensure a more thorough assignment of test flows and test vehicles with the objective to provide justification for the update of the PID.

Similarity of PCB designs covered by the project qualification can be reviewed during the DR and can result in tailoring of the project qualification test plan.

7.7.2 Requirements for project qualification and RFA

a. PCB technology that is not qualified in conformance with requirement 5.1a shall be subject to project qualification using an RFA in conformance with requirement 5.4.2d from ECSS-Q-ST-70.

b. The procurement authority shall submit to its customers for approval the RFA part 1 including the following:

1. PCB approval sheet in conformance with Annex G;
2. Compliance matrix to ECSS-Q-ST-70-60 for PCB qualification and description of the non-qualified aspects;
3. Compliance matrix to ECSS-Q-ST-70-12C for PCB design;
4. Compliance matrix to the PID from the PCB manufacturer;
5. Description of the thermal, electrical and mechanical environment of the application;
6. Project qualification test plan.

c. Non-qualified PCB technology should be procured from a PCB manufacturer that is qualified in conformance with ECSS-Q-ST-70-60 for other technology.

NOTE In this case only a delta qualification is recommended to be performed for the specific technology feature that is not qualified. This reduces the risk, since other technologies are already qualified and periodic auditing has been performed.

d. DR shall be performed in conformance with 6.2.5a with support of the PCB manufacturer to review the manufacturability and reliability of the design and to review previous heritage and test campaigns performed.

e. The DR should be performed together with the final customer.

f. In case risk factors are identified during DR, specific tests and inspections shall be specified during this meeting to mitigate the risk.

g. The qualification test plan in conformance with 7.7.2b.6 shall include tests and inspections to evaluate all PCB technology features under qualification.

h. The project qualification test plan shall include group 6 in conformance with clause 9.8.

i. The group 6 from the qualification test plan should be performed on one spare PCB from the FM batch.

NOTE The advantage of testing the FM batch is to ensure representativity. This is important when using non-qualified PCB manufacturers for whom batch-to-batch QA has not been verified by an audit in conformance with ECSS-Q-ST-70-60. The disadvantage of testing the FM batch is that any nonconformances are discovered at a late stage of the procurement.

j. The group 6 from the qualification test plan may be tailored to cover specific project requirements and PCB technology features under qualification.

k. The project qualification test plan may include specific evaluations on coupons and non-destructive inspection on PCBs.

l. The project qualification test plan shall include IST testing in conformance with clause 9.5.5 in case the PCB technology is within the technology perimeter of IST.

m. The procurement authority shall submit to its customers for approval the RFA part 2 including the following:

1. project qualification test report describing the results of the group 6 in conformance with 7.7.2g;

2. test report for specific evaluation on coupons and PCBs in conformance with 7.7.2j and 7.7.2l;

3. CoC and its lab reports in conformance with 8.3a.

n. In case delta qualification is initiated for a space project under RFA in conformance with the requirement 7.6f, the project qualification should result in an update of the PID of the qualified PCB manufacturer.

o. Project qualification shall provide approval of a PCB technology for the batch used on that project only.

p. In case of recurrent PCB procurement, a new project qualification of the new batch shall be performed if the PID does not include the technology.

NOTE Therefore it is recommended to perform delta qualification of a qualified PCB manufacturer and update its PID, in conformance with requirement 7.7.2n.

q. In case suppliers use IPC standards as PCB procurement specification, the following conditions shall be met:

1. Perform the project qualification using group 6 in conformance with clause 7.7.2.

2. In case double insulation is applicable, the PCB design is in conformance with chapter 6.3 from IPC-2221B for electrical clearance.

3. IPC-6012D and IPC-6012DS for space applications are used for rigid PCBs.

4. IPC-6018C and IPC-6018CS for space applications are used for RF PCBs.

5. IPC-6013C is used for flexible and rigid-flex PCB.

6. PCB manufacturers are on the IPC QML or have passed a specific audit from the procurement authority to assess compliance to the IPC standards from conditions 3, 4 and 5.

7. Coupons and PCBs of all panels are evaluated in conformance with clause 8.

8. Coupon inspection is performed by a third-party lab for evaluation in conformance with IPC-A-600 and the applicable IPC standards from conditions 3, 4 and 5.

NOTE 1 For requirement 7.7.2q.1 during the project qualification, any HDI technology or embedded film components are evaluated.

NOTE 2 For requirement 7.7.2q.1 this is in conformance with IPC-6011 clause 3.6 which specifies that the qualification assessment is as agreed between user and supplier (AABUS).

NOTE 3 For requirement 7.7.2q.2 it is good practice to implement the additional risk mitigations for double insulation in conformance with the present standard and ECSS-Q-ST-70-12.

NOTE 4 For requirement 7.7.2q.3 it is not good practice to use only IPC-6012D class 3, which represents a lower quality class.

NOTE 5 For requirement 7.7.2q.5 it is good practice to use IPC-6013CS for space applications when this is issued.

NOTE 6 For requirement 7.7.2q.7 coupon evaluation includes IST testing in conformance with clause 9.5.5 when this is applicable to the technology.

NOTE 7 For requirement 7.7.2q.7 coupon evaluation includes three times solder bath float test and rework simulation, among others.

NOTE 8 For requirement 7.7.2q.7 PCB visual inspection is performed using 10-40x magnification.

NOTE 9 For requirement 7.7.2q.7 PCB evaluation includes high resistance electrical test with 1 GΩ insulation resistance threshold.

8
Test and inspection for procurement

8.1 Outgoing inspection on PCB

a. The PCB manufacturer shall submit PCBs to outgoing inspection as follows:

   1. visual inspection in conformance with clause 9.3.1;
   2. dimensional verification in conformance with clause 9.3.2;
   3. warp and twist in conformance with clauses 9.3.3.2 and 9.3.3.3;
   4. high resistance electrical test in conformance with clause 9.3.7.

b. The sample plan for the outgoing inspection from requirement 8.1a shall be in conformance with Table 8-1.

   NOTE Table 8-1 specifies sampling on external layers of PCBs during outgoing visual inspection. Internal layers are inspected during microsectioning for outgoing inspection as specified in clause 8.2. In addition some in-process inspections are specified in clause 6.3.

c. The PCB manufacturer and procurement authority may specify a more frequent sampling plan or additional measurement locations in the PCB definition dossier.

   NOTE This can be the case if a review item has been identified during MRR, for instance for the compliance of dimensional aspects. This can be the case for small connectors using small diameter PTH that can be blocked with SnPb. This can also be the case when board geometry is critical for placement in an electronic box. Some designs can specify the thickness over metallisation. Some designs can have complex geometry due to rigid-flex or cut-outs.

d. The PCB manufacturer shall perform referee testing on a spare PCB in case this is specified in Table 10-26.

e. The presence of coupons, the evaluation of coupons, the delivery of coupons to the customer and the delivery of microsection to the customer shall be in conformance with Table 8-2.

Table 8-1: Sampling plan for outgoing visual inspection on PCB

Test method and inspected feature	Sampling
Visual inspection	all PCBs and coupons
Dimensional verification: Thickness	in-process inspection on all panels as per 6.3f.6 and 1 PCB from the batch
dimensional verification: Length and width	1 PCB from the batch
Dimensional verification: diameter of all PTH size	1 PCB from the batch for PTH ≤ 0,6 mm upon customer request: all PCBs
Dimensional verification: smallest conductor width and spacing	1 PCB from the batch for fine pitch: all PCBs
Warp and twist	1 PCB from the batch that is worst-case
Electrical test	all PCBs and coupons

8.2 Outgoing inspection on coupons

8.2.1 Overview

This clause describes the test flow, coupon configuration and inspection methods on coupons and PCBs for procurement. Table 8-2 and Figure 8-1 shows a non-exhaustive overview of coupons and tests specified in this clause. This table shows when evaluations are performed.

Table 8-2: Overview of coupons

Set ID	Location	Feature and name of coupon as per IPC-2221B	Test	Condition for presence of coupon	Condition for evaluation of coupon	Coupon delivered to customer	Microsection delivered to customer
set 1	one corner	PTH and via on A/B	AR + RW	yes	yes	no	yes
		sequential via on Bn	AR	yes	yes	no	yes
		PTH and via on A/B	customer coupon	yes	yes	yes	no
		sequential via on Bn	customer coupon	yes	yes	yes	no
		tracks on A/B	min track width and spacing	yes	optional	yes	optional
set 2	opposite corner	PTH and via on A/B	SB	yes	yes	no	yes
		sequential via on Bn	SB	yes	yes	no	yes
		PTH and via on A/B	customer coupon	yes	yes	yes	no
		sequential via on Bn	customer coupon	yes	yes	yes	no
		tracks on A/B	customer coupon	yes	optional	yes	optional
set 3	anywhere	PTH on A/B	solderability	yes	yes for SnPb < 1 µm	yes	n.a.
		rigid-flex interface on X	SB	yes for applicable technology	yes	no	yes
set 4	4 corners	electrical registration on R	electrical registration	yes for annular ring < 50 µm	yes	yes	n.a.
set 5	anywhere	IST coupon	IST test	yes for applicable technology	yes	yes	optional
set 6	anywhere	peel strength on P	peel strength	yes	optional	yes	n.a.
		coating adhesion on P	tape test	yes	optional	yes	n.a.
		flex bend cycles on X	bend test	yes for applicable	yes	optional	optional

Set ID	Location	Feature and name of coupon as per IPC-2221B	Test	Condition for presence of coupon	Condition for evaluation of coupon	Coupon delivered to customer	Microsection delivered to customer
				technology			
set 7	anywhere	insulation resistance on E	insulation resistance	yes	optional	yes	n.a.
		DWV on E	DWV	yes	optional	yes	n.a.
		controlled impedance on Z	controlled impedance	yes for applicable technology	optional	optional	n.a.
		embedded film resistance	resistance	yes for applicable technology	optional	optional	optional
set 8	anywhere	pure laminate	thermal analysis	yes	optional	yes	n.a.

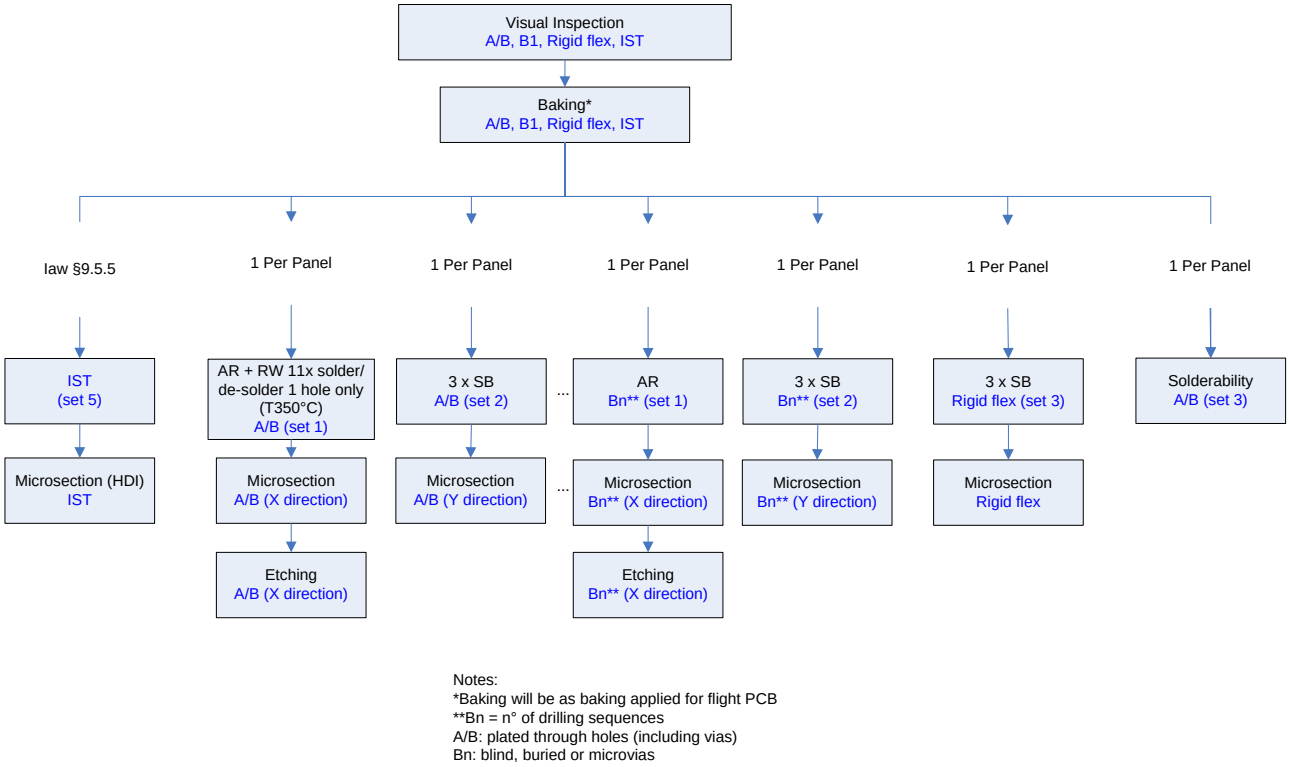


Figure 8-1 flow for preparation, test and inspection of procurement coupons

8.2.2 Configuration of coupons for plated holes

a. Coupons shall be designed in conformance with clause 15 of ECSS-Q-ST-70-12.

b. Each panel shall include the following coupons for plated holes:

   1. Coupon A/B;

   2. Coupon B1, B2… Bn.

      NOTE These coupons can be designed in accordance with IPC-2221B. However, other custom designs are used that cover the same features.

c. Coupon A/B shall include the following features:

   1. PTH with maximum or most frequently used diameter;

   2. through-going via with minimum diameter.

      NOTE For 8.2.2c.1 coupon A of IPC-2221B can be used, and for 8.2.2c.2 coupon B of IPC-2221B.

d. Coupon A/B shall include at least 4 holes.

e. Coupon B1, B2… Bn shall include the following features:

   1. blind via for each plating sequence with minimum diameter;

   2. buried via for each plating sequence with minimum diameter;

   3. microvia for each plating sequence with minimum diameter.

NOTE This is coupon B1, B2, etc. of IPC-2221B.

f. The suffix of coupon B1, B2… Bn shall indicate the plating sequence of the vias that are included.

NOTE An example of vias manufactured at different plating sequences is shown in Figure 8-3.

g. The term "coupon Bn" shall indicate all coupons B1, B2 … Bn for all plating sequences.

h. Coupons for plated holes shall include rows and columns of holes to enable microsectioning of a coupon in both x-direction and y-direction.

NOTE The IPC coupons are designed in a square.

i. Al least two coupons for plated holes shall be placed on opposite corners of the panel to enable assessment of annular ring in both corners.

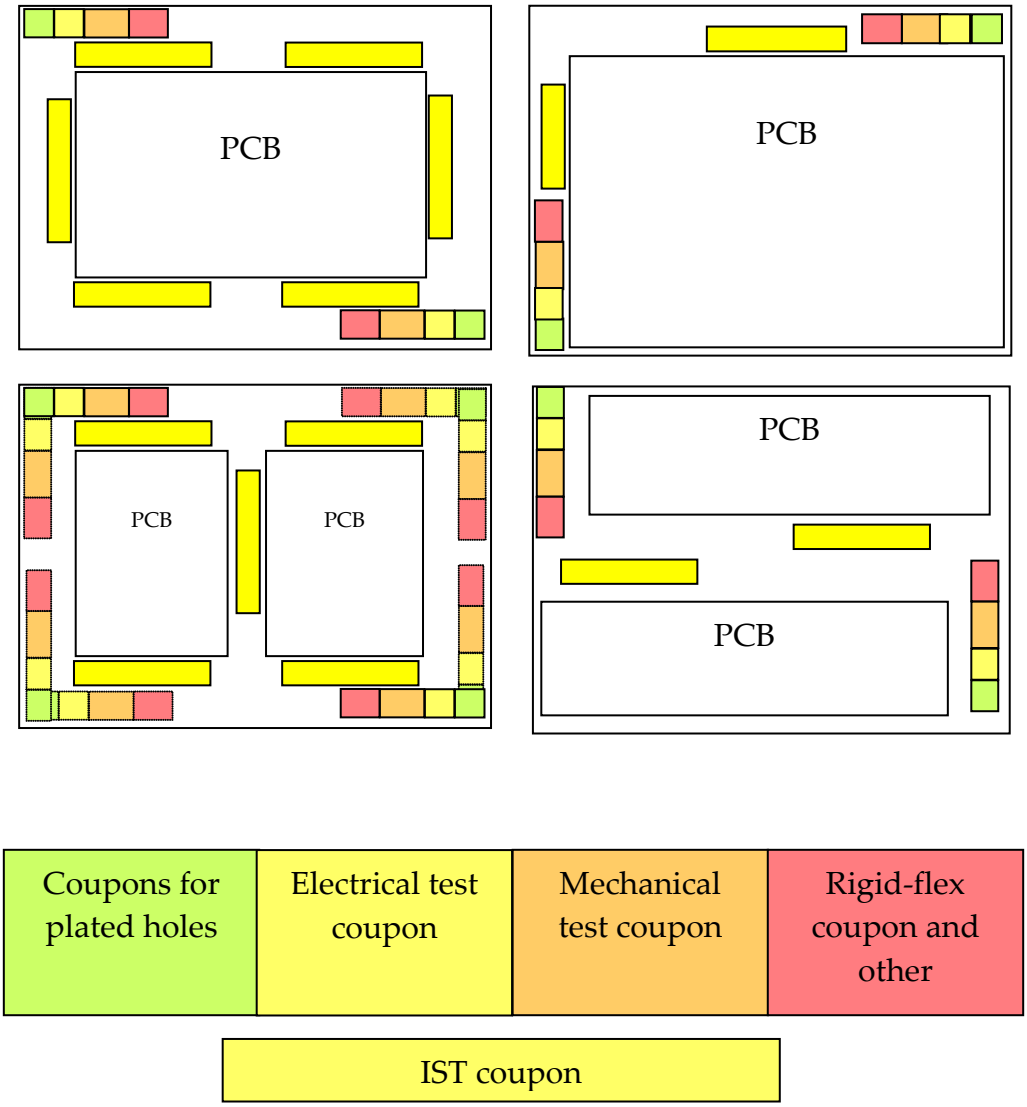


Figure 8-2 Example of placement of coupons and PCB in usable area of manufacturing panel

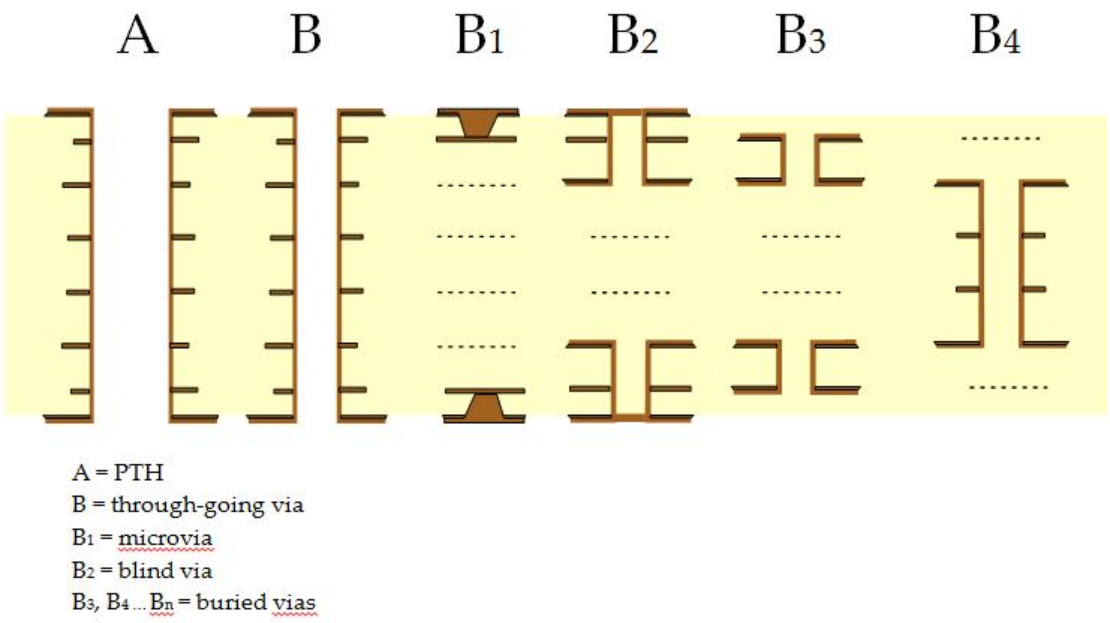


Figure 8-3 Example of vias manufactured at different plating and drilling sequences

8.2.3 Configuration of dedicated coupons

a. In case the technology is within the technology perimeter for IST as specified in the clause 9.5.5.2, the IST coupon shall be designed and tested in accordance with clause 9.5.5.

b. In case of a rigid-flex PCB, a coupon with rigid-to-flex interface shall be included on each panel.

NOTE It is good practice to include in this coupon the via nearest to the rigid-to-flex interface.

c. For designs with reduced annular ring of 25 µm in conformance with requirement 11.5.2.a of ECSS-Q-ST-70-12, electrical registration coupons shall be included on all four corners to verify the annular ring.

NOTE This is coupon F of IPC-2221B. Alternatively, a dedicated pattern can be available on IST coupons.

d. A coupon shall be present for solderability testing.

NOTE 1 This can be achieved by repeating the A/B coupon of IPC-2221B.

NOTE 2 Performing solderability testing is specified in case SnPb < 1 µm in conformance with Table 10-12.

e. In case more than one PCB is placed in the panel, a coupon for evaluation of plating should be placed in the middle of the panel.

NOTE A coupon for plating can be an IST coupon, A/B coupon or a spare PCB. An example of coupon

placement in the centre of the panel is shown in Figure 8-2.

f. If embedded film resistors are used, they shall be included in the coupons, in conformance with requirement 15.2.d.13 of ECSS-Q-ST-70-12.

g. If controlled impedance is used, it shall be included in the coupons, in conformance with requirement 15.2.g of ECSS-Q-ST-70-12.

NOTE Commonly used test probes need a coupon to verify controlled impedance. Some advanced test probes are available, however, that allow testing on the PCB.

h. A coupon shall be present that include minimum track width and spacing on each layer, in conformance with requirement 15.2.d.9. of ECSS-Q-ST-70-12.

NOTE It is good practice to include minimum track width and spacing in the A/B coupon for plated holes.

i. A coupon shall be present that include patterns for mechanical tests in conformance with requirement 15.2.f.2 of ECSS-Q-ST-70-12.

NOTE Mechanical tests include peel strength and coating adhesion. Flex bend cycles can be performed on the coupon with rigid-to-flex interface of requirement 8.2.3b.

j. A coupon shall be present that includes patterns for electrical tests in conformance with requirement 15.2.f.3 of ECSS-Q-ST-70-12.

NOTE Electrical tests include insulation resistance, dielectric withstanding voltage. Specific electrical test conditions can be specified by the procurement authority in conformance with requirement 9.6.3d.

k. A coupon shall be present to perform thermal analysis.

NOTE 1 The coupon can be an area of approximately 1x1 cm without copper and without vias.

NOTE 2 Thermal analyses are used to investigate stability of materials, processes and design. Strict acceptance criteria can be unavailable in which case the test is evaluated against the heritage and datasheets or used for failure investigation.

8.2.4 Evaluation of coupons

a. All coupons shall be evaluated by visual inspection, in accordance with requirements from clause 9.3.1.

b. Evaluation of acceptance criteria for visual inspection and microsectioning shall be performed in accordance with requirements

from clause 10.The coupons specified in requirements 8.2.3d, 8.2.3h, 8.2.3i, 8.2.3j and 8.2.3k may remain untested for procurement.

c. Coupons for plated holes shall be submitted to microscopic inspection in the following conditions:

1. each hole type: as received;
2. each hole type: solder bath float in accordance with clause 9.5.2;
3. at least one PTH: rework simulation in accordance with clause 9.5.4.

NOTE The holes adjacent to the one submitted to RW are considered to be in as-received condition. This allows assessment of both conditions in a single microsection.

d. Microsectioning on coupon A/B shall be performed on at least 4 holes.

e. The microsectioning of coupons for plated holes of each hole type shall be performed in both x-direction and y-direction for assessment of annular ring in both directions.

NOTE To reduce the number of coupons and microsections, it is common practice to microsection the thermally stressed coupon in perpendicular direction to the as received coupon.

f. The microsections of the as-received coupons for plated holes shall be submitted to microscopic inspection in as-polished and micro-etched conditions.

g. The microsection of the thermally stressed coupons for plated holes shall be submitted to microscopic inspection in as-polished condition.

NOTE This is specified because micro-etch reveals the interface between plated copper layers. Therefore this is less efficient to evaluate any plating separation.

h. Solderability test shall be performed for procurement, except in case of requirement 8.2.4i.

i. Solderability test need not to be performed for procurement in case the following conditions are met:

1. The surface finish is hot oil reflowed SnPb;
2. The thickness of the SnPb as specified on the CoC of the panel is in conformance with the requirements of Table 10-12;
3. The PID does not specify that solderability testing is mandatory for procurement.

NOTE In case the thickness of SnPb is not in conformance with the requirements of Table 10-12 as determined during qualification (renewal), the PID can specify that solderability test is performed for all procurement. This is

usually the case upon request by the qualification authority.

j. The microsection of the coupon with the rigid-to-flex interface shall be submitted to microscopic inspection after solder bath float, in as-polished condition.

k. The preparation of the microsection of the coupon with the rigid-to-flex interface should be done using UV-fluorescent resin and vacuum potting and inspected using polarised light.

NOTE This is mandatory for qualification as specified in requirement 7.4d.

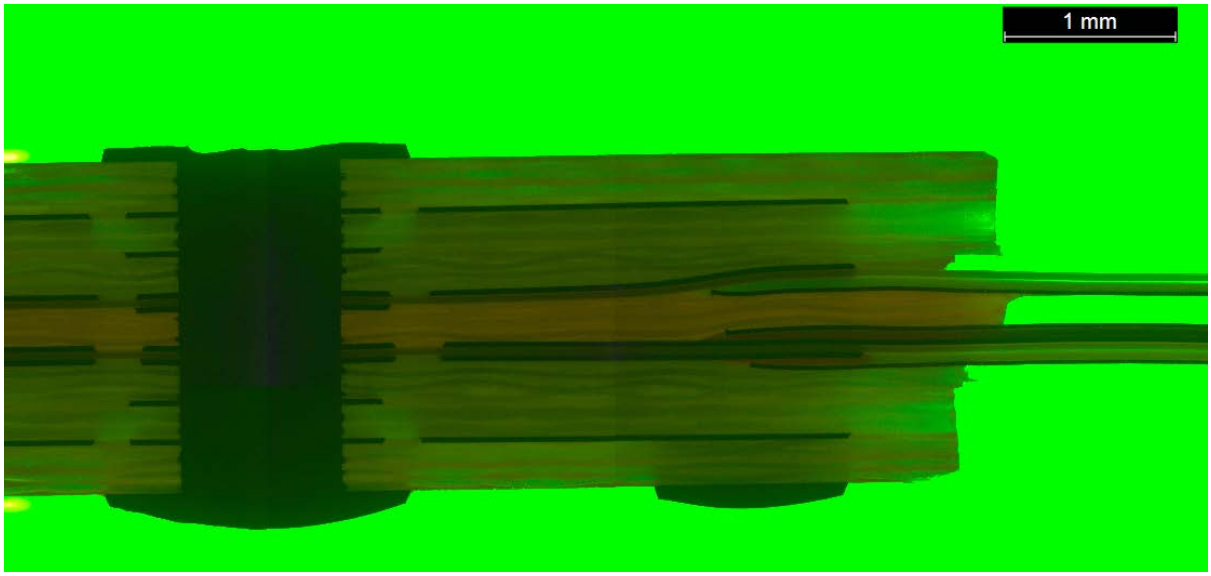


Figure 8-4: Example of target quality of microsection of rigid-flex interface with UV fluorescent resin and polarised light

8.2.5 Delivery of coupons, microsections and spare coupons

a. Coupons shall be delivered to the procurement authority in conformance with the Table 8-2.

b. The IST coupon may be send later than the other coupons, due to its logistics of test and shipment.

c. The following microsections shall be delivered to the procurement authority:

1. Microsections of coupons for plated holes;
2. Microsections of coupon for rigid-to-flex interface.

NOTE This is summarised in Table 8-2.

8.3 Reporting of outgoing inspection and delivery

a. The PCB manufacturer shall report the results of the outgoing inspection on PCB and coupons in the lab reports of the CoC, in conformance with the DRD of Annex B.

NOTE 100 % visual inspection of PCBs is specified in requirement 8.1a.1, whereas the lab report specifies the requirements for the documentation of the visual inspection.

b. The CoC and its lab reports shall be delivered to the procurement authority.

c. The PCB manufacturer shall not deliver a PCB with nonconformances to ECSS-Q-ST-70-60.

d. The PCB manufacturer shall not deliver without approval from the procurement authority a PCB with nonconformances to the PCB definition dossier.

NOTE This includes definition of holes, milling, non-plated holes, dimensional and mechanical requirements, among other things as described in the DRD of annex A of ECSS-Q-ST-70-12.

8.4 Incoming inspection by procurement authority

a. The procurement authority shall perform incoming inspection as follows:

1. Visual inspection on all PCBs, in conformance with the clause 9.3.1,
2. Microscopic inspection on microsections, in conformance with the clause 10.2, by one of the following institutes:
   (a) procurement authority;
   (b) external third-party lab;
   (c) assembly house;
   (d) PCB manufacturer using another inspector than the one for outgoing inspection.
3. Verification of the CoC and its lab reports, in conformance with the Annex B,
4. Verification of quantity,
5. Verification of integrity of packaging.

NOTE 1 The PCB manufacturer provides microsections used for the CoC and customer coupons. Both can be used for the incoming inspection. To avoid deterioration of the surface quality of microsections, it is preferred to perform incoming inspection as soon as possible after delivery.

NOTE 2 Microsection inspection for qualitative aspects is important and detection can be operator dependent. Therefore this requirement specifies to perform an additional verification.

b. The procurement authority need not to perform microscopic inspection of the microsection of the reworked hole in as-polished condition.

NOTE This is specified because the microsection with the reworked hole includes other holes as-received. These as-received holes are inspected as-polished and after micro-etching. The procurement authority can only inspect in as-polished condition by repolishing the etched section.

c. The procurement authority shall maintain records of the accepted incoming inspection.

NOTE Records of incoming inspection are made available during equipment MRR as specified in 6.13t.

d. In case of nonconformances during incoming inspection an NCR shall be issued by the procurement authority to the PCB manufacturer.

e. The procurement authority may perform incoming inspection at their own premises or at the premises of the PCB manufacturer.

NOTE If performed at the premises of the PCB manufacturer, the inspection is typically named: FCSI or MIP or DRB or buy-off.

f. The procurement authority shall complete the incoming inspection within 3 months after availability of the PCBs.

8.5 FAI on PCB by microsectioning

a. FAI on PCB shall include the microsectioning of a representative PCB from the batch for the first procurement.

NOTE FAI is performed in supplement of the standard outgoing and incoming inspection on PCBs and coupons.

b. FAI on PCB should be performed on a representative PCB from the batch for the first procurement, if a technology is procured from a PCB manufacturer for the first time.

c. During FAI on PCB, the microsectioning shall verify the technology features that are procured for the first time.

d. In case of FAI on PCB, it shall be performed and documented by the procurement authority within 4 months after availability of the PCBs, by using one of the institutes specified in requirement 8.4a.2.

e. The documentation of FAI on PCB shall be provided by the procurement authority to the PCB manufacturer.

NOTE FAI is reviewed during MPCB as specified in requirement 6.13r.

f. FAI on PCB shall be performed in case double insulation applies, in conformance with the requirement 13.9.2d of the of ECSS-Q-ST-70-12.

g. FAI on PCB should be performed in case the PCB design is complex and the coupon cannot be designed with full representativity, in conformance with the requirement 15.2 b of ECSS-Q-ST-70-12.

9
Test descriptions

9.1 Overview

This clause describes the test methods for the groups 1 to 6. An overview of this is shown in Figure 7-1.

Some test methods can include acceptance criteria. Test methods that include visual inspection of PCBs and coupons, and microscopic inspection of microsections have acceptance criteria specified in clause 10.

Examples of test patterns and coupons are included in each test method. Reference is made to test patterns from IPC-2221B. In future it is expected that other IPC standards also include test patterns.

9.2 Additional tests

9.2.1 Cleanliness

a. The cleanliness of the samples prior to test and inspection shall be in conformance with 6.10a.

NOTE In case samples need to be cleaned, a cleaning method is specified in clause 11.1 of ECSS-Q-ST-70-08.

9.2.2 Bake-out

a. Standard bake-out shall be minimum 8 hours at 120 °C in ambient pressure.

NOTE Baking is performed to remove humidity from the dielectric materials prior to thermal excursions. PCB laminates are known to be hygroscopic.

NOTE This bake-out is in conformance with clause 8.5d of ECSS-Q-ST-70-38.

b. In case the PCB technology or the test criteria are affected by humidity, the bake-out may be tailored to improve its efficiency.

NOTE Improving efficiency of the bake-out can be established by a longer duration, vacuum or

dry environment or a stepped baking profile. This can be necessary for thick PCBs, a high number of copper plane layers, a high number of flex laminate layers or samples stored in non-controlled environment. Tests that can be significantly affected by humidity include thermal excursions and high resistance electrical test.

c. The PCB manufacturer may tailor the bake-out in case samples are processed immediately after reflow as a final process step.

d. After bake out, re-absorption of humidity shall be prevented until thermal stress testing.

NOTE Precautions can include short duration (for example less than 8 hours) of storage between bake-out and thermal stress test or storage in dry conditions.

9.2.3 Plated copper tensile strength and elongation

a. Plated copper tensile strength and elongation shall be performed in conformance with test method 2.4.18.1a from IPC-TM-650 or an equivalent test method.

b. Plated copper tensile strength shall be ≥ 276 MPa.

c. Plated copper elongation shall be ≥ 18 %.

9.2.4 Steam ageing

a. The test shall be carried out in conformance with test 20a of IEC 60326-2-am 1 (1992-06).

NOTE This test is intended to give an indication of the effects of storage on the solderability of the PCBs. Steam ageing is also described in paragraphs 3.4.3 and 3.4.4. of IPC-J-STD-003C. Steam ageing is an optional method for preconditioning samples in the solderability test as specified in requirement 9.4.11.4c.3.

b. The specimen shall be exposed in the steam generator machine for approximately 80 minutes.

c. After closing the generator, it shall be purged with nitrogen at a flow rate between 250 ml/minute and 750 ml/minute.

d. The temperature inside machine shall be (100 ± 2) °C and stabilized for (5 ± 1) minutes.

e. The nitrogen flow shall be switched off.

f. The 90 °C condensed steam rate in the chamber shall be controlled to (5 ± 0,5) l/minute.

g. A mixture of pure oxygen 20 % and nitrogen 80 % with a flow rate of (100 ± 10) ml/minute shall be switched on for (60 ± 5) minutes.

h. After removing the specimens from the steam generator machine, they shall be dried.

9.3 Group 1 – Visual inspection and non-destructive tests

9.3.1 Visual inspection - general

a. Visual inspection shall be performed using 10x to 40x magnification.

NOTE Examples of equipment used for visual inspection are: binoculars, loups, single scope.

b. Visual inspection shall cover the entire surface of both sides of the sample.

c. Visual inspection shall be performed using high illuminating light sources.

NOTE ECSS-Q-ST-70-08 clause 5.4.a requires 1080 lux. However, higher intensities are typically used for bare board inspection.

d. In case of any suspected nonconformance, the area shall be re-examined at higher magnification of 20x to 40x.

9.3.2 Visual inspection for qualitative aspects

a. Visual inspection for qualitative aspects shall be performed on PCB and coupons for conformance with acceptance criteria from clauses 10.4 and 10.5.

9.3.3 Visual inspection for dimensional verification

9.3.3.1 General

a. Physical dimensions shall be measured for verification of the PCB definition dossier.

NOTE 1 In addition to the specified measurement, the physical dimensions are also submitted to visual inspection in conformance with clause 9.3.1.

NOTE 2 The mechanical drawing is typically used to specify physical dimensions and tolerances of the PCB.

b. PCB thickness shall be measured over base laminate on corners and on the middle of the PCB, unless another methodology is specified in the PCB definition dossier.

c. Length and width of the PCB shall be measured over all edges of the inspected PCB.

d. The diameter of plated and non-plated holes shall be verified for all hole diameters.

e. The number of hole diameters for verification on the inspected PCB shall be specified by the PCB manufacturer.

NOTE Hole diameters can be measured with measuring gauges, a measuring microscope or dedicated automatic systems.

f. Vias of ≤ 0,6 mm may be omitted during dimensional verification of its diameter, unless dimensional verification of these holes is specified in the PCB definition dossier.

NOTE This is because these holes can be blocked with SnPb in conformance with requirement 10.6.3f.

g. Minimum conductor width and spacing shall be measured on external layers.

NOTE 1 Conductors include tracks and SMD pads.

NOTE 2 Conductor width and spacing on internal layers are present on the coupon in conformance with 8.2.3h for optional evaluation by microsectioning. Minimum track width and spacing on internal layers are evaluated by in-process inspection in conformance with 6.3f.3.

h. Minimum conductor width and spacing shall be measured at the foot of the conductor, except for the case specified in requirements 9.3.3.1i and 9.3.3.1j.

NOTE An example of conductor width measured at the foot is shows as seen in a cross section in Figure 9-1.

i. In case overhang or undercut causes the top of the conductor to protrude from the foot, conductor width and spacing shall be measured at the widest point of the conductor.

j. In case of RF PCBs the conductor width may be measured in conformance with the PCB definition dossier.

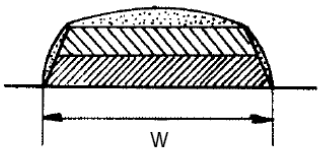


Figure 9-1 Conductor width (w) measured at the foot as seen in a cross section.

9.3.3.2 Warp

a. Warp shall be measured in conformance with the test method 2.4.22c from IPC-TM-650.

NOTE "Bow" is a term that is synonymous to "warp".

b. The PCBs shall be placed unrestrained on a horizontal surface with the convex side upward.

c. The two corners of the measured edge shall be in contact with the horizontal surface.

d. The warp shall be expressed in percentage terms.

e. The maximum distance between the horizontal surface and the PCB shall be measured as specified in Figure 9-2.

f. The length of the PCB shall be measured.

g. Warp shall be calculated as follows:

1. Warp [%] = max distance [mm] / length of PCB [mm] x 100

h. The maximum warp shall be ≤ 1,5 %.

i. The procurement authority may specify a more stringent requirement for warp in the PCB definition dossier.

NOTE 1 A typical stringent warp and twist requirement is ≤ 0,75 %, which is in conformance with IPC-6012DS reference 3.4.3.

NOTE 2 This can be done for complex assembly, such as large components without stress relief, where less warp and twist can avoid stress on component assembly.

NOTE 3 Warp and twist are strongly affected by the symmetry of the build-up. In case the PCB is designed with asymmetric build-up in conformance with requirements 7.1.1a, 7.1.1b, 7.1.2a and 7.1.2d from ECSS-Q-ST-70-12, the procurement authority and PCB manufacturer mutually define the value in the MRR and in the PCB definition dossier. This agreed value cannot exceed ≤ 1,5 % in conformance with requirement 9.3.3.2h.

NOTE 4 On PTFE-based laminates it is not applicable to measure warp and twist because of the material softness.

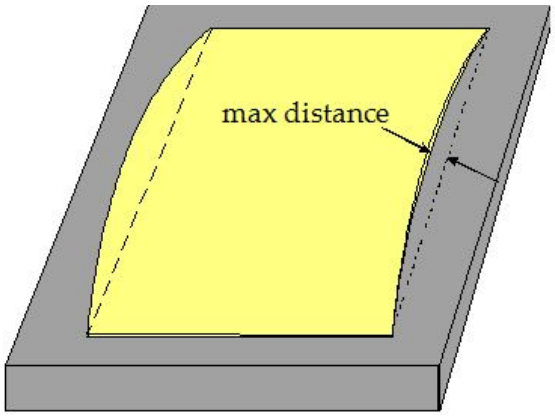


Figure 9-2: Warp

9.3.3.3 Twist

a. Twist shall be measured in conformance with the test method 2.4.22c from IPC-TM-650.

b. The PCB shall be placed on a horizontal surface so that it rests on three corners.

c. In case three corners cannot rest on the horizontal surface by restraining only one corner, the referee test shall be performed in conformance with chapter 5.3 of the test method 2.4.22c from IPC-TM-650.

d. The twist shall be expressed in percentage terms.

e. The distance between the horizontal surface and the fourth corner of the PCB shall be measured as specified in Figure 9-3.

f. The length of the diagonal of the PCB shall be measured.

g. Twist shall be calculated as follows:

   1. Twist [%] = max distance [mm] / length of PCB diagonal [mm] x 100

h. The maximum twist shall be ≤ 1,5 %.

i. The procurement authority may specify a more stringent requirement for twist in the PCB definition dossier.

NOTE See the notes 1, 2, 3 and 4 from clause 9.3.3.2.

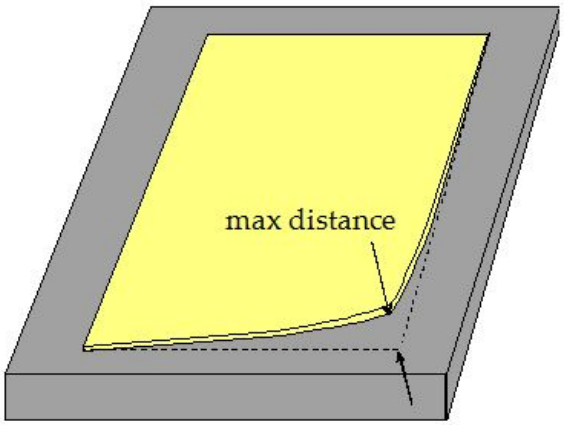


Figure 9-3: Twist

9.3.4 Impedance test

a. Impedance test for controlled impedance lines shall be performed using TDR in conformance with test method 2.5.5.7a of IPC-TM-650.

b. The measurement method for impedance test shall be specified by the procurement authority in the PCB definition dossier.

NOTE This includes nominal impedance and tolerances, transmission line types and reporting. Typical acceptable tolerance can be 10%. DC resistance compensation can be used.

c. Impedance test may be performed on specific coupons or on PCB.

NOTE Specific equipment and training is needed for impedance testing on PCB. It can be difficult to design an impedance coupon that is representative of the PCB. Therefore, this measurement is typically performed on the PCB.

9.3.5 Dielectric constant and loss tangent

a. Dielectric constant and loss tangent of RF materials shall be measured on specific coupons in conformance with test method 2.5.5.2a of IPC-TM-650.

b. The measurement method for dielectric constant and loss tangent shall be specified by the procurement authority in the PCB definition dossier.

NOTE This includes tolerances and reporting.

9.3.6 Cleanliness

a. Cleanliness testing of PCB shall be performed in conformance with clause 11.3 of ECSS-Q-ST-70-08 and test method 2.3.25.1 from IPC-TM-650.

b. The cleanliness value shall be ≤ 1,56 μg NaCl eq /cm².

NOTE 1 This value is historically driven by the limit for an assembled PCB. However, the cleanliness of a bare PCB is typically orders of magnitude better. Nevertheless, a more stringent value is not specified. It is good practice to have a cleanliness value of ≤ 0,1 µg NaCl eq /cm^2.

NOTE 2 Guidelines for cleanliness of bare PCB and assembled PCB are given in IPC-5703 and IPC-5704.

9.3.7 High resistance electrical test

9.3.7.1 Overview

PCBs can fail due to latent short circuits. It is acknowledged that random contamination inside the dielectrical PCB material is of concern, as discussed in clause 6.6. Contamination can comprise of fibres in laminate or on prepreg layers and can originate from the PCB manufacturing processes or from the base material supply chain. The presence of contamination can provide a pathway for leakage current and possible ECM.

Typical electrical testing applied on PCBs by a flying probe equipment, is specified in IPC-9252B and is based on an insulation threshold of 10 MΩ, corresponding to level C for IPC-6012D class 3. The objective of this test method is to verify electrical design, i.e. the absence of unintended connections in the circuit. For IPC-6012DS this test method is amended to 100 MΩ under 250 V bias.

The purpose of the high resistance electrical test method is to determine the quality of the insulation and possible imperfections in the dielectric material. The rationale is that contamination between nets can provide a high-Ohmic path that can be detected under high voltage bias and therefore fails this test. On PCBs that fail the high insulation requirement, it has been demonstrated by DPA that the high-Ohmic path was caused by contamination in the dielectric material.

Clause 9.6.3 requires insulation resistance of ≥1 GΩ (and orders of magnitude higher) for interlayer and intralayer on dedicated test patterns. The requirement for high insulation is further substantiated by the typical volume resistivity of dielectric materials in the order of 10^8 MΩ-cm, determined at humid conditions of 90% RH in accordance with test method 2.5.17.1 of IPC-TM-650.

It is not the purpose of the high resistance test method to stress the dielectric material by screening for the operational voltage with a specified margin. For operational voltages higher than the test voltage (of 250V), a specific test can be specified by the procurement authority in the PCB definition dossier, such as a dielectric withstanding voltage test. The high test voltage of 250 V is applied because it is necessary to generate a leakage current that can be detected by the test equipment and that corresponds to a high insulation threshold of 1 GΩ.

Application of the test voltage of 250V on the smallest insulation distance for standard as well as HDI technology results in a worst-case electrical field of

approximately 3 kV/mm. This is acceptable for the purpose of this high resistance test, because of the heritage with this test voltage on PCBs, the electrical strength specified in datasheets in the order of ≥30 kV/mm and the short duration of the sustain time.

Precautions, such as dehumidification of air, are needed to prevent discharge due to ionisation of air, which has a breakdown strength of 1.5-3.0 kV/mm depending on humidity. This is important for surface conductors spaced approximately 170 μm or closer.

9.3.7.2 High resistance electrical test method

a. High resistance electrical test shall be performed on final PCBs using flying probe equipment.

b. The test voltage shall be ≥ 250 V.

c. The insulation threshold shall be ≥ 1 GΩ.

d. The sustain time shall be ≥ 5 ms.

e. During the ramp-up from 0 to 250 V, the test voltage shall be monitored.

f. Lack of voltage stability during the sustain time and during the ramp-up shall be recorded as test failure.

g. The horizontal adjacency distance shall be ≥ 1,27 mm in-plane.

h. The vertical adjacency distance shall be ≥ 1,27 mm in-plane on the layers above and below the specified net.

NOTE Horizontal and vertical adjacency is specified as a distance in-plane of the PCB to the tested net. This is illustrated in Figure 9-4.

i. Direct resistive isolation testing shall be performed.

j. Indirect isolation testing by signature comparison shall not be performed.

k. The PCB should be dehumidified by baking prior to testing.

l. In case the first test fails between 0,1-1,0 GΩ, one further bake and re-test may be performed.

m. In case the test fails below 0,1GΩ, re-test shall not be performed.

NOTE Failure above 0,1 GΩ can occur due to insufficient surface cleaning or insufficient dehumidification. High temperature during baking can affect the quality of the surface finish which is verified by the PCB manufacturer.

n. In case the test fails because the set voltage is not achieved due to high capacitance caused by presence of plane layers, one further re-test may be performed with adjusted parameters.

NOTE Such adjustment can include longer sustain time or longer ramp-up time.

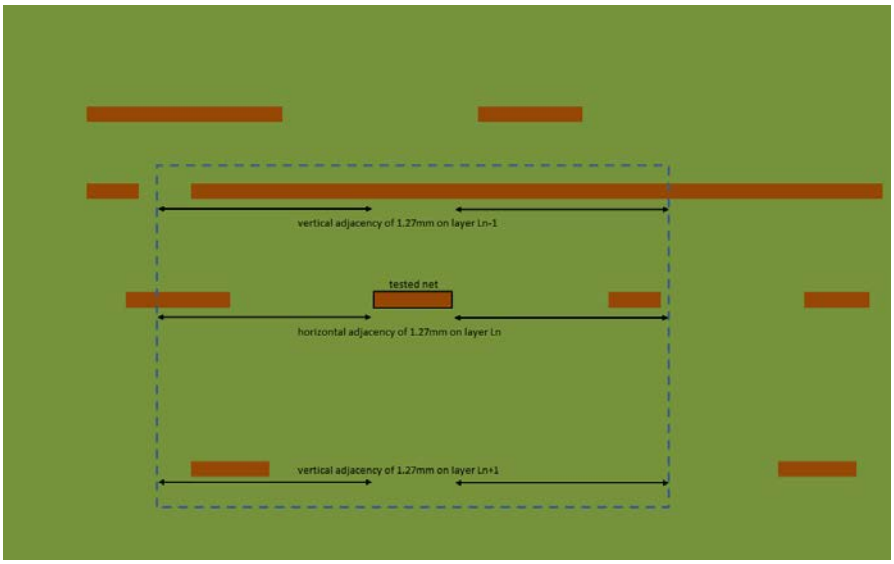


Figure 9-4: Horizontal adjacency on layer Ln and vertical adjacency on the layers above and below.

9.4 Group 2 - Miscellaneous tests

9.4.1 Overview

Long-time overload and short-time overload testing is specified in ECSS-Q-ST-70-10 clauses 7.3.5.1.2 and 7.3.5.1.3. These tests assess the ability of copper tracks and vias to carry a specified current. This test is considered obsolete and covered by the following:

- copper foil and copper plating quality is monitored by specifying purity , elongation, layer thickness and its procurement specification,
- dielectric quality and thermal robustness is monitored by thermal stress tests and by specifying layer thickness and its procurement specification,
- current carrying capacity and self-heating of conductors is specified in PCB design in clause 13.6 of ECSS-Q-ST-70-12.

Internal short circuit testing has been specified in ECSS-Q-ST-70-10 clauses 7.3.5.2. This test assesses leakage current in dielectric insulation between different nets on specific test patterns on coupons. This test is considered obsolete and covered by the following:

- High resistance electrical testing on PCBs in conformance with clause 9.3.7.

Water absorption testing is specified as an optional test in ECSS-Q-ST-70-10 clauses 7.3.6.1. This test assesses the weight percentage of water that can be absorbed by the dielectric materials. This test is considered obsolete and covered by the following:

- Water absorption is described in the specifications of raw materials, such as IPC-4101E for rigid laminates, IPC-4103A for RF laminates, IPC-4204A for flexible laminates, IPC-4203A for coverlay.
- A standard bake-out and prevention of re-absorption are specified for thermal stress tests and assembly.
- The effect of water absorption on ECM is assesses by THB and CAF testing in conformance with clause 9.7.

9.4.2 Peel strength

a. The test shall be carried out in conformance with condition A of test method 2.4.8c from IPC-TM-650.

b. The conductor selected shall be peeled back at one end for a length of approximately 10 mm.

c. The detached end of the conductor shall be gripped over its whole width.

d. Traction shall be applied in a direction perpendicular to the plane of the sample until the copper starts to peel away.

e. The rate of traction shall be kept constant at 50 mm/minute.

f. The traction direction shall be kept perpendicular to the plane of the sample.

NOTE This can be achieved by positioning the sample on a sliding platform.

g. Machine inertia shall have no effect on the measurement.

h. The conductor width shall be the measured width over which the conductor is adhered to the substrate.

NOTE Test coupon P from IPC-2221B is an example of a suitable test pattern.

i. Peel strength shall be as follows:

1. On epoxy: ≥ 12 N/cm;
2. On polyimide: ≥ 12 N/cm;
3. On PTFE reinforced/ceramic filled or non-filled: ≥ 8 N/cm;
4. Cross-linked hydrocarbon: ≥ 8 N/cm;
5. Aramide/polyimide: ≥ 6 N/cm;
6. On flex laminate: ≥ 10 N/cm.

9.4.3 Flexural fatigue

a. Flexural fatigue shall be determined only for flexible laminate.

NOTE The objective of the flexural fatigue test is to determine the ductility and adhesion of copper cladding, kapton laminate and coverlay.

b. The flexible sample shall include etching of the pattern and coverlay bonding representative of the PCB.

c. Flexural fatigue test shall be performed for a flexible PCB.

NOTE A flexible PCB can be manufactured using a double sided flex laminate or sculptured copper layer.

d. Flexural fatigue test shall be performed for a rigid-flex PCB on the individual flexible laminate.

NOTE Flexural fatigue test assesses the bare laminate properties. The individual flexible laminate can be non-representative of a rigid-flex PCB in case multiple flexible layers are used or laminated together. In this case, the bending test assesses the representative construction.

e. Flexural fatigue test shall cover only static applications.

NOTE Dynamic applications are project qualified in conformance with requirement 8.6.2b of ECSS-Q-ST-70-12.

f. The test shall be carried out in conformance with test method 2.4.3.1c of IPC-TM-650 and paragraph 3.10.14 of IPC-6013C.

NOTE The equipment can be similar to the automated equipment described in IPC-TM-650 2.4.3.1c. Alternatively the test can be performed using a manual equipment.

g. The test shall be performed using the following parameters:

1. Number of cycles is 250;
2. One cycle includes bending the flex laminate upwards 90° and downwards 90°;
3. The diameter of the mandrel over which the flex laminate is bend is between 3 mm and 10 mm;
4. The rate does not exceed 20 cycles per minute.

NOTE For requirement 9.4.3g.3, IPC-TM-650 2.4.3.1c recommends 6,35 mm for single sided flex laminate. ECSS-Q-ST-70-10 clause 7.3.3.3 specifies 9,6 mm. A typical test is performed using 3,2 mm.

h. Before and after the test, the resistance shall be measured using 4-wire resistance measurement with the sample in flat condition, bend 90° upwards and bend 90° downwards.

i. The flexural fatigue test shall be performed on two samples manufactured in zero and 90°, covering both orthogonal directions.

NOTE This is done to allow T-shaped and L-shaped flex sections. In addition, the raw material CoC can lack the traceability of the processing direction of the copper cladding. A typical flex

laminate can use rolled and annealed copper in conformance with requirement 8.3.3.d and 8.3.3.e of ECSS-Q-ST-70-12. In this case, the performance of flexural fatigue can be better in the rolled direction than in the other direction. This is caused by the long grain direction of the rolled copper.

j. The test vehicle shall be microsectioned at the zone that was bend during the test.

k. The acceptance criteria shall be as follows:

1. Resistance change is ≤ 10 %;

2. Visual and microscopic inspection is in conformance with clause 10.

NOTE 1 This is done to verify absence of adhesion defects between coverlay and copper, between coverlay and flex laminate and between copper and flex laminate in the bend flexible zone.

NOTE 2 Test coupon X from IPC-2221B is an example of a suitable test patterns.

9.4.4 Bending test

a. Bending test shall be performed only for rigid-flex PCBs.

NOTE The objective of the bending test is to determine the adhesion of flex layers and the rigid-to-flex interface.

b. Bending test shall cover only static applications.

NOTE Dynamic applications are project qualified in conformance with requirement 8.6.2b of ECSS-Q-ST-70-12.

c. The test shall be carried out in conformance with requirements 9.4.3f and 9.4.3g, 9.4.3h, except for the following:

1. Number of cycles is 25;

2. The radius of the mandrel over which the flex laminate is bend equals 12x the thickness of the flexible laminate.

NOTE The build-up of flex laminate with lowest thickness includes 25 µm flex laminate, with 35 µm copper cladding on both sides, with 25 µm coverlay on both sides, with approximately 10 to 20 µm adhesive between coverlay and flex laminate. This results in approximately 165 µm thickness. The minimum bend radius of 12x is in conformance with clause 8.6.2.a of ECSS-Q-ST-70-12. The minimum mandrel radius

therefore equals 1.98 mm, corresponding to a diameter of 3,96 mm.

d. The test vehicle shall be the final rigid-flex PCB.

NOTE This is representative of the number of flex laminates, the thickness of flex laminate, thickness of copper cladding, thickness of coverlay, thickness of bond-ply and penetration of coverlay and bond-ply into the rigid section.

e. The test vehicle shall be microsectioned at the rigid-flex interface and at the zone that was bend during the test.

f. The acceptance criteria shall be as follows:

1. Resistance change is ≤ 10 %.

2. Visual and microscopic inspection is in conformance with clause 10.

NOTE This is done to verify absence of adhesion defects between coverlay and copper, between coverlay and flex laminate, between copper and flex laminate and between prepreg and coverlay in the rigid-to-flex interface and in the bend flexible zone.

9.4.5 Coating adhesion – tape test

a. The coating adhesion test shall be performed in conformance with test method 2.4.1e from IPC-TM-650.

NOTE Coating adhesion test is performed to determine adhesion of surface finish. Examples of surface finish that can be submitted to this test are SnPb, galvanic Au or Ni-Pd-Au.

b. After cleaning, an adhesive tape, at least 50 mm long, shall be applied to the test surface and pressed down to eliminate all air bubbles.

c. After 1 minute, the tape shall be quickly pulled off perpendicular to the coating surface.

d. The surface area to be tested shall be at least 1 cm^2 of conductor.

e. The tape shall have an adhesion of at least 4,4 N/cm.

NOTE Example of tape that can be used is 3M Brand 600 with a width of 13 mm.

f. The surface finish shall not peel from the test surface or stick to the tape.

NOTE Coating adhesion test can be performed on coupon P from IPC-2221B.

9.4.6 Analysis of tin-lead coating

a. The tin-lead alloy should be chemically dissolved.

b. The relative quantities of tin and lead should be determined by atomic absorption spectrometry.

NOTE This is the recommended method for SnPb.

c. Another method resulting in the same degree of precision may be used.

d. The composition of tin-lead shall be: Sn = 63 % ± 8 %

NOTE 1 Lead-rich underplating of tin-lead finish can cause the content of tin in the final reflowed finish to be below the required 55 %.

NOTE 2 Analysis of SnPb coating can be measured coupon P from IPC-2221B.

9.4.7 Outgassing

a. The outgassing test shall be performed in conformance with ECSS-Q-ST-70-02.

b. The outgassing test shall be performed on a specimen without copper.

c. The outgassing shall be determined by measurement of the difference in weight of the specimen before and after the test.

d. The outgassing shall be:

1. RML ≤ 1 %;
2. CVCM < 0,1 %.

9.4.8 Thermal analysis

a. Thermal analysis should be performed on a sample without copper.

b. Td shall be measured in conformance with test method 2.4.24.6 of IPC-TM-650 using TGA.

c. T288 shall be measured in conformance with test method 2.4.24.1 of IPC-TM-650 using TMA.

d. Tg should be measured in conformance with test method 2.4.25c of IPC-TM-650 using DSC.

e. Tg may be measured in conformance with test method 2.4.24c of IPC-TM-650 using TMA.

NOTE Tg, T288 and Td are important properties that affect the thermal reliability, especially for assembly operations.

f. CTE in Z-direction or Z-axis expansion shall be measured in conformance with test method 2.4.24c of IPC-TM-650 using TMA.

NOTE CTE in Z-direction is an important property that affects the thermal reliability of a via. “Z-axis expansion” is measured over a wide temperature range of 50-260°C, which typically generates more reliable test data than “CTE in Z-direction”.

g. The results of thermal analysis should be verified against the slash sheet of IPC-4101E and the supplier specification of the raw materials.

9.4.9 Flammability

a. Flammability shall be in conformance with ESA-HRE-IPL-RQ-0002 chapter 9.2.3.

b. Flammability testing should be performed in conformance with ECSS-Q-ST-70-21.

NOTE This is important for human spaceflight. Product Assurance and Safety Requirements for ISS Pressurized Payloads ESA-HRE-IPL-RQ-0002 chapter 9.2.3 specifies "All payloads materials shall be assessed for flammability by analysis or test according to the flammability requirements in paragraphs 3.10.2 to 3.10.2.2 of SSP 51700 and JSC 29353."

9.4.10 Offgassing

a. Offgassing shall be in conformance with ESA-HRE-IPL-RQ-0002 chapter 9.2.4.

b. Offgassing testing should be performed in conformance with ECSS-Q-ST-70-29.

NOTE This is important for human spaceflight. Product Assurance and Safety Requirements for ISS Pressurized Payloads ESA-HRE-IPL-RQ-0002 chapter 9.2.4 specifies "Determination of offgassing products from materials and assembled articles shall meet the offgassing acceptance criteria in paragraph 7.7.3 of NASA-STD-6001B."

9.4.11 Solderability

9.4.11.1 Overview

The objective of the test is to verify the wettability on PTH. This is performed by floating a sample on molten solder and by assessing the rise of the solder in the PTH. Coverage of solder on the corner of a PTH is more difficult to achieve uniformly compared to an SMT pad. When the solderability test passes on PTH, it is, therefore, also expected to pass on SMT pads. Thus, the need for solderability test on SMT pads has not been identified if it is already performed on PTH.

9.4.11.2 Test vehicle

a. The test pattern for solderability test shall be one of the following:

1. Coupon A/B with PTH as specified in requirement 8.2.2c, or
2. PCB sample with PTH.

b. The coupon shall include representative PTH in accordance with ECSS-Q-ST-70-12 requirements 15.2.d2, 15.2.d4, 15.2.d.5(a) and 15.2.d8.

NOTE 1 Requirements 15.2.d2 and 15.2.d4 specify to include a representative configuration of copper planes and internal heat sink. Requirements 15.2.d.5(a) and 15.2.d8 specify to include PTH with hole sizes of maximum or most frequently used dimensions.

NOTE 2 Solderability coupon type "S" from IPC-2221B specifies dimensional parameters and need to be tailored to meet requirement b.

c. The coupon shall include minimum three PTH.

9.4.11.3 Solderability test parameters

a. The solder shall be type "63 tin solder" in conformance with table 6-1 of ECSS-Q-ST-70-08C.

b. The flux shall be type "ROL0" in conformance with table 6-2 of ECSS-Q-ST-70-08C.

c. The solder bath shall be temperature controlled in conformance with clause 7.2.3.2.2 for pretinning of ECSS-Q-ST-70-08C.

d. The tolerance of the temperature control of the solder bath shall be ±5°C.

e. The solder bath temperature shall be set at 235°C.

9.4.11.4 Test flow

a. After sampling the coupon, it shall be cleaned using a cleaning agent in accordance with clause 6.4 of ECSS-Q-ST-70-08C.

b. Bake out of the sample may be performed in conformance with the requirement 9.2.2a.

NOTE Bake out increases the intermetallic layer. However, this effect is minor compared to the pre-conditioning. Therefore bake out is not mandatory when pre-conditioning is performed, which simplifies the test flow.

c. Pre-conditioning of the sample may be performed by one of the following methods:

1. Preferred method 1: Apply a heating profile to the coupon in conformance with IPC-TM-650 2.6.27 that is representative of vapour phase reflow, or
2. Alternative method 2: 8 hours at 72°C and 85 % R.H., or
3. Alternative method 3: 80 minutes at 90°C steam ageing in conformance with clause 9.2.4.

NOTE 1 Method 1 can be simulated by 2 X 5 minutes at 230°C in an oven, which is in accordance with Table 4-2 of IPC-J-STD-003C. Method 2 is in accordance with paragraph 3.4.2. of IPC-J-STD-003C. Method 3 is in accordance with paragraph 3.4.4. of IPC-J-STD-003C. Method 1 is preferred because it provides the best simulation of reflow assembly and because of its simplicity.

NOTE 2 For method 1, the oven is set at and pre-heated to 230°C. The timing of 5 minutes is in between door openings. A forced air convection oven provides the best transfer of heat to the sample.

NOTE 3 The purpose of pre-conditioning is to simulate the vapour phase reflow that can occur on both sides of a PCB with SMT components prior to soldering of PTH. However, this preconditioning is not a mandatory part of the test flow because it is difficult to perform in a representative manner and because historically customers have not reported poor solderability on SnPb surface finish.

d. Flux shall be applied to the test area and drained on absorbent, clean material prior to solderability test.

e. The solderability test shall be performed in not less than one minute, and not more than five minutes after application of flux.

f. Dross and burned, residual flux shall be removed from the surface of the molten solder immediately prior to solderability test.

g. Solderability test shall be performed using one of the following methods:

1. Preferred method 1: float and slide the coupon gently on molten solder for 5 s, or

2. Alternative method 2: perform rotary dip test for 3 s.

NOTE 1 Method 1 is in accordance with paragraph 4.4.1 of IPC-J-STD-003C. Method 2 is in accordance with paragraph 4.2.2 of IPC-J-STD-003B.

NOTE 2 Rotary dip test is included as an alternative method because this has been used in previous standards. However, the associated non-conformance criteria were based on judging the wetting angle in a microsection. This has proven to be laborious and in some cases difficult to interpret, for instance on samples with high thermal mass.

h. Samples with a high thermal mass shall include ≥ 700 µm total copper thickness in accordance with clause 7.1.2.g of ECSS-Q-ST-70-12 or include heat sinks in accordance with clause 10.4 of ECSS-Q-ST-70-12.

i. Sample with high thermal mass shall be submitted to solderability test using one of the following methods:

   1. Preferred method 1: the coupon is floated on molten solder for a maximum duration of 30 s and the coupon can be depressed into the solder bath to a maximum of 50 % of the coupon thickness after it has been initially floated on the solder bath, or

   2. Alternative method 2: perform rotary dip test for a maximum duration of 30 s.

j. After the elapsed time, the coupon shall be removed from the molten solder and maintained still and horizontal until the solder on the coupon solidifies.

k. Prior to examination, all specimens shall have the flux removed using a cleaning agent in accordance with clause 6.4 of ECSS-Q-ST-70-08C.

l. Test specimens shall be examined at 10X magnification by visual inspection on the side that was not in contact with the solder.

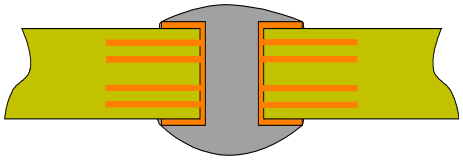
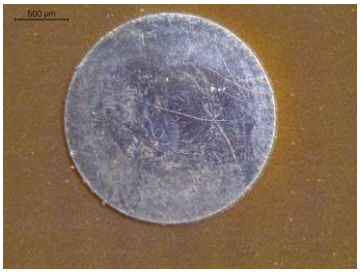
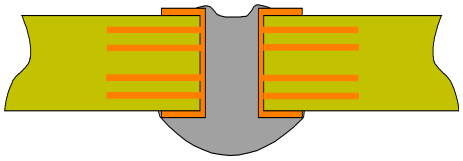
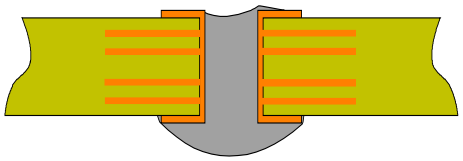
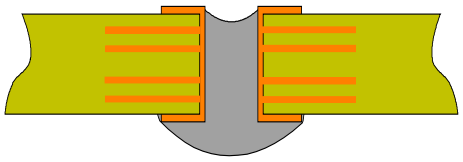
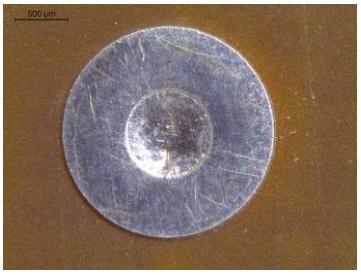
NOTE Microsectioning is not needed.

9.4.11.5 Acceptance criteria

a. Acceptance criteria for solderability of PTH shall be as specified in Table 9-1.

NOTE The non-conformance criteria are based on visual inspection. The schematic drawings of cross sections are only shown for illustration and information. The wetting angle is not evaluated in this test.

Table 9-1: Non-conformance criteria for solderability of PTH

Schematic cross section (for information)	Evaluation	Non-conformance criteria based on visual inspection
	Target condition	 Solder rises above the PTH. Corner and surface pad has been wetted.
	Acceptable	 Solder rises to the top of the PTH. Corner has just been wetted.
	Acceptable	 Solder rises to the top of the PTH on ≥80 % of the circumference. Corner has just been wetted on ≥80 % of the circumference.
	Not acceptable	 Solder does not rise to the top of the PTH on >20 % of the circumference. Corner has not been wetted on >20 % of the circumference.

9.5 Group 3 – Thermal stress and as-received

9.5.1 Overview

The solder bath test is a quick and easy test method to assess robustness of the sample under thermal stress.

Rework simulation is performed to simulate the thermal stress caused by hand solder assembly, rework and repair. The quality of the solder joint is not assessed. This test method can be tailored to be performed on SMT pads.

The rework simulation test method specifies 10 heat cycles. However, worst-case assembly, rework and repair can include more than 10 heat cycles. The stress specified by the test method covers a typical assembly process, but it does not cover worst-case. In case it is foreseen to exceed these test conditions, it is good practice to perform a specific evaluation.

A sample for rework simulation typically includes other holes for evaluation as-received.

9.5.2 Microsectioning

9.5.2.1 Method

a. The methods for microsectioning from test method 2.1.1f from IPC-TM-650 should be used.

9.5.2.2 Sampling

a. The sampling method shall not damage the area of interest to be inspected in the microsection.

NOTE For instance, milling or sawing can cause vibrations that can cause delamination. This is especially important for the rigid-to-flex interface. It is good practice to saw far away from the plane of interest and to grind to the plane of interest once the sample is potted.

9.5.2.3 Potting

a. Samples and cups for potting shall be clean.

NOTE Cleaning can be done ultrasonically with isopropanol.

b. Potting of the sample with resin shall provide edge retention.

NOTE Edge retention is achieved by using a hard resin, such as epoxy. However, also some acrylic resins can achieve good results. Acrylic resins can be preferred in an industrial environment above epoxy ones because of the faster curing time.

c. The potting should be free from air bubbles.

NOTE Absence of air bubbles can be achieved by submitting the uncured potted microsection to a vacuum or overpressure.

d. The curing of the potting resin shall not generate heat that cause damage to the sample.

e. The mixing time and ratio of the resin as specified by the supplier shall be followed.

f. Fluorescent dye should be used for potting of the rigid-to-flex interface.

g. In case fluorescent dye is not used for potting of rigid-to-flex interface, the following shall be demonstrated:

1. the efficiency to detect possible delamination without the contrast from the fluorescent dye;

2. any possible delamination is not caused by the microsectioning.

9.5.2.4 Surface preparation

a. The quality of as-polished microsections shall be free of scratches.

NOTE Examples of microsectioning and microscopy showing target quality are shown in Figure 9-5.

b. The quality of grinding and polishing of microsection shall prevent smearing of soft materials, such as copper.

NOTE 1 Smearing of copper can cover interface lines that can be indicative of adhesion defects, such as interconnect defect.

NOTE 2 It is good practice to perform grinding with incremental grit, for instance 180, 320, 800, 1200, 2500.

NOTE 3 It is good practice to perform polishing with decremental polishing paste size, for example:

- 6 µm polish pad and diamant paste, 20N, 150 rpm, 120 sec;
- 3 µm polish pad and diamant paste, 20N, 150 rpm, 90 sec;
- 1 µm polish pad and diamant paste, 20N, 150 rpm, 60 sec;
- 0,25 µm polish pad and diamant paste, 20N, 150 rpm, 45 sec.

c. Micro-etching of microsections shall be sufficient to reveal interfaces between plating steps.

NOTE 1 Adhesion defects are investigated on as-polished microsections, without the use of micro-etching. This is because micro-etching always causes an interface line to become visible between different copper plating steps. After a defect has been identified, it is useful

to micro-etch the microsection to investigate at which plating interface the defect is observed. If potential nonconformances are observed, a polish-etch-polish process can provide a more detailed investigation method.

NOTE 2 An adequate etching can be achieved, for example, by submerging the sample for 5 to 10 seconds in a solution of 25 ml demineralised water, 25 ml ammonia solution 25% and 1 ml hydrogen peroxide solution 30%.

d. The plane of the microsection should be in the centre of the hole.

NOTE 1 This is especially important for dimensional measurements.

NOTE 2 This is described in clause 3.6.1.5 of IPC-6012D and test method 2.1.1f from IPC-TM-650.

9.5.2.5 Microscopy

a. Quality of metallisation shall be inspected in bright field.

NOTE Bright field achieves the best contrast in the metallised areas.

b. Quality of laminate shall be inspected in dark field or an equivalent lighting method.

NOTE 1 Dark field uses a high illumination intensity showing features underneath the surface of the microsection by transparency of the resin. A similar high illumination intensity can be obtained using polarisation filters.

NOTE 2 Subsurface cracks in laminate can be visible as an area showing “iridescence” in dark field. To conclude on the nature of the iridescence it is good practice to perform progressive polishing to have the surface of the microsection at the same level of the feature. In this case a crack shows up in bright field since it is in the surface of the microsection.

c. The magnification for microscopic inspection may be 50x to 1000x.

d. The specific magnification for microscopic inspection for each acceptance criteria shall be as specified in clause 10.

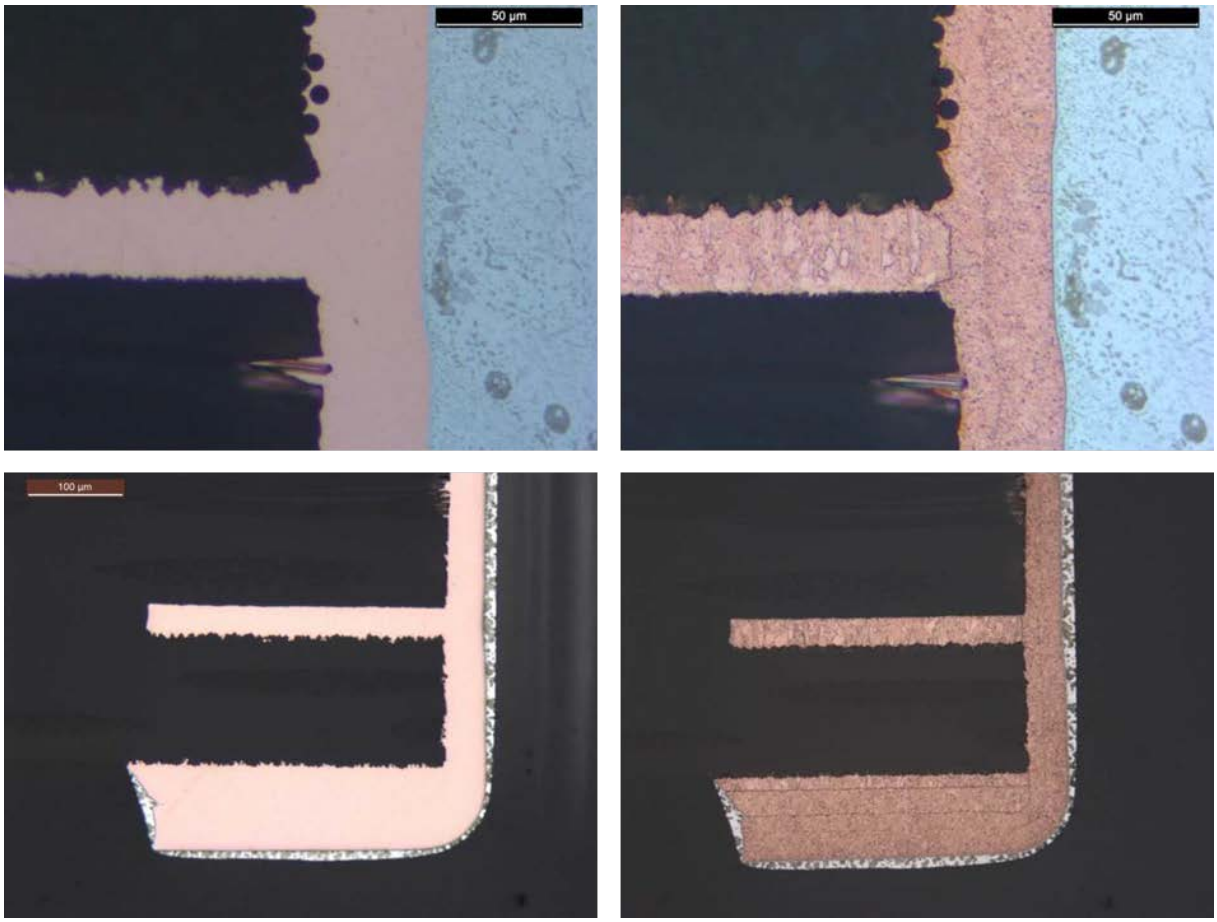


Figure 9-5: Example of target quality of microsection of innerlayer (top) and knee of the hole (bottom), as-polished (left) and after micro-etch (right).

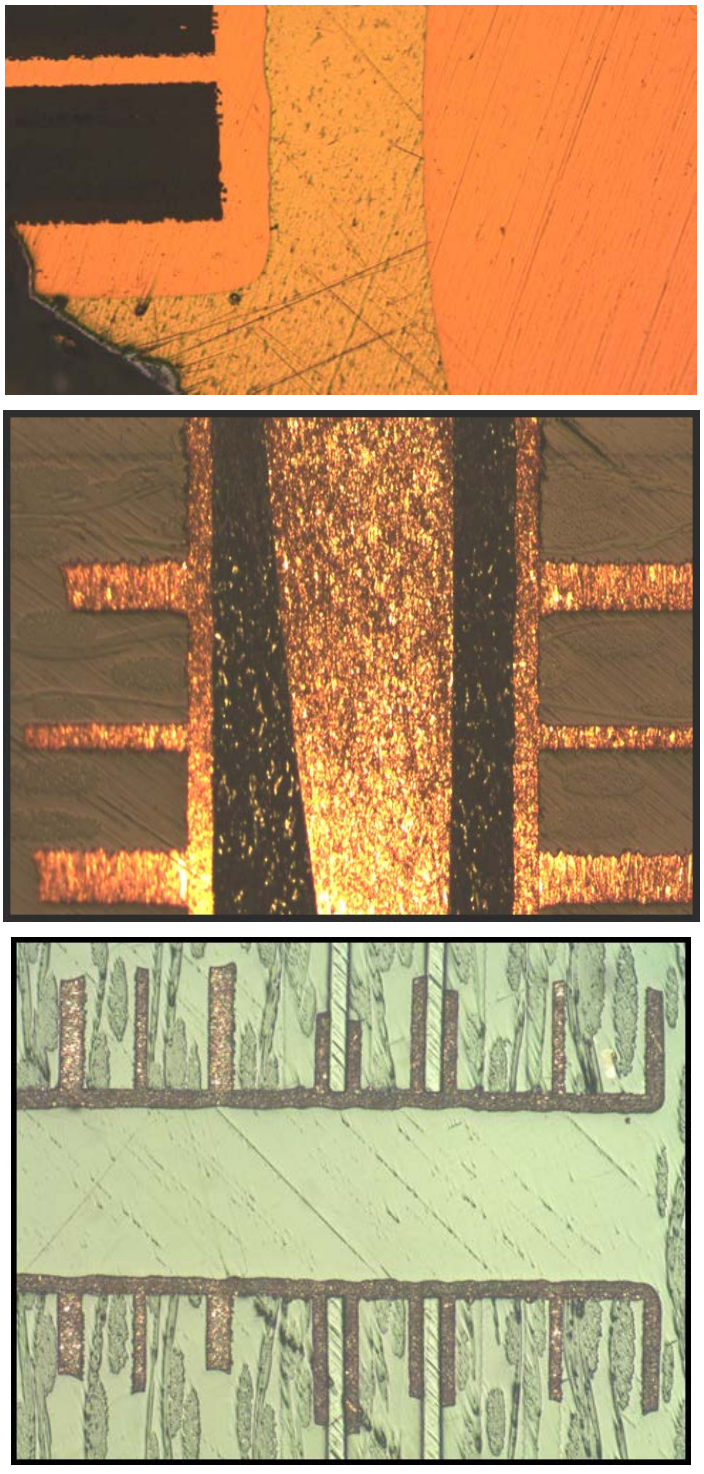


Figure 9-6: Examples of inadequate quality of microsection showing in the top image inadequate polishing, leaving scratches on surface, in the middle image over-etched sample and in the bottom image inadequate lighting, revealing no detail on metallisation, nor on laminate by transparency.

9.5.3 Solder bath float

a. The test shall be carried out in conformance with condition A of test method 2.6.8e of IPC-TM-650.

b. Samples shall be baked in conformance with clause 9.2.2.

c. The solder bath float shall be performed to one side of the sample by floating it for 10 s in a solder bath maintained at 288°C.

d. The sample shall be removed from the bath and cooled down to ambient conditions for a duration of at least 2 minutes.

e. The solder bath float and cool down from requirements 9.5.3c and 9.5.3d shall be repeated 3 times.

NOTE The acronym for the solder bath floating test is "SB". This acronym refers to this test method which specifies 3 cycles. Thus, "SB" does not imply only 1 heat cycle.

f. The samples shall be inspected to ensure that holes are wetted.

g. The samples shall be inspected to evaluate any damage to the substrate.

h. The samples shall be microsectioned for evaluation of integrity of plating and dielectric in conformance with clause 10.

9.5.4 Rework simulation

9.5.4.1 Test vehicle

a. The test pattern for rework simulation test shall be one of the following:

1. Coupon A/B with PTH as specified in requirement 8.2.2c, or
2. PCB sample with PTH.

b. The coupon shall include representative PTH in accordance with ECSS-Q-ST-70-12 requirements 15.2.d.5a and 15.2.d.8.

NOTE These clauses specify to include PTH with hole sizes of maximum or most frequently used dimensions.

9.5.4.2 Rework simulation test parameters

a. The solder shall be type "63 tin solder" in conformance with table 6-1 of ECSS-Q-ST-70-08C.

b. The flux should be type "ROL0" in conformance with table 6-2 of ECSS-Q-ST-70-08C.

c. The solder iron and solder tip shall in conformance with clause 5.6.7 of ECSS-Q-ST-70-08C

NOTE To meet requirement 5.6.7.e. of ECSS-Q-ST-70-08 it is good practice to use a solder iron with a power of ≥ 80W.

d. The solder tip temperature shall be set at 350°C.

NOTE This temperature covers the maximum temperature in conformance with requirement 5.6.7h of ECSS-Q-ST-70-08 for epoxy and polyimide technology without large thermal mass. For polyimide technology with thermal mass, requirement 5.6.7j of ECSS-Q-ST-70-08 allows a higher soldering temperature of 380°C. This is not covered by the rework simulation test using the specified conditions.

9.5.4.3 Test flow

a. Bake out of the sample shall be performed in conformance with the clause 9.2.2.

b. Copper wires should have a diameter of 0,2 mm to 0,7 mm smaller than the diameter of the PTH.

c. Copper wires may be solid wire or stranded wire.

d. The wire and PTH shall be fluxed.

e. The wire shall be pretinned.

f. The wire shall be inserted in the PTH and soldered.

g. During soldering the tip of the solder iron shall be in contact with the pad of the PTH and the wire for a maximum duration of 5 seconds.

h. Sample with high thermal mass should be submitted to pre-heating during the rework simulation test.

NOTE This is done to limit the soldering time to maximum 5 seconds.

i. After soldering, the sample shall be allowed to cool down for at least 30 s.

j. Additional flux shall be applied after the cool down, just prior to the next solder cycle.

k. While the solder is molten in conformance with requirement 9.5.4.3g, the wire shall be moved by at least 5 mm.

NOTE It is good practice not to remove the wire from the PTH and not to re-insert during subsequent solder cycle. This is done to avoid mechanical stress, which is considered to be less reproducible and dependant on operator and dimensions of wire and PTH. The test method is intended to impose thermal stress only. However, removal of wire can be optionally performed but this only provides a conclusive outcome if results are positive.

l. Clauses 9.5.4.3i, 9.5.4.3j and 9.5.4.3k shall be repeated 10 times in total.

NOTE 1 The wire is left inside the PTH.

NOTE 2 The acronym for the rework simulation is “RW”. This acronym refers to this test method

which specifies 10 cycles. Thus, "RW" does not imply only 1 heat cycle.

m. A microsection shall be performed on the soldered hole including the wire to evaluate the integrity of plating and dielectric in conformance with clause 10.

9.5.5 Interconnect stress test (IST)

9.5.5.1 Overview

IST testing is a test method that performs rapid thermal cycling on IST coupons. The IST coupons are daisy-chained vias with power circuits through which a current is applied to heat the IST coupon and sense circuits that are used to monitor the resistance change as function of thermal cycling.

PCB technology of highest complexity or with aspects that are expected to affect thermal endurance are IST tested within the technology perimeter for procurement as specified in 9.5.5.2.2. In addition, in-process IST testing as well IST testing for qualification is performed. The thermal endurance of PCB technology that does not fall within the technology perimeter as specified in 9.5.5.2.2 is, therefore, covered by the in-process IST verification.

9.5.5.2 Technology perimeter

9.5.5.2.1 In-process control

a. The PCB manufacturer shall have a work instruction for in-process IST control.

b. In-process IST control shall enable quantification of the reliability and monitoring of the stability.

c. The PCB manufacturer shall specify the IST coupon design and IST test method to be used.

NOTE This can deviate from the IST test parameters from clause 9.5.5.4.

d. The work instruction for in-process IST control shall specify the following:

1. The technology, build-up and design reference of the IST coupon;
2. The rationale for the IST coupon design based on the PID;
3. IST test parameters;
4. Test moment and frequency;
5. Statistical Process Control (SPC) limits.

NOTE A typical frequency of testing is once per week or two weeks.

9.5.5.2.2 Procurement

a. IST shall be performed for procurement in case the PCB definition dossier includes one or more of the following:

1. Any PCB with ≥ 0.3 mm in z-direction of no-flow prepreg or 85NT;

   NOTE No-flow prepreg and 85NT have high thermal expansion in z-direction. The thermal expansion is the driver for barrel crack and therefore necessitates IST testing.

2. Rigid epoxy PCB with ≥ 12 copper layers;

3. Rigid-flex PCB with one or more of the following aspects:

   (a) ≥ 12 copper layers, or

   (b) ≥ 2 flex laminates, or

   (c) asymmetric build-up or asymmetric lamination;

4. HDI PCB with microvias or with aspect ratio > 7.

b. At least one coupon shall be included per panel and submitted to IST testing.

9.5.5.2.3 Qualification

a. IST shall be performed for qualification activities in conformance with clause 7.2.

b. IST shall be performed until 5% resistance increase is reached or until a maximum of 1500 cycles.

   NOTE 1 Acceptance criteria are as per clause 9.5.5.4.3. Testing to EOL is performed to provide information about the limits of the robustness.

   NOTE 2 At least 3 IST coupons are used for initial qualification and at least 1 IST coupon is used for delta qualification and qualification renewal, in conformance with clause 5.6.

   NOTE 3 For qualification it is not practical to test microvias after having tested other via types on that coupon to EOL.

9.5.5.3 IST coupon design and location on panel

a. The IST coupon design shall be type “X”.

   NOTE 1 For instance “TVX” or “SLX”. This indicates the presence of an internal (‘P’) and external (‘H’) heating circuit..

   NOTE 2 An IST coupon typically includes two power circuits (H and P) and two sense circuits (S1 and S2). One sense circuit can include more than one plating sequence. In some cases more than one IST coupon is needed to represent all vias and plating sequences.

   NOTE 3 The sense circuit is typically designed to be sensitive to barrel crack. The power circuit applies heat to the coupon and in addition it is typically designed to be sensitive to

interconnect defect. The standard power circuit is applied through interconnects on 4 internal layers. These therefore are assessed by IST, whilst other layers remain unassessed. In case the need arises for more comprehensive assessment of interconnections of all layers, PWB Corp can be requested to design specific coupons.

b. IST coupon design shall be representative of the PCB for the following features:

1. minimum drill diameter;
2. minimum drill pitch for the via type;
3. all plating sequences, except for the case 9.5.5.3c;
4. pad diameter;
5. copper foil thickness;
6. presence of NFP;
7. layer function for signal or plane;
8. diameter of clearance holes in planes.

NOTE 1 An IST coupon design work sheet is available on the test equipment supplier's website www.pwbcorp.com that includes these items.

NOTE 2 Space PCBs typically use SnPb surface finish. During IST testing it has been observed that SnPb enters into barrel cracks and crack initiations. This can accelerate crack growth due to wedging. This can also mask or delay resistance increase. Therefore SnPb finish can be stripped and bare copper coupons can be tested. Studies have shown correlation between both configurations.

NOTE 3 Multiple coupons can be necessary to accommodate IST on all plating sequences.

c. The plating sequence to manufacture a buried via across top and bottom layer of a single laminate need not to be included in the IST coupon.

d. The coupon should be located as close as possible to the PCB.

e. In case of more PCBs per panel, the coupon should be located as close as possible near the centre of the panel.

f. The coupon should not be located in the corner of the panel.

NOTE This is done to be representative of worst-case Cu coverage. Location of IST coupon on the panel is shown in Figure 8-2.

9.5.5.4 IST test method

9.5.5.4.1 Preparation

a. Electrical pre-screening and possible down selection should be performed in conformance with instruction PWB-150316 in case multiple IST coupons are available.

NOTE The referenced work instruction is available on the website of the test equipment supplier.

b. Bake-out of IST coupons shall be performed in conformance with requirement 9.2.2a.

c. After bake-out, connectors shall be soldered to the IST coupon.

d. Reabsorption of humidity in IST coupons should be prevented in conformance with requirement 9.2.2d.

e. Correct soldering of connectors should be verified by measuring again the resistance of IST coupons.

f. In uncontrolled conditions, IST coupons shall be submitted to IST testing within 12 hours after baking.

g. In case re-absorption of humidity is mitigated in conformance with point 9.5.5.4.1d, IST coupons need not to be submitted to IST testing within 12 hours after baking.

9.5.5.4.2 IST test parameters

a. IST shall be performed in conformance with test method 2.6.26A from IPC-TM-650, except for the parameters specified in this clause 9.5.5.4.2.

b. The IST preconditioning cycles should be 6 times to 230 °C.

c. The IST preconditioning cycles may be tailored in case the following conditions are met:

1. The IST preconditioning cycles are representative of the assembly environment and potential repair and rework;
2. The IST preconditioning cycles are minimum 3 times to 230 °C.

d. The power circuit for preconditioning shall be the “superheat” circuit

NOTE Superheat circuit is identified by “H”.

e. IST cycling shall be performed to the following temperature limits:

1. polyimide: 170°C;
2. epoxy: 150°C;
3. microvias on polyimide: 210°C;
4. microvias on epoxy: 190°C.

f. Failure threshold of resistance change shall be 5 % for standard holes.

NOTE In case a resistance below 250 mΩ is measured during electrical pre-screening, in conformance with 9.5.5.4.1a, the noise can be high. In this case it is good practice to confirm the failure

threshold with the test equipment supplier. This can result in re-design of the coupon for future use.

g. Failure threshold of resistance change shall be 4 % for microvias.

h. The failure threshold for resistance change shall apply to all circuits on the IST coupon.

NOTE 1 A failure on the internal power circuit indicates a weak interconnection. This is not the typical failure mode in an IST test. This can cause local over-temperature due to high resistance.

NOTE 2 A failure on the sense circuit indicates barrel crack. This is the typical failure mode in an IST test. This does not cause local over-temperature because this circuit is passive.

i. "Compensation" shall be "Calculated" for standard tests.

j. "Compensation" shall be "None" for microvia testing and for testing standard vias with a pitch of ≥ 2.5 mm.

k. "Sense Fail Type" shall be "A or B".

l. The power circuit for IST cycling shall be the internal power circuit.

NOTE 1 The internal power circuit is identified by "P".

NOTE 2 IST cycling includes the first few IST cycles before preconditioning and all IST cycles after preconditioning.

m. For testing microvias, the power cable shall be connected directly to the microvias sense circuit.

NOTE The sense cable is connected to a power or sense circuit that has previously demonstrated to be robust, e.g. the superheat circuit. The measured sense data is not considered important and any failure or variation measured is disregarded.

9.5.5.4.3 IST acceptance criteria

a. Any coupon shall have an IST endurance of ≥ 400 cycles for standard holes.

b. Any coupon shall have an IST endurance of ≥ 100 cycles for microvias.

c. Any coupon should have an IST endurance of ≥ 400 cycles for microvias.

NOTE IST testing of microvias can be performed after IST testing of standard holes in case both hole types are present on the same coupon. The IST cycles for standard holes occur to a lower temperature, which does not impact the IST performance of the microvia circuit tested subsequently.

9.5.5.4.4 Analysis and reporting

a. After IST testing, the coupon should be submitted to microsectioning.

b. In case the required number of IST cycles are not achieved, the coupon shall be submitted to microsectioning to investigate the cause of failure and possible corrective actions.

c. The location for microsectioning should be determined by observing the hotspot during infrared thermography while a small current is passed through the failed circuit.

NOTE 1 The purpose is to get a visual confirmation of the failure mechanism in the metallisation. Barrel crack, wear-out of the copper barrel and innerlayer separation should be the main focus of this inspection.

NOTE 2 In case tin-lead is included on the IST coupon, it is good practice to verify the absence of tin-lead in barrel cracks by microsectioning, as this can impact the measured IST endurance. An example of this is shown in Figure 9-7.

d. The IST test report shall include the following:

1. Summary of test parameters;
2. Reference to the coupon design drawing;
3. Graph of resistance change as function of IST cycles.

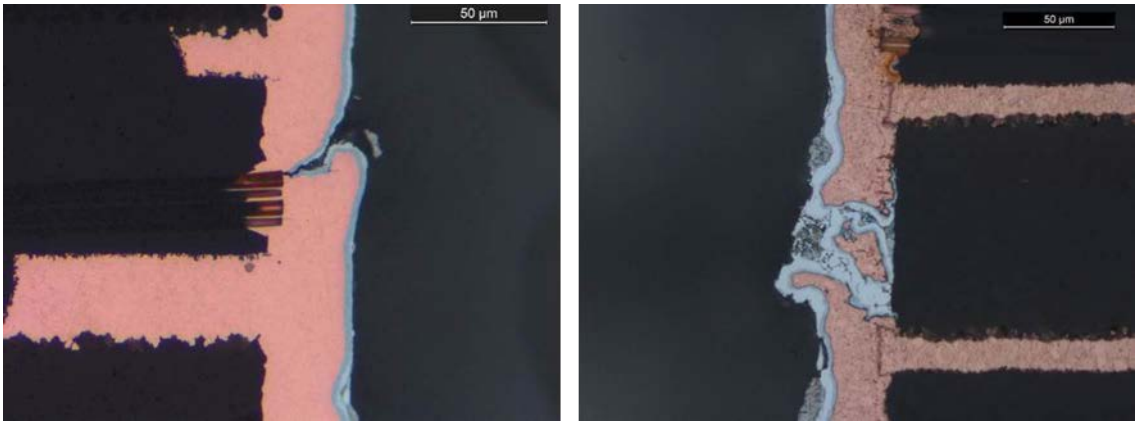


Figure 9-7: Examples of barrel cracks after IST testing showing a nominal crack size (left) and a large crack filled with SnPb (right)

9.5.5.5 Special IST test for RF PCB technology

9.5.5.5.1 Overview

Standard IST coupon design includes interconnects on L2+3 (and Ln-1 and Ln-2) in the power circuit. The sense circuit is designed to be sensitive for barrel crack, as it includes no innerlayer connections. For special technology, this design can be modified to have better sensitivity for interconnects on critical layers. This is of value in case laminate materials are used that are prone to

smear, such as PTFE based materials for RF PCBs. Smear can be impacted by drill size and drill bit quality.

9.5.5.5.2 IST coupon design for interconnect verification in RF PCBs

a. Normal IST coupons shall be included for RF PCB in case this is within the technology perimeter in conformance with 9.5.5.2.2a.

NOTE Normal IST coupons evaluate mainly barrel strength.

b. Specific IST coupons for interconnect verification may be included for RF PCB technology to assess smear.

c. Specific IST coupons for interconnect verification should include all drill sizes for holes that interconnect on RF laminate.

NOTE This does not include non-functional pads.

d. The daisy-chain should include the largest drill diameter for holes that interconnect on RF laminates.

NOTE Interconnection in large holes are most stressed during IST cycling.

e. The daisy-chain should include interconnection on all RF innerlayers.

f. The daisy-chain should include interconnection on outermost RF innerlayers.

NOTE 1 This is for example L2, L3, Ln-1 and Ln-2.

NOTE 2 The interconnects on outermost innerlayers are most stressed during IST cycling.

g. The power cable should be connected to the superheat circuit.

NOTE This circuit is not affected by the quality of interconnects and provides a stable heat source.

h. The IST cycling may be performed to a temperature of 210°C.

NOTE The high temperature is recommended to provide sufficient stress to the interconnections on thermally robust PTFE layers. The possible presence of low Tg laminate needs to be evaluated, but is not deemed critical to this test temperature as sensitivity to barrel strength is designed to be low.

9.6 Group 4 – Assembly and life test - extended

9.6.1 Overview

ECSS-Q-ST-70-10 group 4 included thermal cycling. This is superseded by the accumulative test flows of group 4 and group 6 described in this clause and in clause 9.8.

Group 4 includes a higher number of 500 thermal cycles with a lower temperature range of 155 °C. In addition, group 4 includes electrical testing and

peel strength. The group 4 is performed for initial qualification of a material or technology and provides evidence that the PCB technology withstands the thermal excursions from assembly verification, in conformance with requirement 13.3.d of ECSS-Q-ST-70-08 and 14.6 of ECSS-Q-ST-70-38. See clause 9.8.1 for an overview of group 6.

9.6.2 Test flow for group 4

a. The test vehicle for group 4 shall include the PCB.

b. The test vehicle for group 4 shall include coupons that are specified for each test method.

c. The following test steps shall be performed for group 4 in this order:

1. bake-out in conformance with clause 9.2.2;
2. intralayer and interlayer insulation resistance with AC and DC voltage in conformance with clause 9.6.3;
3. intralayer and interlayer dielectric withstanding voltage with AC and DC voltage in conformance with clause 9.6.4;
4. reflow simulation in conformance with clause 9.8.3;
5. rework simulation on at least 4 PTH of the PCB in conformance with clause 9.5.4;
6. thermal cycling in conformance with clause 9.8.4 with the following modifications:
   (a) for requirement 9.8.4g the minimum temperature is -55°C;
   (b) for requirement 9.8.4h the maximum temperature is +100°C;
   (c) for requirement 9.8.4i the temperature range is 155°C;
   (d) for requirement 9.8.4j the number of thermal cycles is 500;
7. intralayer and interlayer insulation resistance with AC and DC voltage in conformance with clause 9.6.3;
8. intralayer and interlayer dielectric withstanding voltage with AC and DC voltage in conformance with clause 9.6.4;
9. peel strength in conformance with clause 9.4.1;
10. microsectioning in conformance with clause 9.5.2;
11. evaluation of acceptance criteria in conformance with clause 10.2.

d. Microsectioning and evaluation in conformance with 9.6.2c.10 and 9.6.2c.11 shall be performed on the following:

1. At least 4 PTH from the PCB that have been subjected to rework simulation;
2. All technology features under qualification.

NOTE Technology features under qualification can include all via types, the build-up and materials.

e. Interconnection resistance on a daisy-chain coupon may be monitored during thermal cycling.

f. In case a daisy-chain coupon is used in conformance with requirement e, change of interconnection resistance shall be ≤ 10%.

g. The daisy-chain coupon may be an IST coupon.

NOTE 1 Continuous in-situ measurement using four-wire resistance is commonly performed on coupons in a thermal cycling chamber. The daisy-chain is designed with sufficient length to allow a sensitive measurement.

NOTE 2 This evaluation can provide correlation of traditional chamber thermal cycling with IST cycling by continuous measurement of interconnection resistance on the same pattern. It can also quantify the electrical performance of a thermally stressed daisy-chain by measuring before and after the group 4 test flow.

NOTE 3 Rework simulation is only performed on the PCB. It is not performed on coupons for insulation resistance, dielectric withstanding voltage, IST or peel strength.

9.6.3 Insulation resistance

a. The insulation resistance test shall be performed in conformance with tests 6a for external intralayer insulation resistance, test 6b for internal intralayer insulation resistance and test 6c for interlayer insulation resistance of IEC 60326-2-am 1 (1992-06).

NOTE This test is superseded by the high resistance electrical test on PCB. However, insulation resistance is still measured on coupons before and after environmental testing.

b. A direct voltage of 250V shall be applied between the two closest conductors that are not electrically connected.

NOTE Table 13-3 and table 13-4 of ECSS-Q-ST-70-12 allow, for instance, a minimum conductor spacing of 200 µm on external layers without conformal coating, 81 µm on internal layers for HDI and 25 µm between layers on flex laminate.

c. Test voltage shall be DC for qualification activities.

d. The procurement authority may define in the PCB definition dossier specific AC insulation resistance testing on coupons or PCB.

NOTE 1 The majority of applications for space are in DC. It is important to note that DC/DC converters can have some AC sections.

NOTE 2 Peak transient voltages in AC or DC is covered by requirement 13.8.2.b from ECSS-Q-ST-70-12.

NOTE 3 The failure mechanisms of primary concern in PCB materials are of slow time constant, such as ECM. In this case, DC is deemed worse-case than AC.

e. When the voltage is applied, the insulation resistance (R) shall be measured after 1 minute, except the case specified in 9.6.3f.

f. In case a stable reading is obtained earlier, the insulation resistance (R) may be measured before 1 minute.

g. The test pattern for intralayer insulation resistance shall have at least 25 mm parallel conductors.

NOTE Insulation distance between tracks or between layers is representative of the PCB, as specified in clause 15.2a of ECSS-Q-ST-70-12.

h. The test pattern for interlayer insulation resistance shall have at least 1 cm^2 superimposed conductors.

NOTE Test coupon E of IPC-2221B can be used for intralayer insulation resistance. For interlayer insulation resistance, test coupon E is modified as per requirement 9.6.3h.

i. The intralayer insulation resistance as received shall be ≥ 10 GOhm.

j. The interlayer insulation resistance as received shall be ≥ 100 GOhm.

k. The intralayer insulation resistance after thermal stress shall be ≥ 1 GOhm.

l. The interlayer insulation resistance after thermal stress shall be ≥ 10 GOhm.

NOTE To measure such high resistance it is recommended to use an equipment with a measurement range up to 1000 GOhm.

9.6.4 Dielectric withstanding voltage (DWV)

a. The test shall be carried out in conformance with IPC-6012D chapter 3.8.1 and condition B of test method 2.5.7d of IPC-TM-650.

NOTE 1 This method specifies 1000 V DC for 30 s. The procurement authority can define specific AC testing on coupons or PCB as specified in requirement 9.6.3d.

NOTE 2 PCB qualification does not cover for continuous operation of the assembled PCB at any voltage, which is typically performed at unit level. Bare PCBs are not subject to tests and requirements for rating and derating.

b. For interlayer measurements the test voltage shall be applied between two superimposed conductors with a surface area of ≥ 1 cm^2.

c. For intralayer measurements the test voltage shall be applied between two adjoining, but not electrically connected conductors within the same layer with a total length of ≥ 25 mm.

NOTE Insulation distance between tracks or between layers is representative of the PCB, as specified in clause 15.2a of ECSS-Q-ST-70-12.

d. Visual inspection shall show no evidence of breakdown, flashover or sparking.

NOTE 1 Test coupon E of IPC-2221B can be used for intralayer DWV. For interlayer DWV, test coupon E is modified as per requirement 9.6.4b.

NOTE 2 Advanced test equipment are capable to monitor voltage or leakage current continuously during the applied test voltage. A sudden drop in voltage is indicative of a discharge. This is relevant because visual inspection is not fully efficient on internal layers covered by plane layers.

9.7 Group 5 – ECM tests

9.7.1 Overview

Group 5 in ECSS-Q-ST-70-10 included a damp heat test. This is superseded by the THB and CAF tests specified in this clause.

The THB test has the objective to assess the cleanliness of the sample, which includes cleanliness of raw laminate and cleanliness of PCB manufacturing processes. The adhesion of resin to, for instance, fibre contamination can be degraded during thermal stress of assembly, such as vapour phase reflow. Fibre contamination can provide a pathway for ECM. Because of the relatively large particle size of typical contamination, this type of ECM is possible for PCB designs using standard insulation distance.

The CAF test has the objective to assess the material properties for its CAF resistance. The adhesion of resin to glass fibre reinforcement can be degraded during thermal stress. The glass-to-resin interface, or a hollow glass fibre, can provide a pathway for ECM. The CAF mechanism is only probable at small insulation distance, as for HDI designs. The CAF test can also detect contamination as for the THB test, but this is not its objective.

The environment of THB and CAF tests include a temperature of 85 °C because this is the maximum operational temperature for which PCBs are qualified in conformance with requirement 5.1b. The tests include a relative humidity of 75% RH because this provides some margin and acceleration of test compared to the maximum relative humidity of 65% in clean rooms. However, it is

possible that PCB assemblies are tested or operated at higher humidity outside of cleanrooms.

Ground-based testing at unit level is deemed the worst-case environment for a potential ECM because of the presence of humidity in the atmosphere. However, studies have shown that the time constant of desorption of humidity from the somewhat hygroscopic laminate can be underestimated significantly in the presence of ground-planes and other complex PCB geometry.

9.7.2 Temperature, Humidity, Bias (THB)

9.7.2.1 General

a. A justification shall be provided in case any part of this test method is tailored.

NOTE The specified method can be superseded by future test campaigns to implement lessons learned or to represent applications.

9.7.2.2 Test vehicle

a. The lay-out of the test vehicle for THB test shall meet the following conditions:

1. It includes two comb patterns in x and y direction on each internal layer;
2. It includes 150 µm as-designed insulation distance D between tracks;
3. Each comb pattern covers an area of ≥ 30x30 mm;
4. The sensitivity of the pattern is ≥ 20000 number of squares.

NOTE 1 An example of a test vehicle for THB testing is shown in Figure 9-8.

NOTE 2 150 µm as-designed can result in minimum 120 µm as-manufactured.

b. The sensitivity S of the pattern shall be as follows

$$S = L \times N / D$$

L length of track

N: number of gaps between tracks

D: insulation distance

NOTE 1 The unit of the sensitivity is “number of squares”. This is a dimensionless value representing the interface area, that is proportional to the sum of the length of parallel tracks and inverse proportional to the insulation distance.

NOTE 2 The pattern in Figure 9-8 uses 150 µm track width and 150 µm insulation distance over an area of 30 mm length and width. This results

in 30/(0.15+0.15)=100 gaps N. Therefore the sensitivity S= 30 x 100 / 0.15 = 20000 number of squares.

c. The THB test shall assess internal layers.

d. The build-up of the test sample shall include ≥ 8 copper layers, uni-flow prepreg, no-flow prepreg, flex laminate and rigid laminate materials in conformance with the PID.

NOTE An example of the build-up is shown in Figure 9-9.

e. The thickness shall be 1.6 mm ± 10% over connector metallisation.

f. The manufacture of samples shall follow the process flow as specified in the PID including the manufacture of windows in no-flow prepreg as for rigid-flex PCBs.

NOTE Manufacture of windows and use of various materials are sources of contamination which are aimed to be included in the test vehicle.

g. Copper foil thickness shall be 35 µm.

h. Surface finish on connector shall not be SnPb

NOTE This is specified because SnPb can contaminate the connector pins on the test rack. Alternative finishes, such as galvanic Au and/or Ni or ENEPIG do not show this problem. External layers and surface finish is not within the scope of the test method.

i. In total four samples shall be tested from at least two different panels.

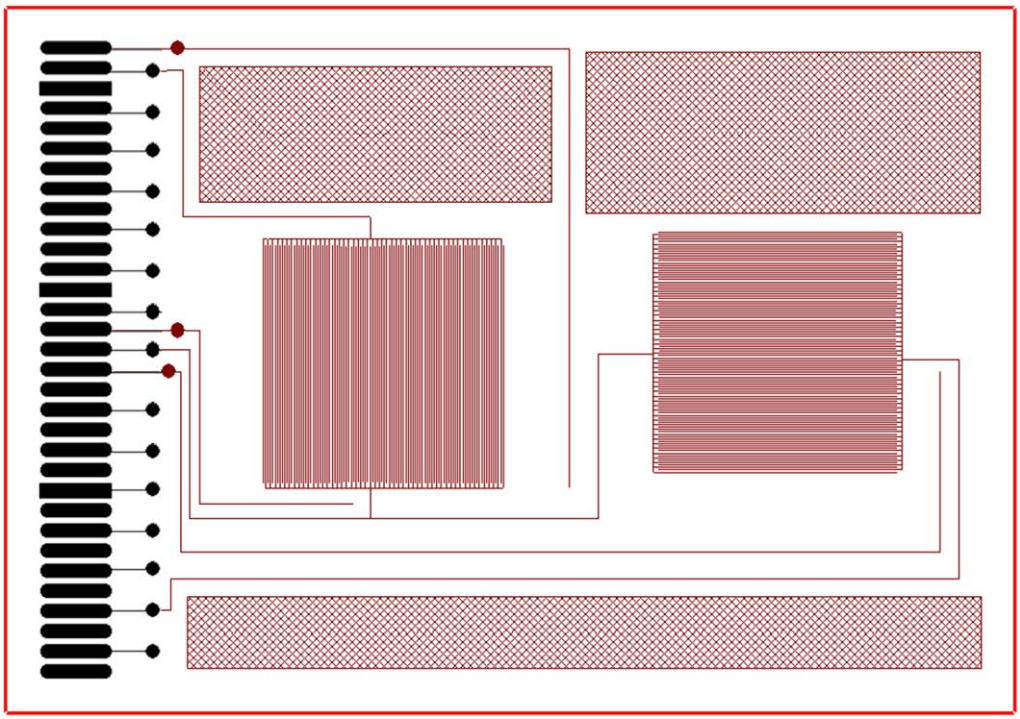


Figure 9-8: THB test pattern

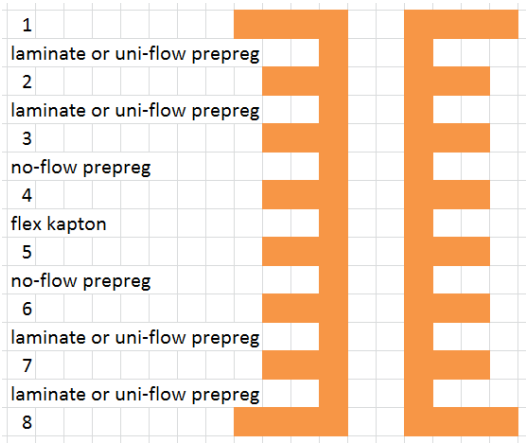


Figure 9-9: Build-up for THB test vehicle

9.7.2.1 Test method

a. The sample preparation method shall be as follows:

1. bake-out in conformance with clause 9.2.2;
2. two times reflow simulation in conformance with clause 9.8.3;
3. ultrasonic cleaning followed by bake-out in conformance with clause 9.2.2.

NOTE 1 Reflow simulation is performed to represent assembly environment and because the high temperature can carbonise contaminants or can weaken the adhesion between resin and contaminant.

NOTE 2 Ultrasonic cleaning can be performed in IPA. This is done to ensure clean surfaces in the connector pattern.

b. The THB method shall be as follows:

1. THB Ambient using the parameters: 24h, 25°C, 50 %RH, 50V;
2. THB ECM using the parameters: 150h, 85°C, 75 %RH, 50V;
3. THB Ambient using the parameters: 24h, 25°C, 50 %RH, 50V.

NOTE 1 The THB Ambient part is done to determine ambient insulation resistance prior to and after the THB ECM part. This verifies that any failures during the THB ECM part persist after returning to ambient conditions.

NOTE 2 It is good practice to verify that changes in the environmental chamber do not cause high humidity or condensation on samples. From Ambient to ECM, this is achieved by increasing temperature prior to increasing RH. From ECM to Ambient this is achieved by decreasing RH prior to decreasing temperature and by using a slow rate of temperature change.

c. During THB Ambient and THB ECM insulation resistance of all patterns shall be measured periodically using an electrometer capable of measuring high resistances combined with a switchbox, while maintaining the bias voltage.

NOTE The AutoSIR equipment can perform this task.

d. Acquisition rate shall be at least once in 10 minutes.

NOTE A faster acquisition rate is good practice to be able to detect transient changes.

e. After THB test, samples shall be microsectioned to determine the cause of a breach of insulation resistance.

NOTE 1 It is good practice to perform horizontal microsectioning just adjacent to the layer that has failed. After that, cross sectioning can be performed in addition to provide better visibility of the failure site.

NOTE 2 Infrared thermography can be performed, possibly using "lock-in" technique, to determine the failure location in x,y direction. The location in z-direction is known because each layer is acquired individually. It is good practice to ensure that the voltage used during thermography is not higher than the test voltage during THB and that the current does not heat up and damage the failure site. Instead of failure location using thermography, the whole 3x3 cm pattern can be included in horizontal microsectioning. This minimizes the risk of damage due to heat and it is relatively simple to perform microscopy on such sample area.

f. It shall be determined if a breach of insulation occurred in prepreg or in laminate layers.

NOTE The cleanliness of prepreg layer is under control by the PCB manufacturer. The cleanliness of laminate layers is under control by the laminate supplier.

9.7.2.2 Acceptance criteria

a. A sudden drop in resistance by an order of magnitude shall be breach of insulation.

NOTE Breach of insulation can occur intermittent or continuous. Examples of stable insulation and breach of insulation are shown in Figure 9-10.

b. Breach of insulation that is demonstrated by microsectioning to be caused by lack of cleanliness shall be evaluated during the audit in conformance with clause 6.6.

NOTE The test can only be treated as nonconform in case contamination is demonstrated to be the cause of breach of insulation. The electrical response only, is not sufficient. Hence, it is not necessary that the environmental parameters are fully representative of operational use. The test only serves to find contamination, if any. Test results of contamination causing breach of insulation are evaluated together with the cleanliness of processes during the audit.

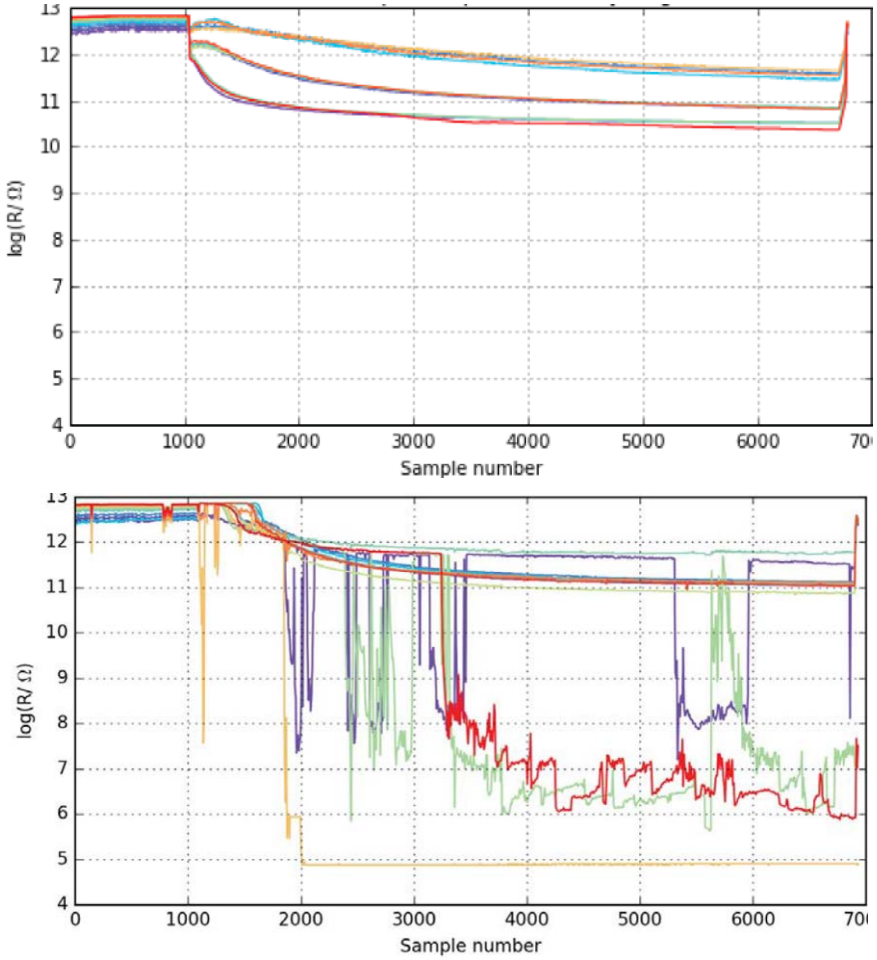


Figure 9-10: Insulation resistance during THB Ambient (until sample nr 1000) and THB ECM showing continuous breach of insulation on 4 patterns in the lower graph. The top graph shows stable insulation.

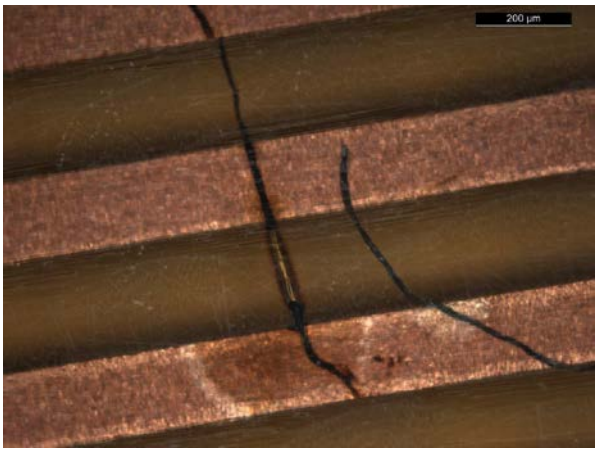


Figure 9-11: Horizontal microsection showing fibre contamination on tracks in prepreg resin causing breach of insulation.

9.7.3 Conductive Anodic Filament (CAF)

9.7.3.1 General

a. A justification shall be provided in case any part of this test method is tailored.

NOTE The specified method can be superseded by future test campaigns to implement lessons learned or to represent applications.

9.7.3.2 Test vehicle

a. The lay-out of the test vehicle for CAF test shall meet the following conditions:

1. It includes the pattern configuration A as specified in Table 9-2for aligned vias using ≥20x20 vias configured in x and y direction;
2. It includes the pattern configuration B as specified in Table 9-3 for staggered vias using ≥10x20 vias;
3. It includes the pattern configuration C as specified in Table 9-4 for vias in plane using ≥20x20 vias with all non-functional pads removed;
4. Electrical registration coupons in x and y direction for verification of registration.

NOTE 1 For requirement 9.7.3.2a.1 such comb pattern of aligned vias result in 20 vias x 19 spacing = 380 CAF opportunities within a layer.

NOTE 2 For requirement 9.7.3.2a.2 such comb pattern of staggered vias result in 10 vias x 19 spacings x 2 manhattan paths = 380 CAF opportunities within a layer.

NOTE 3 For requirement 9.7.3.2a.3 the C pattern of vias-in-plane is used to represent via-to-track.

The non-functional pad is removed on all layers, otherwise the failure mechanism can be as for the configuration conductor-to-conductor.

NOTE 4 For requirement 9.7.3.2a.3 C pattern is designed with bias voltage connected to the vias. Therefore the vias are positive, i.e. the anode. CAF grows from the anode, hence CAF can grow from the via, which is the purpose of this test pattern design.

NOTE 5 For requirement 9.7.3.2a.4 test pattern A is deemed to be most susceptible to CAF.

NOTE 6 For requirement 9.7.3.2a.4 laser drilled microvias give less propensity for CAF compared to mechanical vias, because:

- smaller diameter and smaller contact area to glass
- less desmear
- less vibrations during hole wall formation

Based on this, testing a mechanical via is considered representative or slightly worse-case of a microvia. For microvia, the critical spacing is to a conductor, not to an adjacent microvia. This is therefore covered by test pattern C. By design, microvias can be spaced further apart than mechanical vias because of small feature size and possibility to stagger.

b. The build-up of the test vehicle for CAF test shall meet the following conditions:

1. Representative of the PID for material and PCB technology;
2. ≥ 10 copper layers;
3. 1.6 mm ± 10 % thickness over connector metallisation;
4. 17 µm copper foil on inner and outer layers;
5. Single sequence for drilling and plating;
6. Sequential lamination.

NOTE 1 The stack-up is laminated once, after which it passes through the lamination process for a second time to simulate sequential construction.

NOTE 2 It is important to note in Table 9-2, Table 9-3 and Table 9-4 that hole diameters are specified as drill bit diameter, not finished hole diameter.

c. The manufacture of samples shall follow the process flow as specified in the PID.

d. Surface finish on connector shall not be SnPb

NOTE This is specified because SnPb can contaminate the connector pins on the test rack. Alternative finishes, such as galvanic Au and/or Ni or ENEPIG do not show this problem.

e. In total 10 samples shall be tested from at least two different panels.

f. Registration should be ≤ 80 µm.

g. The actual registration achieved on each coupon shall be included for the calculation of minimum insulation distances.

Table 9-2: CAF pattern dimensions – via-to-via straight

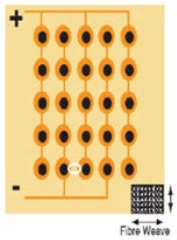
Description	Pattern	Drill diam. (µm)	Pad diam. (µm)	Via edge to via edge (µm)
x and y direction 1020 pitch 	IPC A1	750	860	270
	IPC A2	650	810	370
	IPC A3	500	750	520
	IPC A4	350	690	670
	ECSS A4	300	600	720

Table 9-3: CAF pattern dimensions – via-to-via staggered

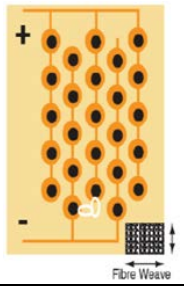
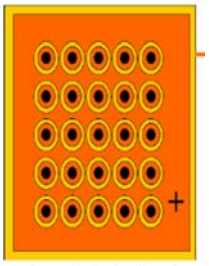
Description	Pattern	Drill diam. (µm)	Pad diam. (µm)	Via edge to via edge (µm)	Via edge to via edge Manhattan distance (µm)
1080 pitch 	IPC B1	800	940	280	396
	IPC B2	700	890	380	537
	IPC B3	550	840	530	750
	IPC B4	450	750	630	891
	ECSS B4	300	600	780	1103

Table 9-4: CAF pattern dimensions – via-to-plane

Description	Pattern	Drill diam. (µm)	Pad diam. (µm)	Clearance diam. (µm)	Via edge to plane (µm)
	IPC C1	350	none	640	145
	IPC C2	350	none	700	175
	IPC C3	350	none	850	250
	IPC C4	350	none	960	305

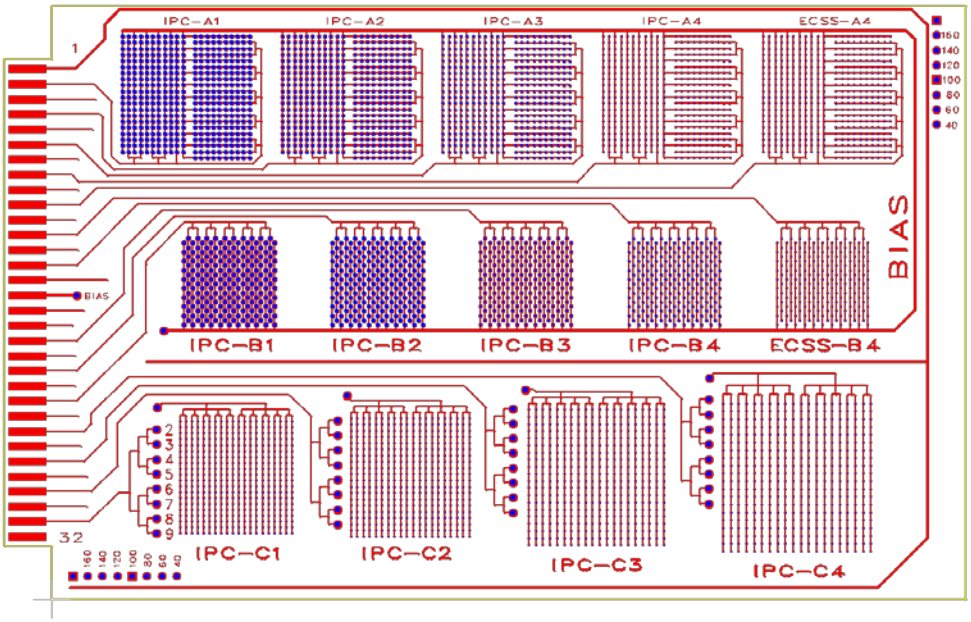


Figure 9-12: Lay-out of CAF pattern

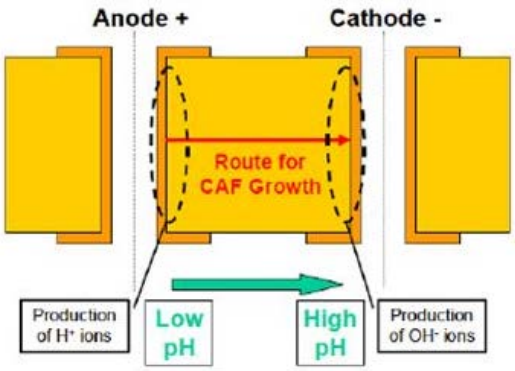


Figure 9-13: Schematic for CAF growth

9.7.3.3 Test method

a. The sample preparation method shall be as follows:

1. measurement of registration on electrical test coupons;
2. bake-out in conformance with clause 9.2.2;
3. six times reflow simulation in conformance with clause 9.8.3;
4. ultrasonic cleaning followed by bake-out in conformance with clause 9.2.2.

b. The CAF test method shall be as follows:

1. Ambient phase using the parameters: 24 h, 25°C, 50 % RH, 0 V;
2. Preconditioning phase using the parameters: 96 h, 85 °C, 75 % RH, 0 V;
3. CAF phase using the parameters: 500 h, 85 °C, 75 % RH, 50 V;
4. Ambient phase using the parameters: 24 h, 25°C, 50 % RH, 0 V.

NOTE CAF is relevant for HDI which can use voltages up to 30 V in conformance with ECSS-Q-ST-70-12. The guidelines in IPC-9691B recommend a margin of x2. For practical considerations of the test equipment this is limited to 50 V.

c. During the CAF test method insulation resistance of all patterns shall be measured periodically using an electrometer capable of measuring high resistances combined with a switchbox, while maintaining the bias voltage if applicable.

NOTE The AutoSIR equipment can perform this task.

d. Acquisition rate during the CAF phase shall be at least once in 10 minutes.

NOTE A faster acquisition rate is good practice to be able to detect transient changes.

e. During the ambient and preconditioning phases, only a few acquisitions of insulation resistance shall be done.

NOTE This is specified because bias voltage is applied during measurement, in phases that are specified to be without bias stress.

f. After the CAF test method, the location of breach of insulation should be determined on each pattern by electrical insulation of sections of the pattern.

NOTE Localisation in A and B pattern comprises of determining the x, y location, which can be achieved by insulation of sections of the surface pattern. Localisation in C pattern comprises of determining the layer, which can be achieved by insulation of the interconnections to the planes that are designed on the surface.

g. After localisation samples should be microsectioned to determine the cause of a breach of insulation resistance.

9.7.3.4 Reporting of results

a. A sudden drop in resistance by an order of magnitude shall be breach of insulation.

NOTE Breach of insulation can occur intermittent or continuous. Examples of stable insulation and breach of insulation are shown in Figure 9-10.

b. The results shall be evaluated by the qualification authority and by the procurement authority for the HDI technology under evaluation.

9.8 Group 6 – Assembly and life test - short

9.8.1 Overview

Group 6 includes a lower number of 200 thermal cycles with a higher temperature range of 200 °C. It does not include electrical testing and peel strength. This thermal cycling method is quicker to perform and has heritage from ECSS-Q-ST-70-10. The group 6 is performed for delta qualification or project qualification, in case it is not necessary to cover the general assembly verification.

The test levels for thermal cycling are not only driven by space environment. Thermal cycling to the levels specified in clauses 9.6.2 and 9.8.2 provide reference to the heritage test levels that assess robustness of the PCB construction.

See clause 9.6.1 for an overview of group 4.

9.8.2 Test flow for group 6

a. The test vehicle for group 6 shall include the PCB.

b. The test vehicle for group 6 may include additional coupons.

c. The following test steps shall be performed for group 6 in this order:

1. bake-out in conformance with clause 9.2.2;
2. reflow simulation in conformance with clause 9.8.3;
3. rework simulation on at least 4 PTH of the PCB in conformance with clause 9.5.4;
4. thermal cycling in conformance with clause 9.8.4;
5. microsectioning in conformance with clause 9.5.2;
6. evaluation of acceptance criteria in conformance with clause 10.2.

d. Microsectioning and evaluation in conformance with 9.8.2c.5 and 9.8.2c.6 shall be performed on the following:

1. At least 4 PTH of the PCB that have been subjected to rework simulation;
2. All technology features under qualification.

e. In case of project qualification, the reflow simulation and rework simulation may be tailored to be representative of the assembly processes.

f. In case of project qualification, the reflow simulation and rework simulation shall be representative of the worst-case assembly processes.

NOTE Assembly processes include initial assembly by hand and machine soldering, as well as rework and repair.

g. In case of project qualification with specific environmental requirements, the thermal cycling may be tailored.

NOTE 1 Specific environmental requirements can include operational temperature below -55 °C or above +85 °C, for instance for detector technology that is exposed to planetary environment.

NOTE 2 It is not good practice to reduce the temperature range or number of cycles because thermal cycling is not only a simulation of space environment. It also simulates equipment on/off cycles and it is considered a general assessment of PCB robustness.

9.8.3 Reflow simulation

a. Reflow simulation shall be performed using a vapour phase equipment and process that are representative of assembly, except for the case in requirement 9.8.3b.

b. In case reflow simulation is used for a specific project qualification that uses another assembly method than vapour phase, the test method may be tailored to be representative.

c. The test board shall be lowered into the vapour phase at a temperature of minimum 215 °C.

NOTE Specific vapour phase chemistry are commonly used with a temperature of up to 230 °C.

d. The duration at the maximum temperature of the profile shall be between 5 s and 10 s.

e. The sample shall be cooled at ambient temperature for at least 10 minutes.

f. After cool down, the sample shall be exposed to a second reflow by repeating the steps from requirements 9.8.3c, 9.8.3d and 9.8.3e.

9.8.4 Thermal cycling

a. Thermal cycling shall be performed in a one chamber system with ambient pressure.

b. A temperature sensor shall be in contact with the test vehicle to monitor its temperature continuously.

c. The rate of temperature change shall not exceed 10 °C/minute.

d. The dwell time at minimum and maximum temperature shall be at least 15 minutes.

e. The cycling programme shall start with the hot cycle first.

f. The temperature should be minimum -60 °C and maximum +140 °C.

g. The minimum temperature shall be between -55 °C and -70 °C.

NOTE This covers the assembly verification in conformance with requirement 13.3.d of ECSS-Q-ST-70-08 and 14.6 of ECSS-Q-ST-70-38.

h. The maximum temperature shall be between +130 °C and +145 °C.

NOTE The Tg of laminates is typically higher than this temperature.

i. The temperature range shall be at least 200 °C.

j. The number of cycles shall be 200.

10
Acceptance criteria

10.1 Overview

The tables in this clause specify the technological features under evaluation. They include an identification by a reference letter, as specified in clause 4.4. The tables specify acceptance criteria for the technological features, as well as the inspection sample and the inspection method. The inspection sample includes a description of the condition, such as AR, RW, SB. In case this condition is placed in brackets, it indicates that vias with the condition in brackets are present on the coupon and are available for inspection for the technological feature, but the condition in brackets holds no relevance for the evaluation of the technological feature. This is the case for defects associated with PCB manufacture and present in AR condition when these defects are evaluated on a coupon after thermal stress that does not cause alteration of the defect.

Illustrations of measurements methods and acceptance criteria are given in photographs and drawings in the notes of the tables from clauses 10.2 to 10.4.

10.2 Inspection by microsectioning for dimensional verification

a. For the technological feature internal annular ring, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-1.

b. For the technological feature external annular ring, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-2.

c. For the technological feature copper foil thickness, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-3.

d. For the technological feature copper plating thickness, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-4.

For the technological features etchback and glass fibre protrusion, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with

e. Table 10-5.

f. For the technological feature wicking, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-6.

g. For the technological feature wrap copper, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-7.

h. For the technological feature dielectric thickness for standard technology. The acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-8.

i. For the technological feature dielectric thickness for microvia layers, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-9.

j. For the technological features microvia dimensions and aspect, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-10.

k. For the technological feature microvia plating voids, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-11.

l. For the technological features tin-led thickness and composition, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-12.

m. For the technological features electrolytic nickel and gold dimensions, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-13.

n. For the technological feature undercut, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-14.

o. For the technological feature overhang, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-15.

p. For the technological feature dimensional verification of the rigid-flex interface the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-16.

Table 10-1: Annular ring internal

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Inner layer	≥ 50 µm	Location: coupon A/B + A/Bi Condition: set 1 AR(+RW) + set 2 Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Lighting: bright field Measure as shown in Figure 10-1. Measure at the foot of the pad. Measure innerlayer pad from the hole wall. Measure excluding plated copper.
b.	Inner layer at end of blind via	≥ 50 µm		
c.	Inner layer at end of buried via	≥ 50 µm		
d.	Micro via capture pad	≥ 10 µm		
e.	Inner layer in conformance with 10.6.1d	≥ 25 µm	Location: electrical registration in 4 corners Frequency: per panel	

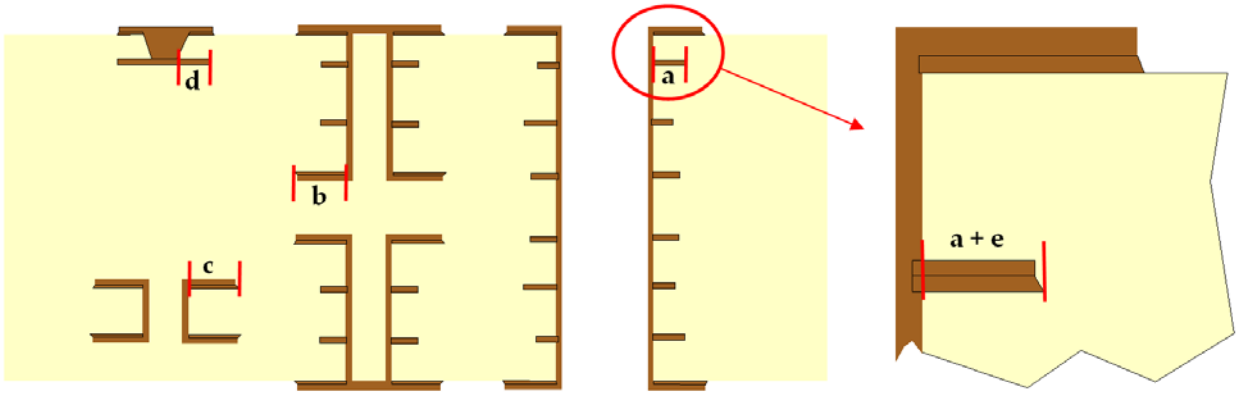


Figure 10-1:Annular ring internal

Table 10-2: Annular ring external

Ref..	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Outer layer	≥ 100 µm	Location: coupon A/B + A/Bi Condition: set 1 AR(+RW) + set 2 Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Lighting: bright field Measure as shown in Figure 10-2. Measure at the foot of the pad. Measure excluding plated copper for ref f. For all other references, measure including plated copper.
b.	Outer layer PTH solder side	≥ 200 µm		
c.	Outer layer PTH solder side only for rigid polyimide	≥ 130 µm		
d.	Outer layer PTH only for flex termination	≥ 250 µm on component hole ≥ 100 µm on non-soldering hole		
e.	Outer layer blind via	≥ 100 µm		
f.	Micro via outer layer	≥ 10 µm		
g.	Non-plated hole outer layer	≥ 250 µm		

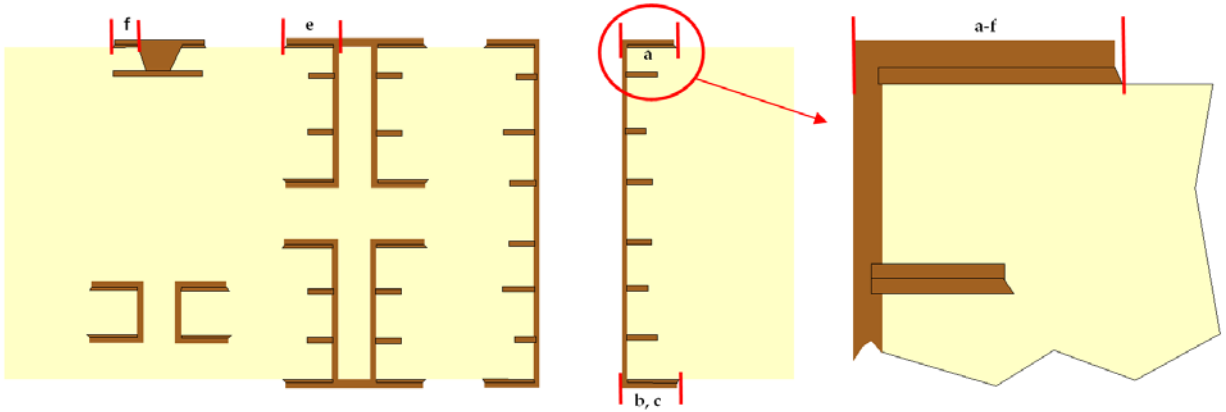
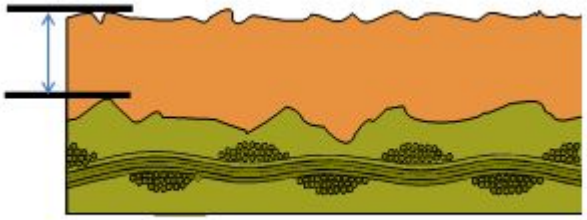


Figure 10-2 Annular ring external

Note: Annular ring on outer layer as specified in ref a from Table 10-2, includes vias and PTH on component side for rigid, rigid/flex and flex technology.

Table 10-3: Copper foil thickness

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
	Nominal copper foil thickness	**Minimum measured copper foil thickness after processing**	Location: coupon A/B Condition: set 1 AR(+RW) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x for a, b ≥ 400x for c, d, e Illumination: bright field Measure as shown in Figure 10-3.
a.	70 µm	≥ 56 µm		
b.	35 µm	≥ 25 µm		
c.	17 µm	≥ 11 µm		
d.	12 µm for HDI	≥ 9 µm		
e.	9 µm for HDI	≥ 6 µm		



The microetching and passivation on the top surface is not subtracted from the thickness measurement.
The treatment on the bottom surface to the laminate is subtracted from the thickness measurement.

Figure 10-3: Copper foil thickness

Note 1: The equivalent IPC test method is described in IPC-A-600 test method 3.2.4 and IPC-6012D chapter 3.6.2.15

Note 2: This is also specified in Table 7-1 of ECSS-Q-ST-70-12C.

Table 10-4: Copper plating thickness

Ref.	technological feature		Acceptance criteria	Inspection sample	Method
a.	Electroplated copper in PTH and through going vias	Rigid	≥ 25 µm average on resin ≥ 20 µm on any local thin area on resin or glass	Location: coupon A/B + A/Bi Condition: set 1 AR(+RW) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field Measurement "average on resin" is performed on 3 locations in the hole in accordance with Figure 10-4 and in accordance with zone A of Figure 10-5. Measurement "on any local thin area on resin or glass" is performed in accordance with zone B of Figure 10-5.
b.		Flexible	≥ 25 µm average on resin ≥ 20 µm on any local thin area on resin or glass		
c.		Rigid-flex	≥ 30 µm average on resin ≥ 25 µm on any local thin area on resin or glass		
d.	Electroplated copper in blind and buried via		≥ 25 µm average on resin ≥ 20 µm on any local thin area on resin or glass		
e.	Electroplated copper over base copper		≥ 25 µm		

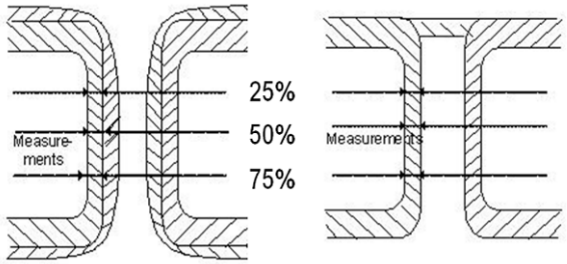


Figure 10-4: Three measurements of copper plating thickness at locations that are at 25 %, 50 % and 7 % of the height of the hole

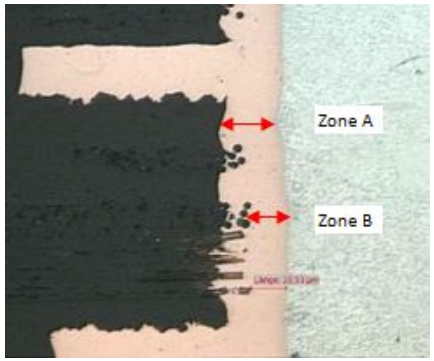


Figure 10-5: Measurement "average on resin" is performed on zone A. Measurement "on any local thin areas on resin or glass" is performed on Zone B

Note 1: There is no additional requirement for total copper thickness on surface. Min copper foil after processing is 11 µm, plus 25 µm plated copper, results in 36 µm total copper thickness for standard technology.

Note 2: Coupon A/B includes the minimum via diameter in conformance with requirement 15.2.d.6 from ECSS-Q-ST-70-12 which is verified for copper plating thickness as the inspection from this table.

Table 10-5: Etchback and glass fibre protrusion

Ref.	technological feature	Acceptance criteria	Inspection sample	Method
a.	Etchback	Between negative -13 µm and positive +20 µm	Location: coupon A/B + A/Bi Condition: set 1 AR(+RW) set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: x200 min illumination: bright field
b.	Glass fibre protrusion, in case of negative etchback	Glass fibres should protrude into hole wall relative to the resin		
c.	Glass fibre protrusion, in case of positive etchback	Glass fibres should protrude into hole wall relative to the inner layer		
d.	Glass fibre protrusion	Glass fibre protrusion should be limited such that the requirement for minimum Cu plating thickness is achieved.		

Ref.	technological feature	Acceptance criteria	Inspection sample	Method

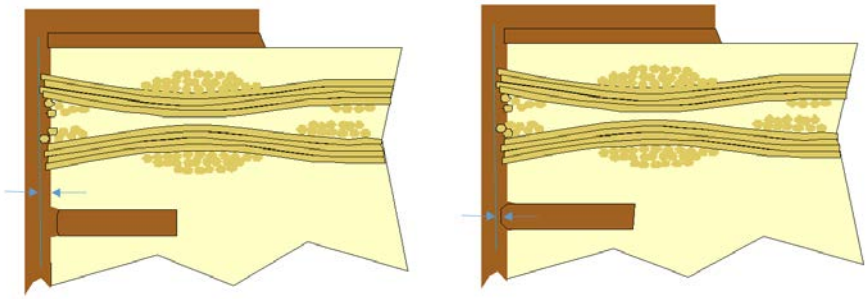


Figure 10-6: Glass fibre protrusion in case of negative etchback (left) and positive etchback (right)

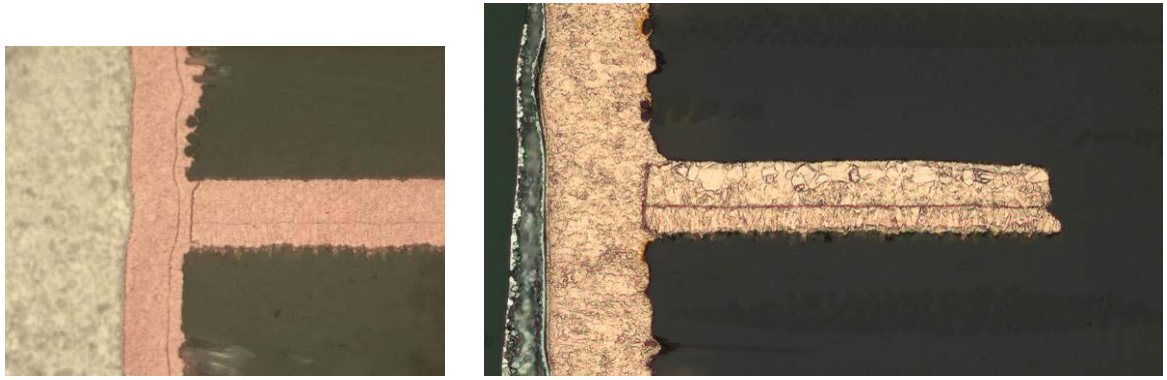


Figure 10-7: Example of negative etchback (left) and approximately neutral etchback (right)

Note 1: Glass fibre protrusion is a qualitative assessment of the general aspect of the hole. A single occurrence outside requirement is not a nonconformance if the general aspect meets the requirement.

Note 2: Etchback is the distance from resin of hole wall to innerlayer foil. It can be both positive or negative depending on the processes used.

Table 10-6: Wicking

Ref.	Technological feature	Acceptance criteria	Sample	Method
a.	Wicking on standard technology	≤ 50 µm	Location: coupon A/B + A/Bi Condition: All coupon sets Frequency: per panel	Microsection and Microscope: Magnification: x200 min Lighting: bright field Wicking is measured from the resin of the hole wall.
b.	Wicking on reduced annular ring of ≥ 25 µm	≤ Min annular ring		

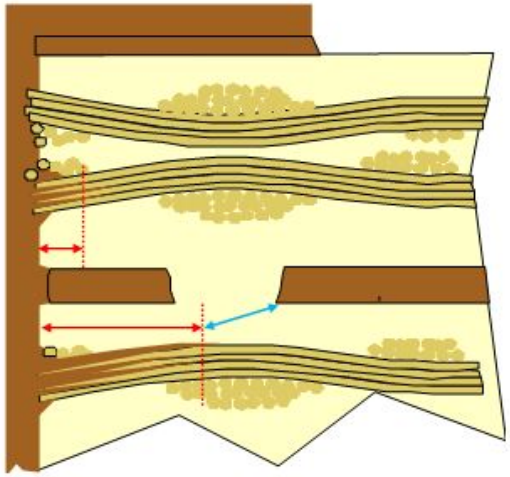


Figure 10-8: Wicking is measured from resin of hole wall (red arrows). In case it exceeds the annular ring, the insulation distance to adjacent circuitry (blue arrow) can be reduced.

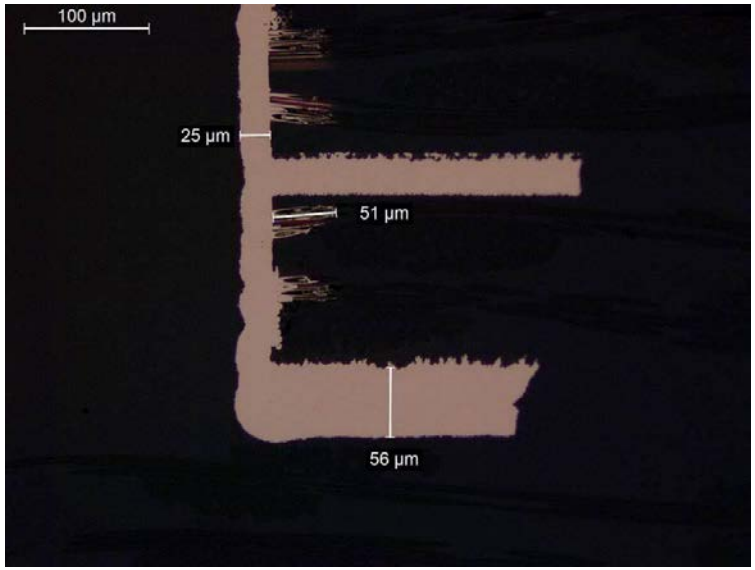


Figure 10-9: Example of wicking

Table 10-7: Wrap copper

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Copper wrap thickness	≥ 5µm wrap thickness	Location: coupon A/Bi Condition: set 1 AR (+RW), set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field Wrap thickness as per red arrows Wrap length as per blue arrow
b.	Copper wrap length	≥ 25µm wrap length		

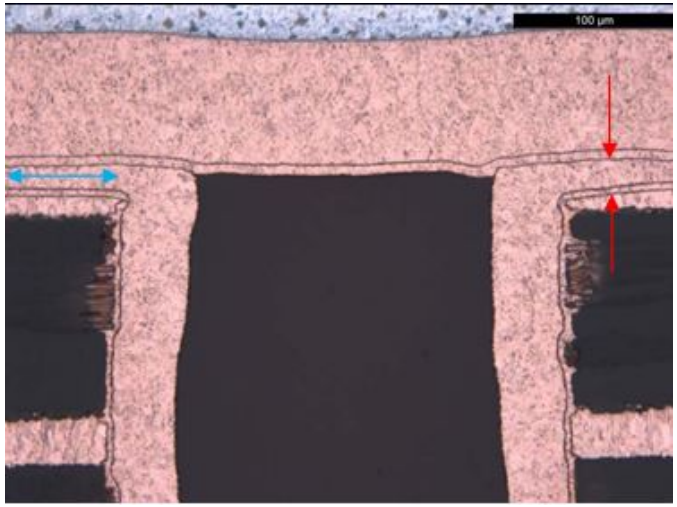


Figure 10-10: wrap target condition

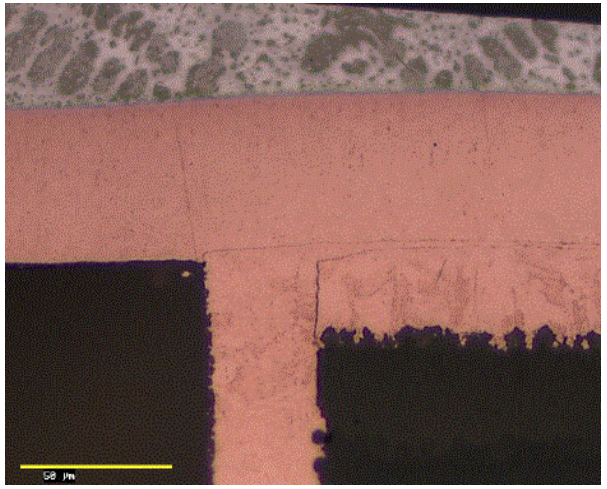


Figure 10-11: Wrap thickness below requirement, not acceptable

Note: Planarization or selective plating can be in the PCB manufacturer's PID, if the copper wrap criteria from this table are met. Insufficient wrap copper indicates too much planarization. This can cause separation in plating layers due to lack of mechanical strength.

Table 10-8: Dielectric thickness – standard technology

Ref.	technological feature	Acceptance criteria	Inspection sample	Method
a.	Insulation between layers	≥ 70 µm for rigid ≥ 22,5 µm for flex	Location: coupon A/Bi Condition: set 1 AR + set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field
b.	Number of prepreg	min 2		
c.	Number of glass layers in laminate	recommended ≥ 2, i.a.w. ECSS-Q-ST-70-12 clause 7.1.3.b.		
d.	Glass fibre compression	not acceptable in case track is compressed into glass bundle and resin starvation occurs		

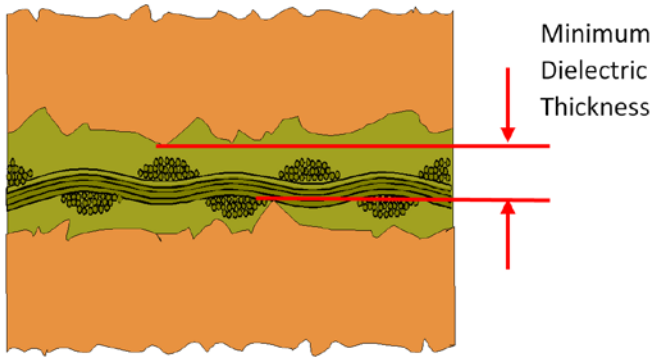


Figure 10-12:Projected-peak-to-peak insulation

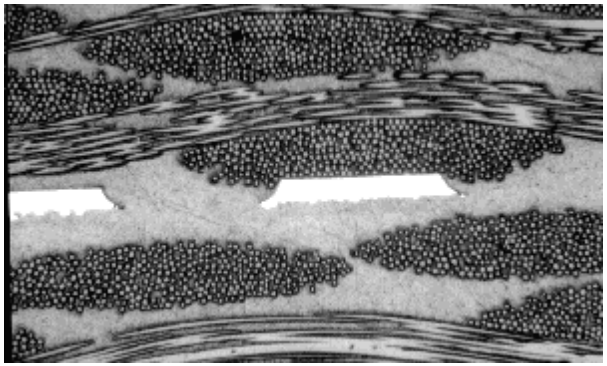


Figure 10-13: Example of glass compression

Table 10-9: Dielectric thickness – microvia layers

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Insulation between layers	≥ 60 µm and ≤ 120 µm	Location: coupon A/Bi Condition: set 1 AR (+RW), set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field
b.	Number of prepreg	2		
c.	Penetration of capture pad	Complete penetration through pad not acceptable		

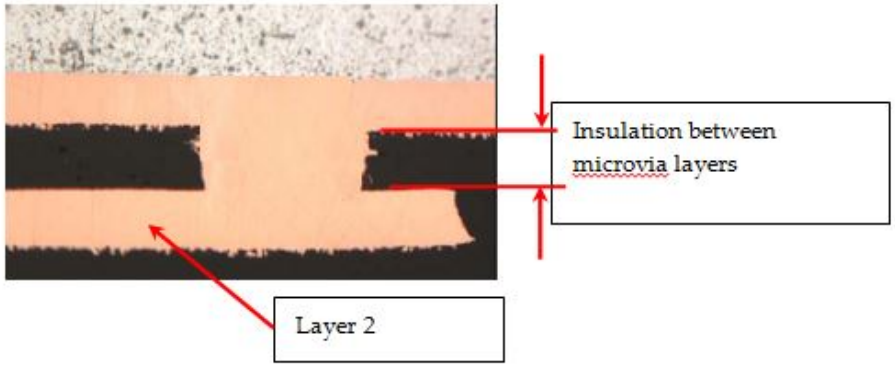


Figure 10-14 Microvia insulation

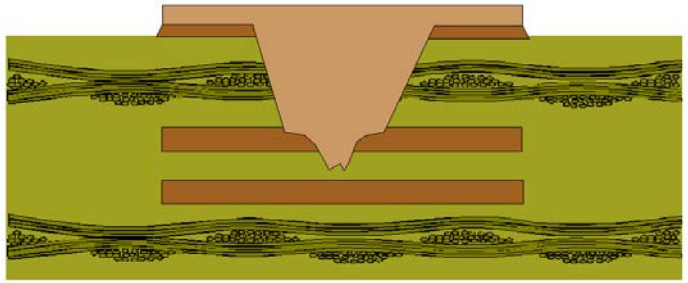


Figure 10-15 Penetration of capture pad for µvia, not acceptable

Note: Dielectric thickness of approximately 60 µm can create a risk for glass compression. The maximum of 120 µm is caused by 20 % tolerance on as-designed thickness of 100 µm, in conformance with req 11.4.i from ECSS-Q-ST-70-12. The maximum thickness is in addition limited by the requirement for aspect ratio ≤ 1 of microvias, in conformance with ref c from Table 10-10. In case of high dielectric thickness there can be a risk not to meet the contact diameter of 100 µm in conformance with ref d from Table 10-10.

Table 10-10: Dimension and aspect of microvias

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Dimple	≤ 50 µm	Location: coupon A/Bi Condition: set 1 AR (+RW) set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field Planarity is measured at the top of the copper surface
b.	Bump	≤ 15 µm		
c.	Aspect ratio	≤1 ECSS-Q-ST-70-12 11.4.2.a.		
d.	Contact diameter to capture pad	≥100 µm continuous contact ECSS-Q-ST-70-12 11.4.2.g		
e.	Interconnect defect from microvia to capture pad	not acceptable		

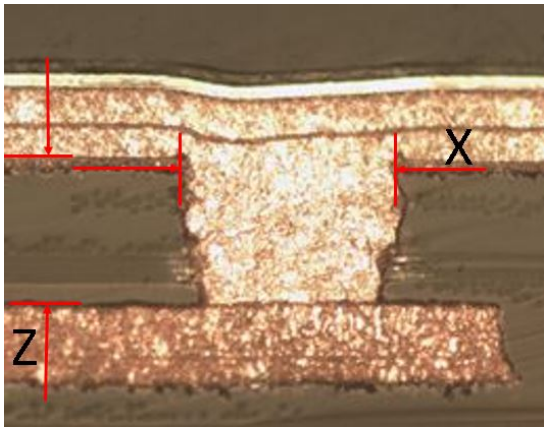


Figure 10-16 Microvia aspect ratio, X ≥ Z

(X=laser drilled diameter in layer 1 base copper, Z=distance from top of layer 1 base copper to top of capture pad copper)

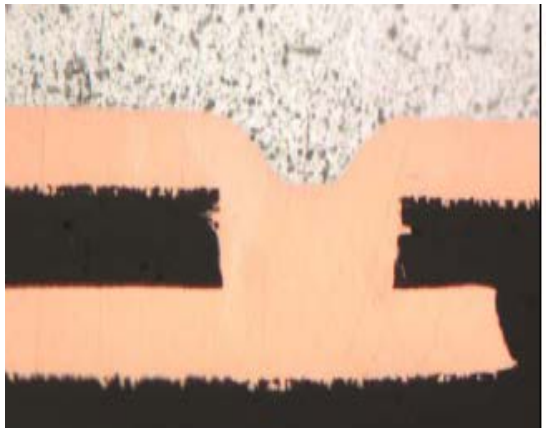


Figure 10-17 Dimple in microvia

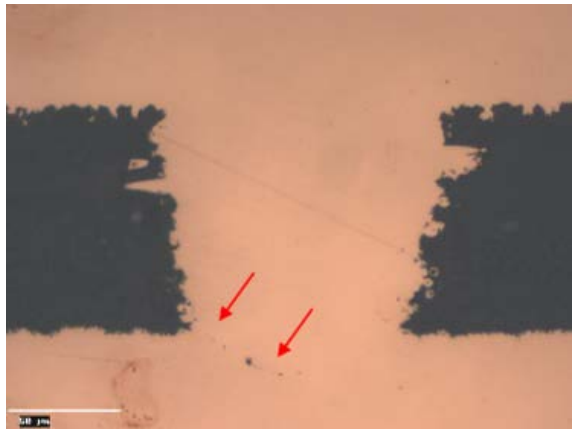


Figure 10-18 ICD on capture pad

Note: Microvias can show resin or glass at the bottom edge. This is not considered a defect in case 100 µm continuous contact is achieved. Presence of dielectric material is not considered ICD.

Table 10-11: Microvia plating voids

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Void inside copper filled microvia	Target condition: no voids, Voids acceptable if: - Less than 25% of the copper filling area in the cross section AND - Minimum copper fill thickness is 18µm on hole wall, on top of capture pad and to top surface of the copper fill.	Location: coupon A/Bi Condition: set 1 AR+(RW), set 2 (SB), IST coupon (after test) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field

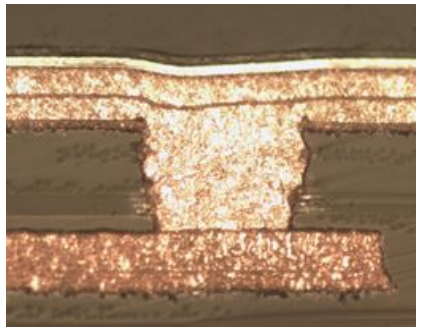


Figure 10-19 Microvia plating, target condition

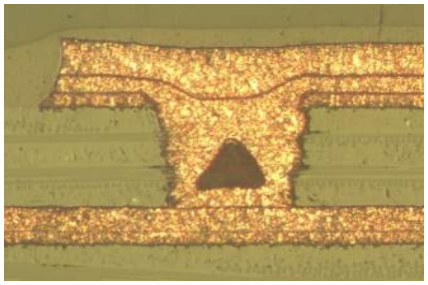


Figure 10-20 Example of void in microvia plating

Note1: See requirement 10.6.3a

Note 2: Allowance for voiding is specified in this table for a relatively low sample size as done for procurement. In qualification a larger sample size can be taken to verify that the target condition is achieved.

Note 3 Voids in copper filling are typically of spherical or triangular shape.

Table 10-12: Tin-lead thickness and composition

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	SnPb composition	Tin content 63±8 wt%	Location: coupon A/B Condition: set 1 AR Frequency: per panel	Ref a: XRF, SEM-EDX, atomic absorption spectrometry on bare PCB Ref b, c, d, e: Microsection and Microscope: Magnification: ≥ 200x for b, c, e ≥ 500x for d Illumination: bright field
b.	SnPb thickness on SMT pads	≥ 5 µm on thickest area		
c.	SnPb thickness on PTH hole wall	≥ 8 µm on thickest area		
d.	SnPb thickness on PTH corners	≥ 1 µm excluding the IMC OR < 1 µm acceptable in case: - SnPb present on top of IMC AND - acceptable solderability i.a.w. 9.4.11		
e.	SnPb thickness on PTH pads	≥ 5 µm OR < 5 µm acceptable in case: - SnPb present on top of IMC AND - acceptable solderability i.a.w. 9.4.11		

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method

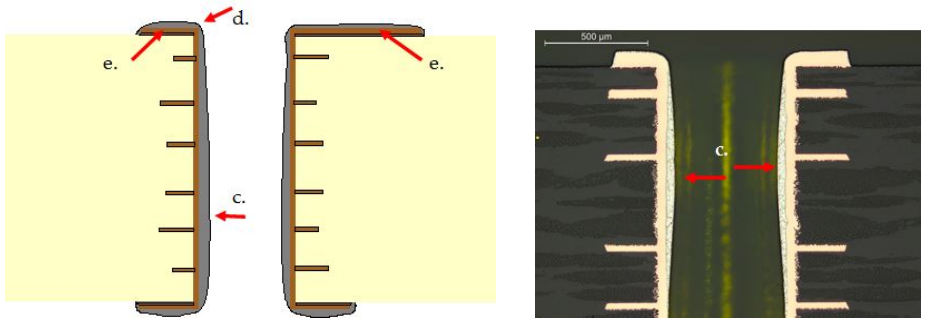


Figure 10-21: Tin-lead thickness in PTH schematic (left) and a typical microsection (right)

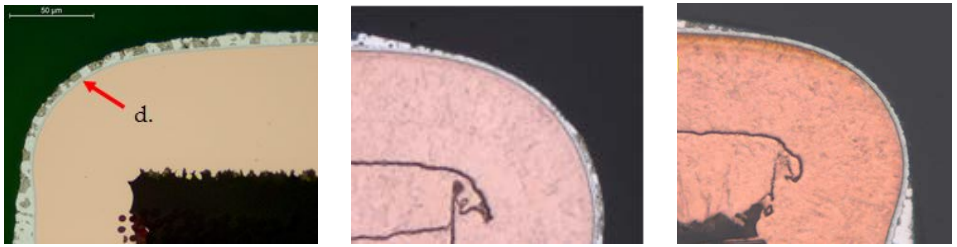


Figure 10-22: Tin-lead thickness on PTH corner – target thickness (left), coverage of less than 1 µm (middle), absence of SnPb on IMC (right)

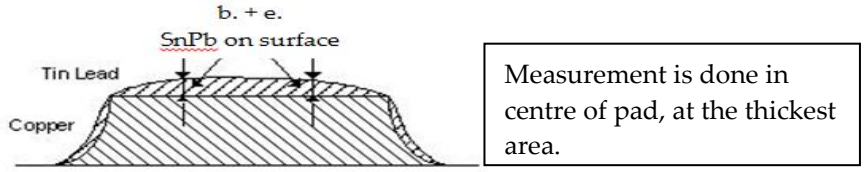


Figure 10-23: Tin-lead thickness on pad

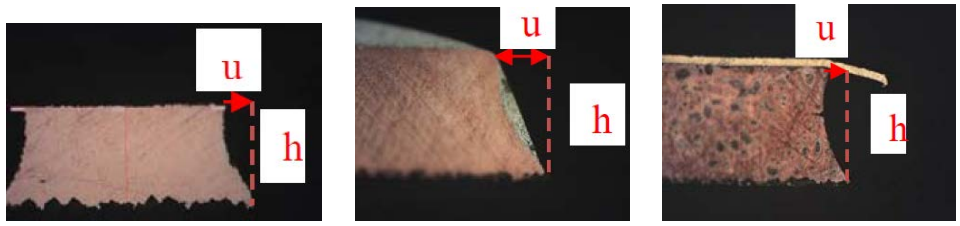
Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
Note 1:	Ref d allows for less than 1 µm SnPb thickness as long as the IMC is covered by SnPb and acceptable solderability test is obtained.			
Note 2:	For SMT assembly it can be important to have a SnPb thickness variation of less than 25 µm to ensure planarity. This can be important within the same SMT footprint for dedicated devices, but it is considered less important among different footprints of the PCB. This aspect depends on the design of the footprint that can have SMT pads with or without through-going vias adjacent to it. In case the customer needs to specify planarity of SnPb finish on SMT footprints, it is good practice to include this in the PCB definition dossier.			

Table 10-13: Electrolytic nickel and gold dimensions

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Electrolytic nickel	≥ 2 µm on all locations, and ≤ 10 µm on hole wall	Location: PCB or coupon A/B Condition: AR Frequency: per panel	XRF on PCB, or Microsection and Microscope: Magnification: ≥ 200x illumination: bright field
b.	Electrolytic gold on nickel	≥ 1 µm		
c.	Electrolytic gold on copper	≥ 3 µm		
d.	Length of tin-lead overlap on Au	≥ 150 µm		
Note 1: Gold is not a recommended finish for soldering as per ECSS-Q-ST-70-08 clause 6.6.2a and 6.8.2a. Note 2: Tin-lead overlap as –designed is 200 µm as per see 7.8.1.d.1 of ECSS-Q-ST-70-12 Note 3: For Ref. a, no max on surface is specified Note 4: For Ref. d and c no max is specified				

Table 10-14: Undercut

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Undercut on internal layers	u ≤ h	Location: coupon A/B Condition: set 1 AR Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field
b.	Undercut on external layers reflowed Sn/Pb finish	u ≤ h		
c.	Undercut on external layers Electrolytic Ni/Au or Au finish	u ≤ h		



Ref A Ref B Ref C

Figure 10-24: Undercut

Note

Table 10-15: Overhang

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Overhang on reflowed Sn/Pb finish	No overhang	Location: coupon A/B Condition: set 1 AR Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field
b.	Overhang on electrolytic Ni/Au or Au finish	D ≤ 2x total thickness of copper (h) in case of conformal coating as per 10.6.3i		

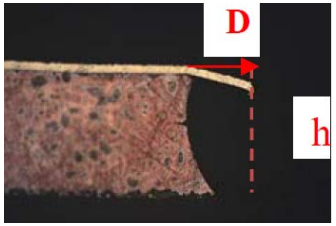


Figure 10-25:Overhang of electrolytic Au

Note: For Tin-lead finish during the reflow operation the overhang of Tin-lead is flowing on the side of the tracks or pads: if the reflow operation has been well conducted there is no overhang left.

Table 10-16: Rigid-flex interface -dimensional verification

Ref.	Technological feature	Acceptance criteria	Sample	Method
a.	Coverlay and bond-ply insertion into rigid section i.a.w. ECSS-Q-ST-70-12 clause 9.4.c	≥ 1 mm	Location: rigid-flex coupon Condition: SB Frequency: per panel	Microsection and Microscope Magnification: 50-200x illumination: bright and dark field
b.	Distance between hole wall and rigid edge of interface, i.a.w. ECSS-Q-ST-70-12 clause 9.5.a.	≥ 2mm		
c.	Overlap between coverlay and pad, i.a.w. ECSS-Q-ST-70-12 clause 9.4.e.	Not acceptable		

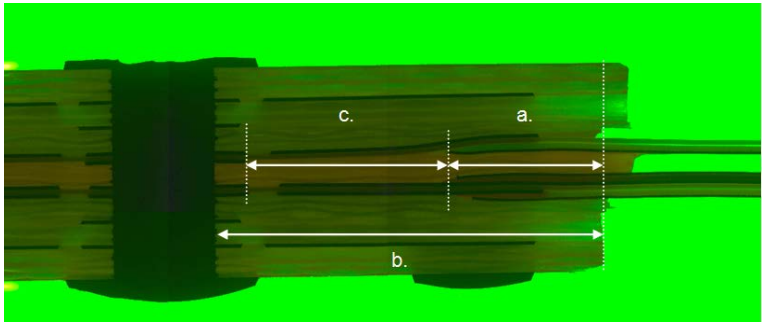


Figure 10-26: Example of dimensional verification of rigid-flex interface

Note 1: In case coverlay insertion into rigid section is 2 mm and distance between hole wall and rigid edge is 2mm then the coverlay overlaps the pad and requirement is not achieved. Requirement 9.4d from ECSS-Q-ST-70-12 specifies that in a multilayer rigid-flex PCB where flex laminates are bonded together with bondply, the ends of the coverlay and bondply are off- set in the rigid section by 1 mm to prevent a line of weakness.

Note 2: Requirements a and b are as-manufactured. Requirement a is derived from 1,5 mm (from ECSS-Q-ST-70-12) as-designed and allowing for 0,5 mm manufacturing tolerance.

Note 3: To achieve ≥ 2 mm distance in requirement b, it can be necessary to design a larger distance to allow for manufacturing tolerances. Moreover, for complex build-ups a further increase of this distance by design is good practice because tolerances are larger.

10.3 Inspection by microsectioning for qualitative aspects

a. For the technological feature via filling the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-17.

b. For the technological feature cap lift, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-18.

c. For the technological feature blind via planarity, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-19.

d. For the technological features burrs and nodules, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-20.

e. For the technological features voids and inclusions in copper plating the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-21.

f. For the technological features wedge voids the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-22.

g. For the technological feature resin voids, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-23.

h. For the technological features delamination, blistering, crazing and measling, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-24.

i. For the technological feature pad lift, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-25.

j. For the technological feature dielectric cracks, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-26.

k. For the technological features cracks and separation in copper, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-27.

l. For the technological feature ICD, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-28.

m. For the technological feature smear, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-29.

n. For the technological features hole wall pull away and resin recession, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-30.

o. For the technological feature nail heading, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-31.

p. For the technological feature copper-invar-copper, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-32.

q. For the technological feature inhomogeneity in dielectric, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-33.

r. For the technological features contamination and foreign inclusions, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-34.

s. For the technological feature rigid-flex interface delamination between coverlay and prepreg, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-35.

t. For the technological feature rigid-flex interface adhesive voids in coverlay and bond-ply, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-36.

u. For the technological feature rigid-flex interface misalignment of prepreg, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-37.

Table 10-17: Blind and buried via filling

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Voids or cracks in the resin of blind and buried vias inside zone A	Target condition: no voids, no cracks Incidental voids or cracks are acceptable in case the plane of the microsection is filled as follows: - for buried via ≥ 85%, - for blind via ≥ 75%.	Location: coupon A/Bi Condition: set 1 AR + set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field
b.	Voids or cracks in the resin of blind and buried vias outside zone A	Voids at open ends, as shown in Figure 10-28, are not acceptable		
		Voids in contact with cap plating, as shown in Figure 10-28, are not acceptable		

Figure 10-27: examples of acceptable voids

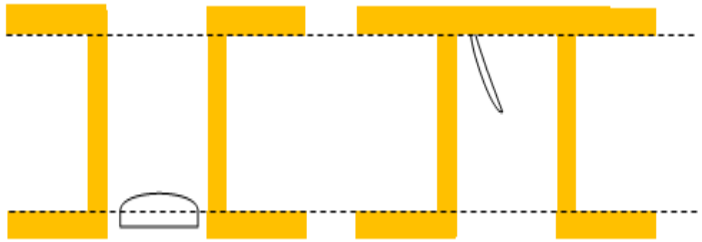


Figure 10-28: examples of unacceptable voids

Note 1: The via filling can be performed by resin flowing from the prepreg or by pre-filling using ink or plugging paste.

Note 2: This figures in this table also apply to cracks.

Note 3: Cracks protruding out of the via are evaluated in conformance with Table 10-26.

Table 10-18: Blind via cap lift

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Cap lift (bulging)	Not acceptable in case via-in-pad are used for soldering as per 6.2.3e.	Location: coupon A/Bi Condition: set 1 AR + set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field
b.	Thin line separation	Acceptable as received and after solder bath float up to 3 µm separation.		
c.	Copper surface plating thickness on resin	≥ 25 µm in conformance with Ref e from Table 10-4		

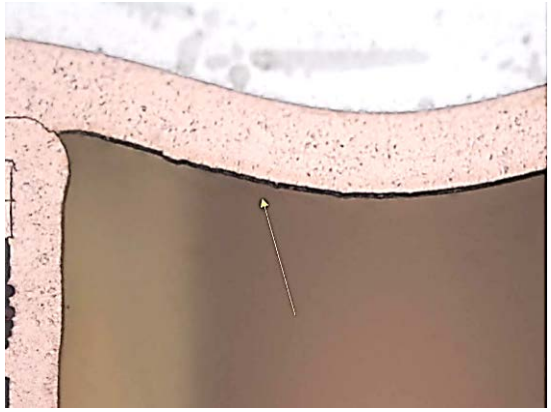


Figure 10-29: example of acceptable thin line separation

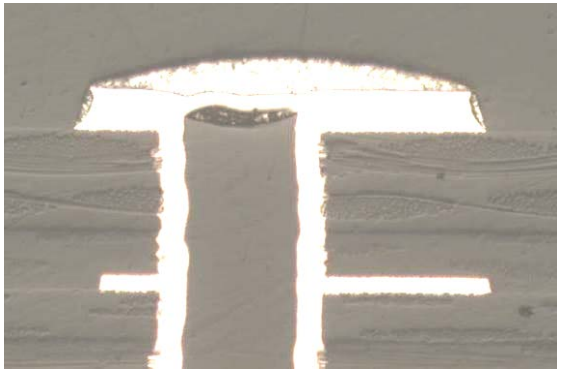


Figure 10-30: example of non-acceptable bulging

Table 10-19: Blind via planarity

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Dimple of blind via	≤ 50 µm ≤ 76 µm in case no AAD footprint on PCB	Location: coupon A/Bi Condition: set 1 AR + set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field Planarity is measured at the top of the copper surface
b.	Bumb on blind via	≤ 15 µm		

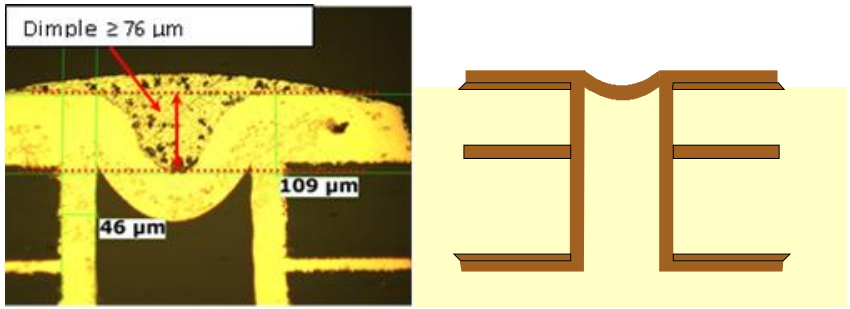


Figure 10-31: Example of dimple on blind via

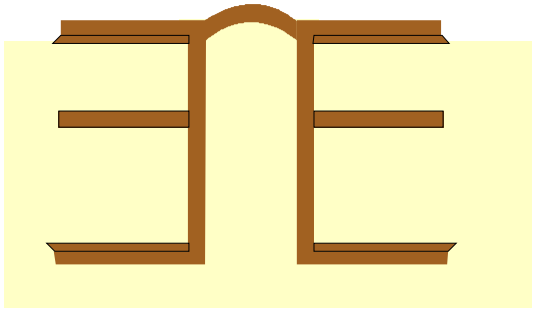


Figure 10-32: Example of bumb on blind via

Table 10-20: Burrs and nodules

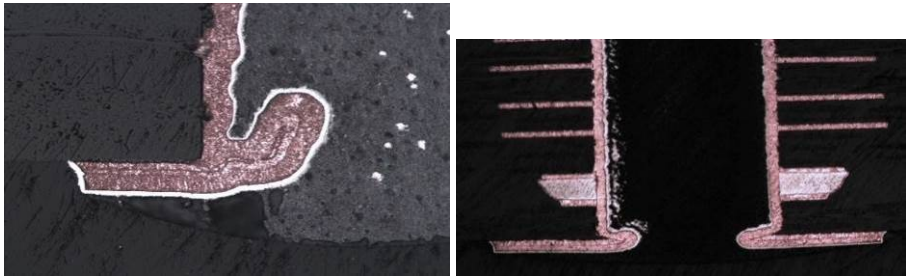
<table>
<tr><th>Ref.</th><th>Technological feature</th><th>Acceptance criteria</th><th>Inspection sample</th><th>Method</th></tr>
<tr><td rowspan="2">a.</td><td rowspan="2">Burrs and nodules</td><td>Not acceptable if diameter of plated hole is reduced to below the requirement</td><td rowspan="2">Location: coupon A/B
Condition: set 1 AR (+RW), set 2 (SB)
Frequency: per panel</td><td rowspan="2">Microsection and Microscope:
Magnification: ≥ 200x
illumination: bright field</td></tr>
<tr><td>Not acceptable if detached by probing with a gauge</td></tr>
<tr><td colspan="2"> 
Figure 10-13: Example of plating nodule</td><td colspan="3"> 
Figure 10-13: Example of burrs reducing hole diameter</td></tr>
<tr><td colspan="5">Note 1: It is good practice to avoid the presence of burrs and nodules because they can have a negative impact on reliability of the PTH as evaluated in IST.
Note 2: In case the PCB definition dossier does not specify a tolerance of vias, the tolerance of 0,1mm from requirement 6.2.3f.3 is used.</td></tr>
</table>

Table 10-21: Voids and inclusions in copper plating

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Voids and inclusions in copper plating	Target condition: no voids, no inclusions Incidental voids and inclusions are acceptable in case: - size ≤ 5 µm - Not reducing Cu plating thickness below the requirement of Table 10-4 - embedded within Cu plating layer - not in contact with SnPb	Location: coupon A/B + A/Bi Condition: set 1 AR(+RW) set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field
b.	Skip plating	Target condition: no skip plating Incidental skip plating on glass fibres is acceptable. Not acceptable on flex laminate		

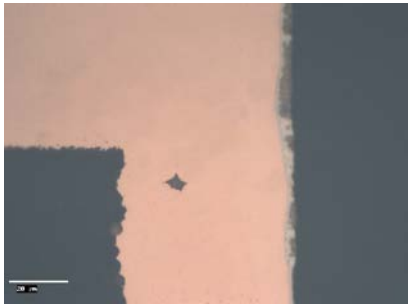


Figure 10-33: Example of voids – top image shows etch-out and bottom image shows an encapsulated void or inclusion

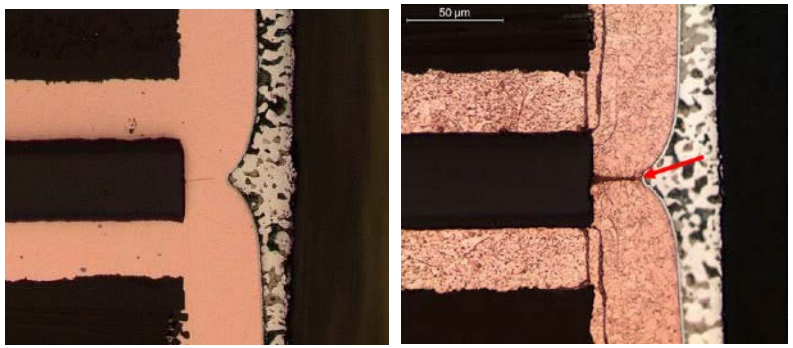


Figure 10-34: Skip plating on flex laminate as-polished (top) and after micro-etch (bottom)

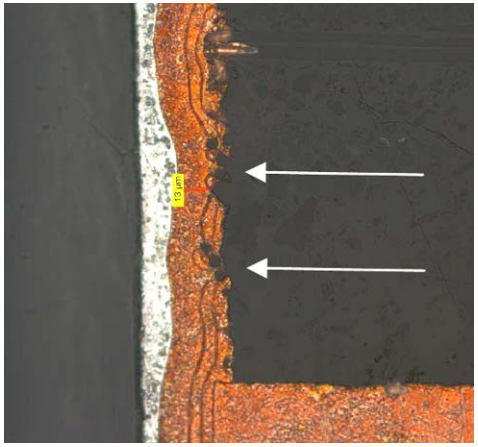


Figure 10-35: Skip plating on glass fibres

Note: Skip plating can be caused by electroless copper that does not cover local areas of the hole wall, such as glass fibres or flex laminate. Subsequent galvanic copper layers can cover up the skip plating, in which case the requirement for minimum copper thickness on local thin areas can be achieved. This can be observed as a plating fold in an etched microsection. On an unetched microsection the copper can seem continuous.

Table 10-22: Wedge voids

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Open wedge void	Not acceptable	Location: coupon A/B + A/Bi Condition: set 1 AR (+RW) set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field
b.	Copper filled wedge void	≤ 13 µm in depth (x direction) ≤ 10 µm in height (z direction)		
c.	Enclosed wedge void	≤ 13 µm in depth (x direction) ≤ 10 µm in height (z direction) Opening in wedge void ≤ 5 µm as per ref a of Table 10-22		

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method

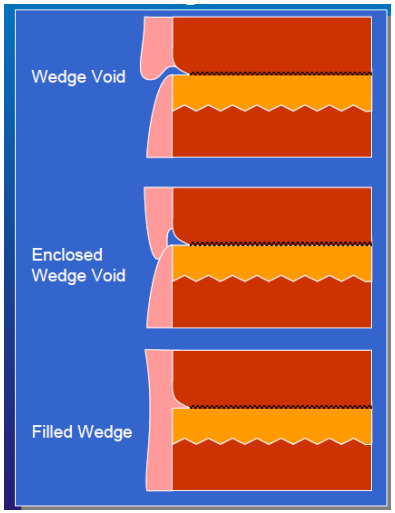


Figure 10-36 Schematic of wedge voids

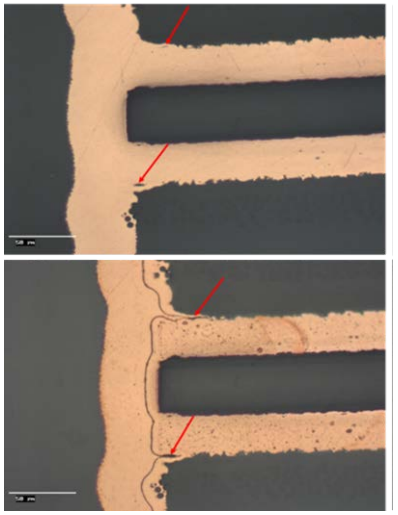


Figure 10-37 Example of wedge voids

Table 10-23: Resin void

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Resin voids	Target condition: no voids Incidental voids are acceptable if ≤ 80 µm and remaining insulation is in conformance with the PCB definition dossier	Location: coupon A/B + A/Bi Condition: set 1 AR (+RW), set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field
				

Figure 10-38: Example of resin void

Note: Resin voids can occur in prepreg as well as laminate

Table 10-24: Delamination, blistering, crazing, measling

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Delamination, blistering, crazing, measling	Not acceptable	Location: coupon A/B + A/Bi Condition: set 1 AR (+RW), set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field

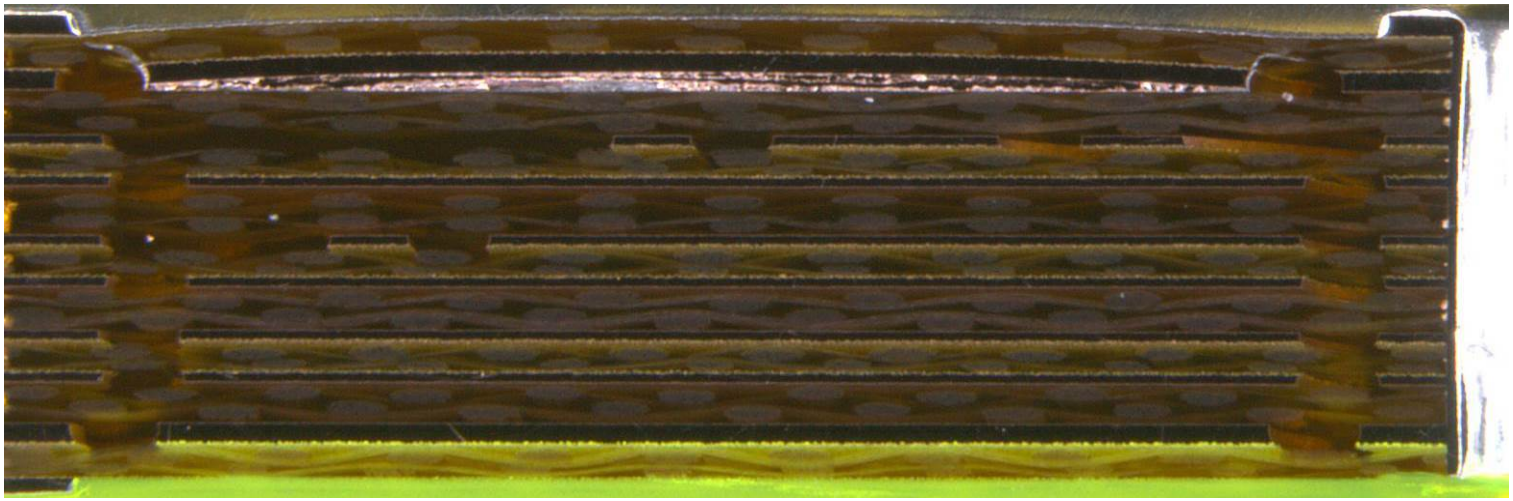


Figure 10-39: Example of delamination

Note : These defects are also evaluated during visual inspection as per Table 10-41.

Table 10-25: Pad Lift

Ref.	technological feature	Acceptance criteria	Inspection sample	Method
a.	Pad lift and cracks associated with pad lift	Acceptable if the following conditions are met: - epoxy technology, and -pads of PTH or via or blind via, and after thermal stress, and -height of pad lift ≤ 40 µm, and -cracks associated to pad lift do not touch the hole wall -cracks meet requirements 10.6.2.	Location: coupon A/B + A/Bi Condition: set 1 AR+RW; set 2 SB Frequency: per panel	Microsection and Microscope Magnification: x200 min Lighting: bright and dark field

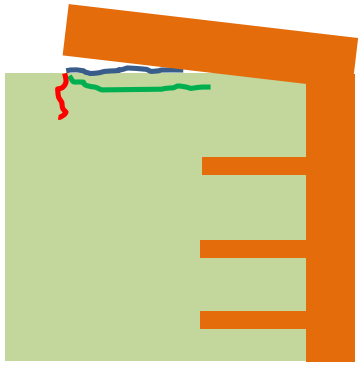


Figure 10-40: Pad lift schematic

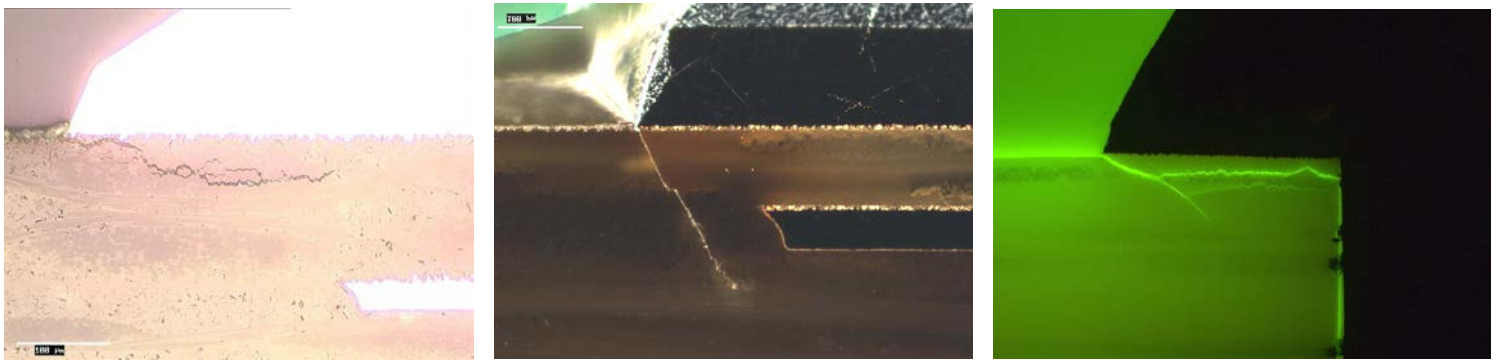


Figure 10-41: Examples of pad lift cracks. The right image is unacceptable because cracks continue until the hole wall

Note 1: The background for pad lift to occur on epoxy technology is because the Tg of the material is below the solidification temperature of solder. Therefore the thermal expansion (above Tg) is high, while the solder has already solidified (during cooling).

Note 2: Blue line: Adhesive failure between copper and dielectric. This is named “pad lift” or ”lifted lands”. Green line: Horizontal crack or void of any size in dielectric under the pad. This is included as “pad lift”. In case crack protrudes from underneath the pad or into the glass reinforcement, it is evaluated as a “laminate crack” as per Table 10-26. Red line: Vertical crack in dielectric extending from the edge of the pad. This is named “laminate crack” and it is covered in Table 10-26.

Table 10-26: Dielectric cracks

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Drilling crack Standard PCB technology	≤ 80 µm	Location: coupon A/B + A/Bi Condition: set 1 AR+RW; set 2 SB Frequency: per panel	Microsection and Microscope Perform inspection under dark field to locate any cracks. Perform measurement of crack length in bright field at 500x magnification. Determine remaining insulation distance as per 10.6.3c and 10.6.3d
b.	Drilling crack HDI PCB technology	≤ 50 µm and ≤ annular ring		
c.	Crack associated with the end of a conductor pattern	≤ 80 µm and referee test 4 microsections in the spare PCB after SB shall not show cracks more than 80 µm		
d.	Random cracks in the dielectric	≤ 80 µm and referee test 4 microsections in the spare PCB after SB shall not show cracks.		
e.	Multiple adjacent cracks	≤ 80 µm and evaluated as a single crack		
f.	Any crack in z-direction	≤ 80 µm and not crossing glass reinforcement		
g.	Remaining insulation distance	In conformance with the PCB definition dossier		

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method

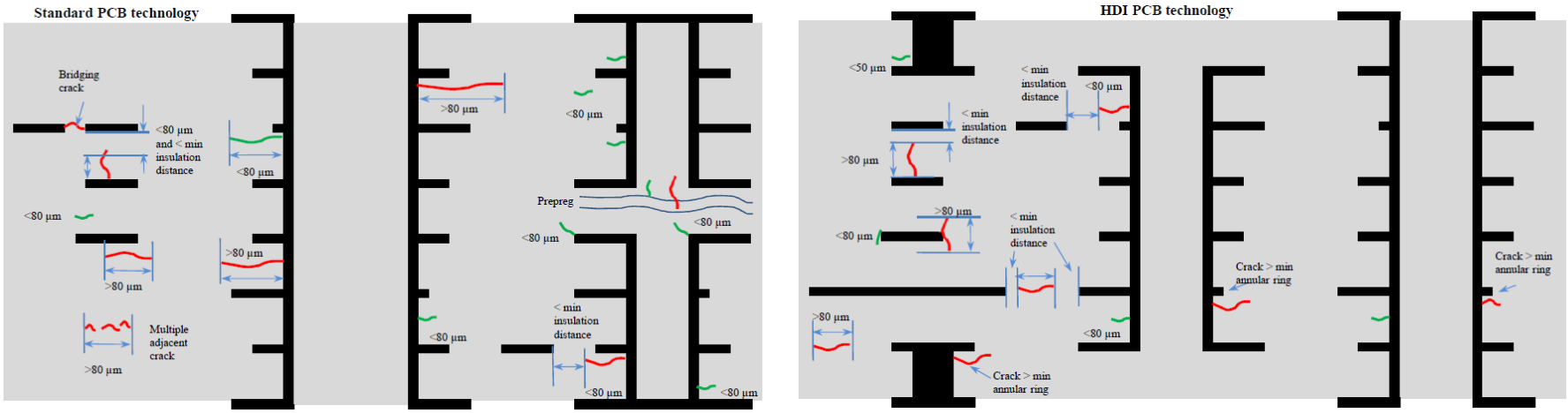


Figure 10-42: Acceptable (green) and non-acceptable (red) dielectric cracks

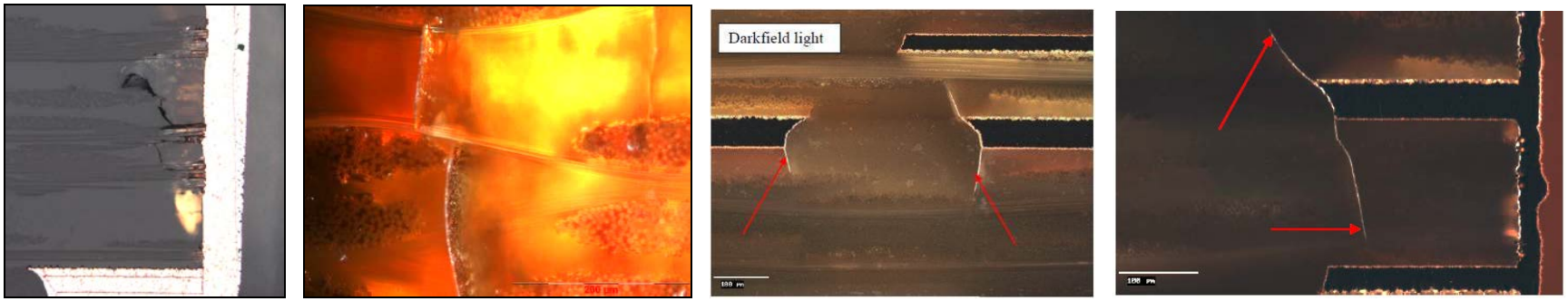


Figure 10-43: Examples of laminate cracks

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
Note 1: The PCB definition dossier is in conformance with the DRD of ECSS-Q-ST-70-12 annex A. The insulation distance specified in the PCB definition dossier is in conformance with ECSS-Q-ST-70-12 Table 13-7.				
Note 2: Cracks can be observed at the end of conductor patters, in particular when using thick copper profile and resin-rich areas. Random dielectric cracks can be observed in specific prepreg materials.				
Note 3: Multiple adjacent cracks are evaluated as a single crack from start of one crack until the end of the adjacent crack, as shown in Figure 10-42.				
Note 4: Referee testing is performed by microsectioning and microscopic inspection of a spare PCB in conformance with this table.				

Table 10-27: Cracks and separation in copper

Ref	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Cracks in internal and external copper foil	Not acceptable	Location: coupon A/B + A/Bi Condition: set 1 AR+RW; set 2 SB Frequency: per panel	Microsection and Microscope Magnification: x 200 min Lighting: bright field
b.	Cracks in copper plating including barrel cracks and corner cracks			
c.	Separation between external copper foil and copper plating	Not acceptable AR, RW, SB Acceptable on vertical edge of foil and on horizontal treatment side of foil in case this has been evaluated by group 6 test in qualification		

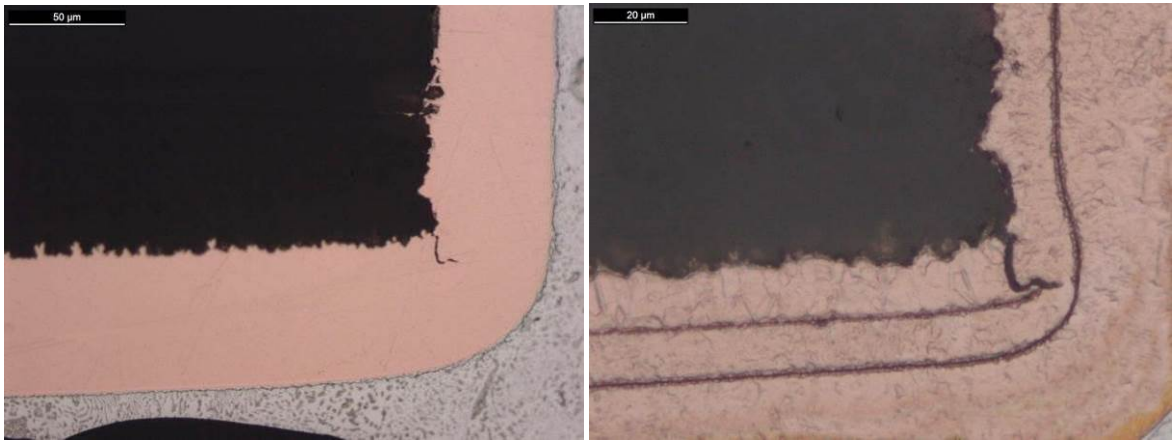


Figure 10-44: Example of C foil separation as-polished and after micro-etch

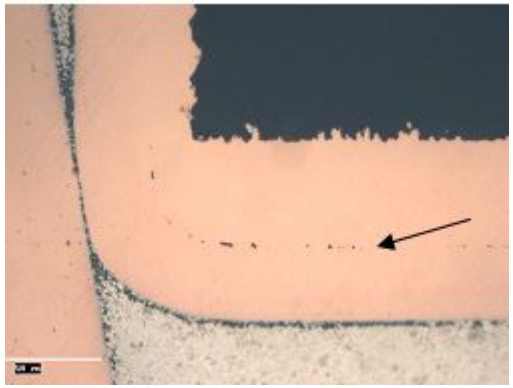


Figure 10-45: Example of interface line between plated copper layers on a non-etched microsection

Note : Interface lines between copper plating layers can occur. ECSS-Q-ST-70-60 does not specify an accept or reject criterion for such feature. It can be justified by group 6 for qualification.

Table 10-28: Interconnect defect, ICD

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Interconnect defect	Not acceptable	Location: coupon A/B and A/Bi Condition: set 1 AR (+RW), set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: x 500 illumination: bright field
b.	ICD in microvia	See Table 10-10 ref e.		

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method

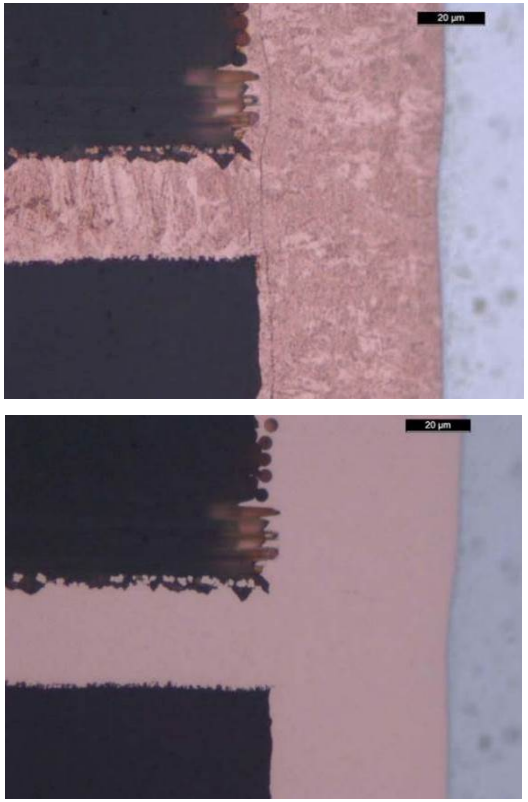


Figure 10-46: Interconnect after stress, target condition, after microetch (top) and as-polished (bottom)

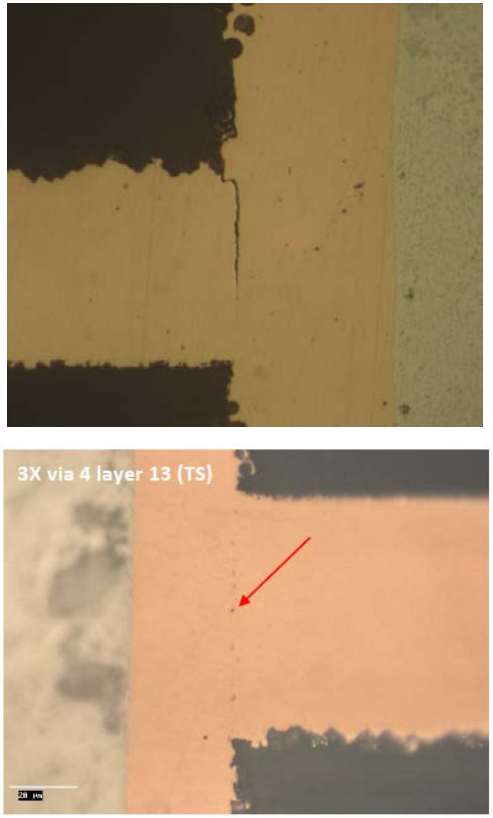


Figure 10-47: Examples of ICD

Note1: It is important for this type of defect that microsections are evaluated in as-polished condition. Microetching can be done to determine the exact interface once a defect has been observed. However, an etched microsection is not suitable for initial evaluation for ICD since it always shows an interface line between foil and plating.

Note 2: ICD is not to be confused with smear.

Table 10-29: Smear

Ref.	Technological feature	Acceptance criteria	Sample	Method
a	Smear	Polyimide and Epoxy: no smear accepted ≤ 10 % smear is acceptable on PTFE based resins ≤ 25% smear is acceptable on PTFE based resins in case the additional horizontal microsection shows ≤ 33 % smear in the circumference	Location: coupon A/B + A/Bi Condition: set 1 AR (+RW), set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x min Lighting: bright field

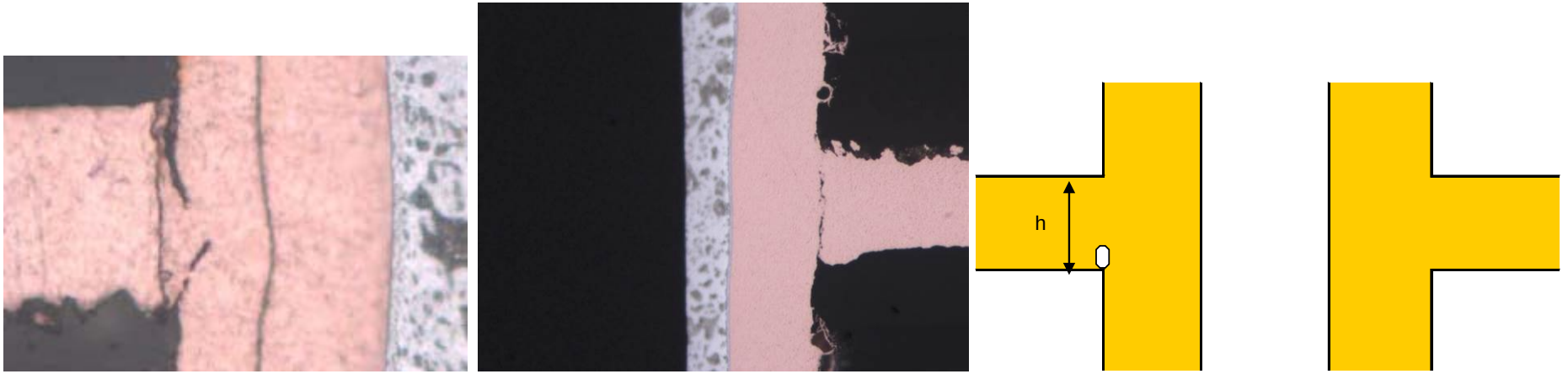


Figure 10-48 Example of smear

Note: In case 10-25 % smear is observed, an additional horizontal microsection is taken to verify the extent of smear around the circumference.

Table 10-30: Hole wall pull away and resin recession

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Hole wall pull away or resin recession	≤ 20 % of the sum of dielectric on standard layers Locally acceptable up to 100 % on specific layers in case: - specific layers include heat sink or include dielectric thickness ≥ 200 µm, and - hole wall pull away ≤ 10 µm between hole wall and resin, and - resin recession between hole wall and epoxy resin is ≤ copper thickness of hole wall, and - it has been evaluated by the group 6 test in qualification.	Location: coupon A/B + A/Bi Condition: set 1 RW set 2 SB Frequency: per panel	Microsection and Microscope Magnification: x 200 min illumination: bright field

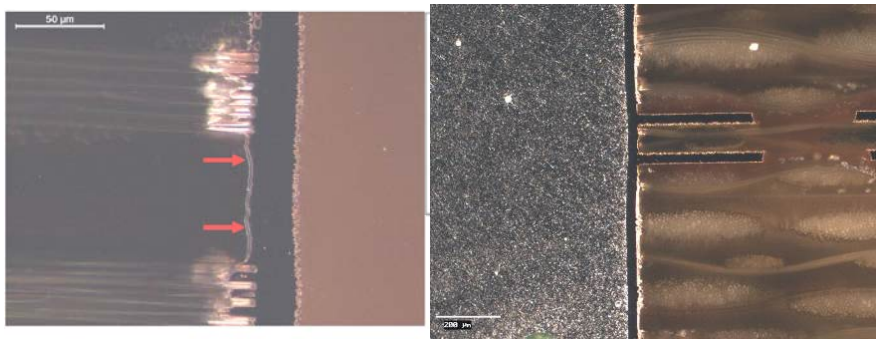


Figure 10-49: Example of hole wall pull away - showing separation of copper in a straight line (left) or slightly bulging outward (right)

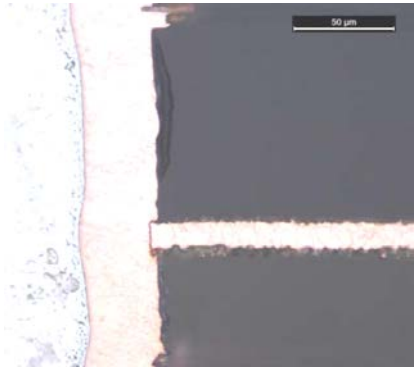


Figure 10-50: Example of resin recession - showing concave retraction of epoxy resin

Note 1	Group 6 on hole wall pull away or resin recession is performed to show absence of cracks in copper and separation between hole wall and resin within the requirement.
Note 2:	The requirement for plated copper thickness is applicable in case hole wall pull away or resin recession causes thinning of the hole wall.
Note 3:	Hole wall pull away can be observed on polyimide resin due to lower adhesion of plated copper to the resin. It can also be observed on epoxy resin. Resin recession can be observed on epoxy resin due to shrinkage of the resin after thermal stress and subsequent separation of the hole wall. Resin recession is not typically observed on polyimide because of the thermal stability of the resin. Hole wall pull away usually appears as a separation of the copper in a straight line or bulging outward from the dielectric. Resin recession usually appears as a concave retraction of the resin.
Note 4:	In case of local layers with 100 % HWPA, the other standard layers have HWPA ≤ 20 % of the sum of the dielectric, as specified in this table. The sum of the dielectric is calculated on the remainder of the standard build-up, i.e. not including the layers where 100% HWPA is permitted.

Table 10-31: Nail heading

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Nail heading	≤ 50 % of inner layer copper thickness	Location: coupon A/B + A/Bi Condition: set 1 AR (+RW), set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: bright field

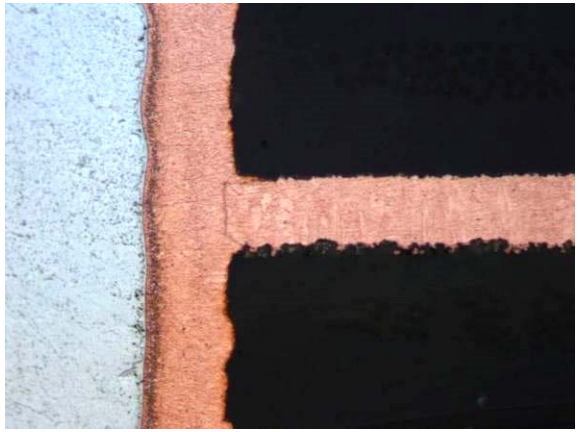


Figure 10-51: Target condition

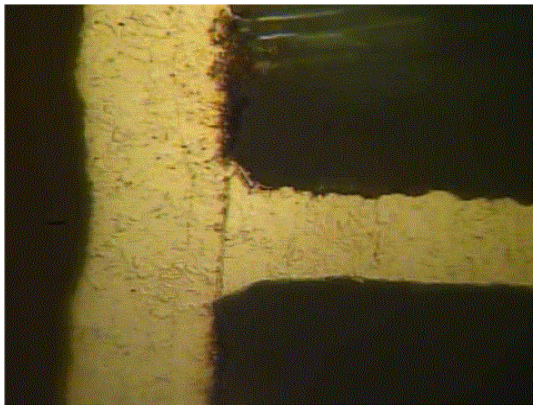


Figure 10-52: Acceptable nail heading

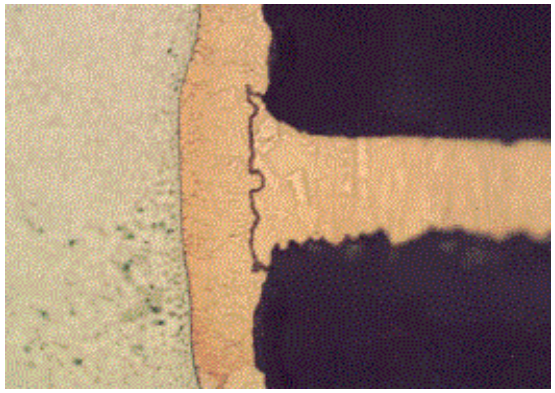


Figure 10-53:Unacceptable nail heading, exceeding 50 % of innerlayer copper thickness

Note:.

Table 10-32: Cu-Invar-Cu

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Nailheading in CIC layers	≤ 50 % of copper thickness on CIC layer	Location: coupon A/B + A/Bi Condition: set 1 AR (+RW) set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 500x illumination: bright field
b.	Separation or contamination between copper on CIC layer and plated barrel	No separation or contamination allowed		
c.	Separation or contamination between Invar layer and plated barrel	≤ 20 % separation/contamination		

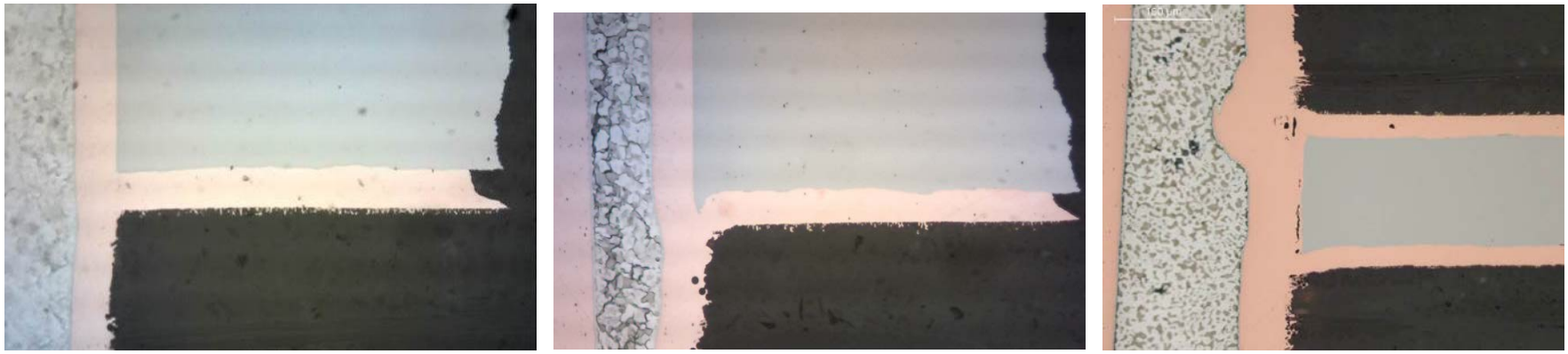


Figure 10-54: Examples of CIC connection, target condition (left), nailheading (middle), separation to CIC (right)

Note: Contamination can be Invar smear, seen as a grey substance between copper and plated barrel

Table 10-33: inhomogeneity in dielectric

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Agglomeration of bromine flame retardant	Unacceptable	Location: coupon A/B + A/Bi Condition: set 1 AR (+RW) set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x illumination: dark field
b.	Agglomeration of filler	Unacceptable		
c.	Swirl or milky appearance in no-flow prepreg	Acceptable in case it has been evaluated by the group 6 test in qualification.		
d.	Demarcation line in no-flow prepreg	Acceptable in case it has been evaluated by the group 6 test in qualification.		

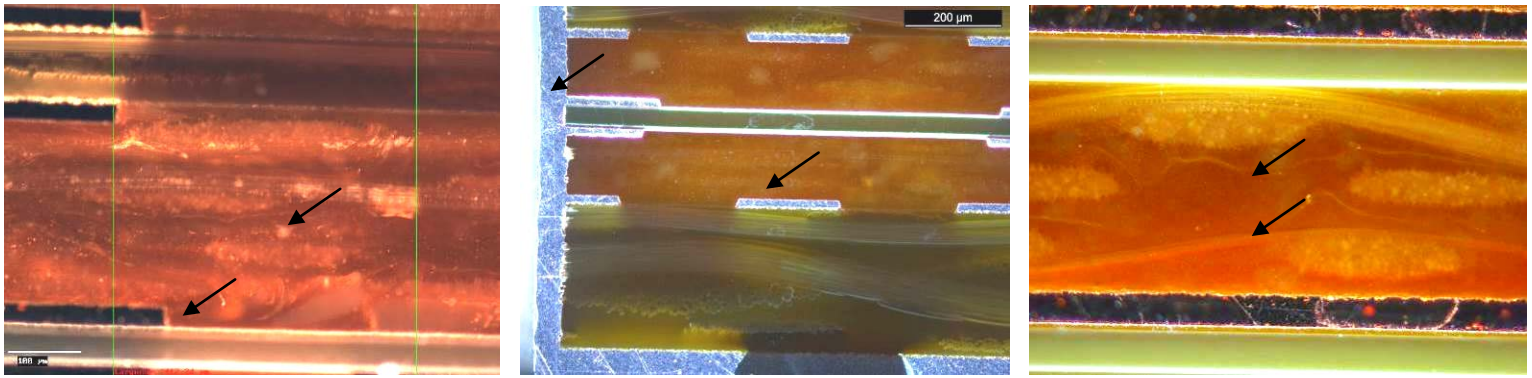


Figure 10-55: Examples of swirl (left and middle) and demarcation line (right). In the middle picture the difference between no-flow prepreg (top) and laminate (bottom) is noticeable.

Note: Cracks are evaluated in conformance with Table 10-26

Table 10-34: contamination or foreign inclusion

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Non-metallic contamination in microsection	Target condition: no contamination Incidental contamination is acceptable if ≤ 80 µm and remaining insulation is in conformance with the PCB definition dossier	Location: coupon A/B + A/Bi Condition: set 1 AR+RW set 2 SB Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x min illumination: bright field
b.	Metallic contamination	Not acceptable		

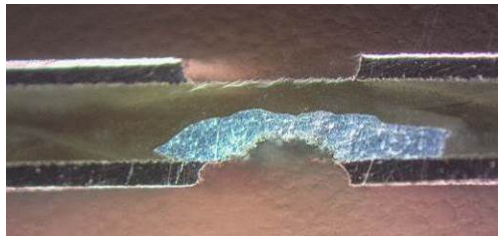


Figure 10-56: Example of metallic contamination in laminate

Note: Fibre contamination cannot be efficiently evaluated in a cross section.

Table 10-35: Rigid-flex interface - delamination between coverlay and prepreg

Ref	Technological feature	Acceptance criteria	Sample	Method
a.	Delamination between coverlay and prepreg	Not accepted	Location: rigid-flex coupon Condition: SB Frequency: per panel	Microsection and Microscope: Magnification: 50 - 200x illumination: dark field or UV fluorescent

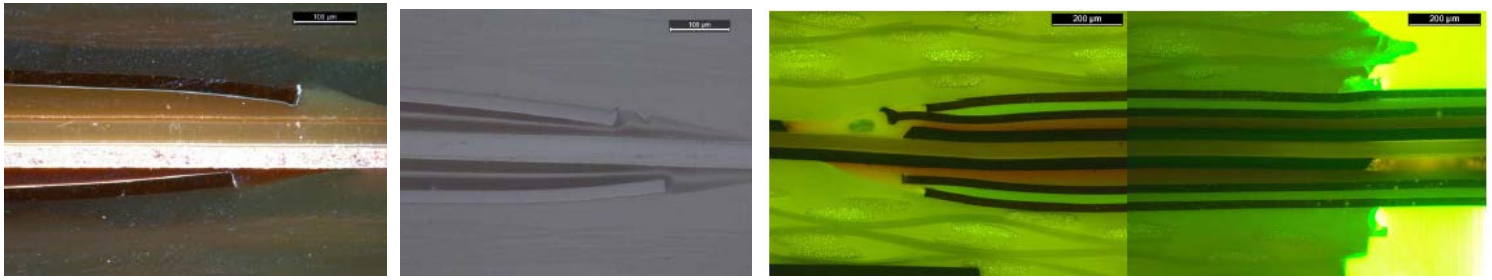


Figure 10-57: Acceptable adhesion between coverlay and prepreg

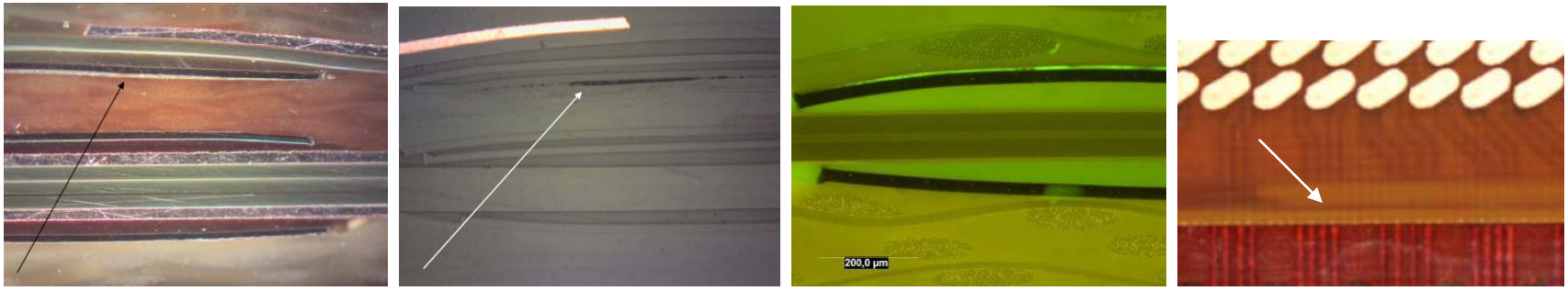


Figure 10-58: Delamination between coverlay and prepreg

Note: Preparation of the microsection can create separation between materials due to mechanical stress.

Table 10-36: Rigid-flex interface -adhesive voids in coverlay and bond-ply

Ref	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Adhesive void in Rigid-flex interface	Target condition: no voids Incidental voids of ≤ 80 µm are acceptable in case the insulation distance is in conformance with the PCB definition dossier	Location: rigid-flex coupon Condition: AR Frequency: 1 per panel	Microsection and Microscope: Magnification: 50 - 200x illumination: dark field or UV fluorescent or bright field

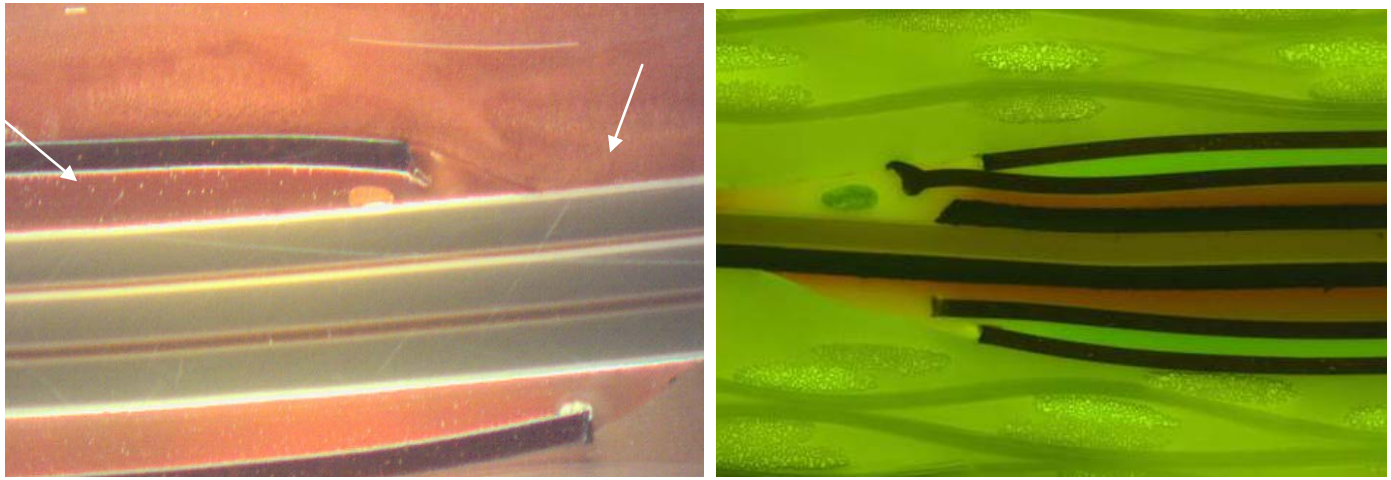


Figure 10-59 Example of voids in acrylic adhesive in rigid-to-flex interface

Note: Bond-ply consist of kapton with adhesive on both sides as indicated in the note of requirement 9.3.e of ECSS-Q-ST-70-12. Only adhesive between copper layers does not provide sufficient insulation.

Table 10-37: rigid-flex interface - misalignment of prepreg

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Resin squeeze out	≤ 1,5 mm	Location: rigid-flex coupon Condition: SB Frequency: per panel	Microsection under magnification
b.	Adhesive filet recession	≤ 0,5 mm into rigid section		

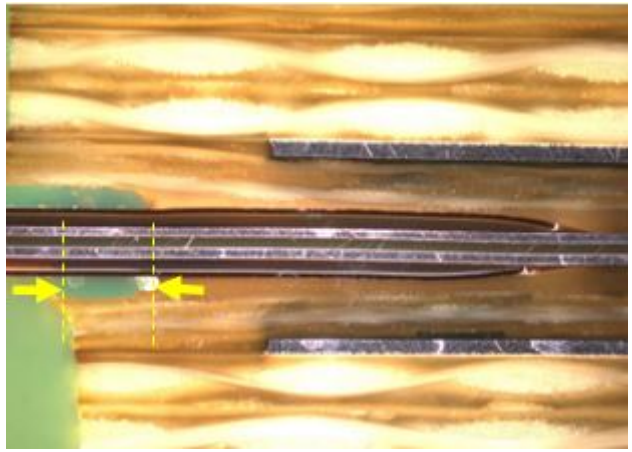


Figure 10-60: Example of adhesive filet recession into rigid section as observed in microsection

Note: These features are also evaluated in visual inspection in conformance with Table 10-48

10.4 Visual inspection

a. For the technological feature conductor width, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with **Table 10-38**.

b. For the technological feature conductor spacing, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with **Table 10-39**.

c. For the technological feature surface metallisation the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-40.

d. For the technological features measling, crazing, blistering and delamination the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-41.

e. For the technological features contamination and inhomogeneity, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-42.

f. For the technological feature scratches, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-43.

g. For the technological features weave exposure, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-44.

h. For the technological feature haloing the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-45.

i. For the technological feature tin-lead surface quality the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-46.

j. For the technological feature marking the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-47.

k. For the technological features rigid-flex interface misalignment of prepreg, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-48.

l. For the technological feature rigid-flex interface fibre protrusion the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-49

m. For the technological feature rigid-flex interface haloing the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-50.

n. For the technological features rigid-flex interface aspect of flex laminate and coverlay the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-51.

Table 10-38: Conductor width

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Peak, nick, pinhole	Acceptable if the following conditions are met: X ≤ 20 % of L Y ≤ L minimum conductor width (L – X) ≥ PCB definition dossier	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥10x X is the as-manufactured conductor width
b.	Conductor width	Tolerance of conductor width is ≤ 20 % in conformance with Table 7-3 from ECSS-Q-ST-70-12		
c.	Peak, nick, pinhole on SMD pad	Not acceptable in pristine area consisting of the middle 80% of the pad		

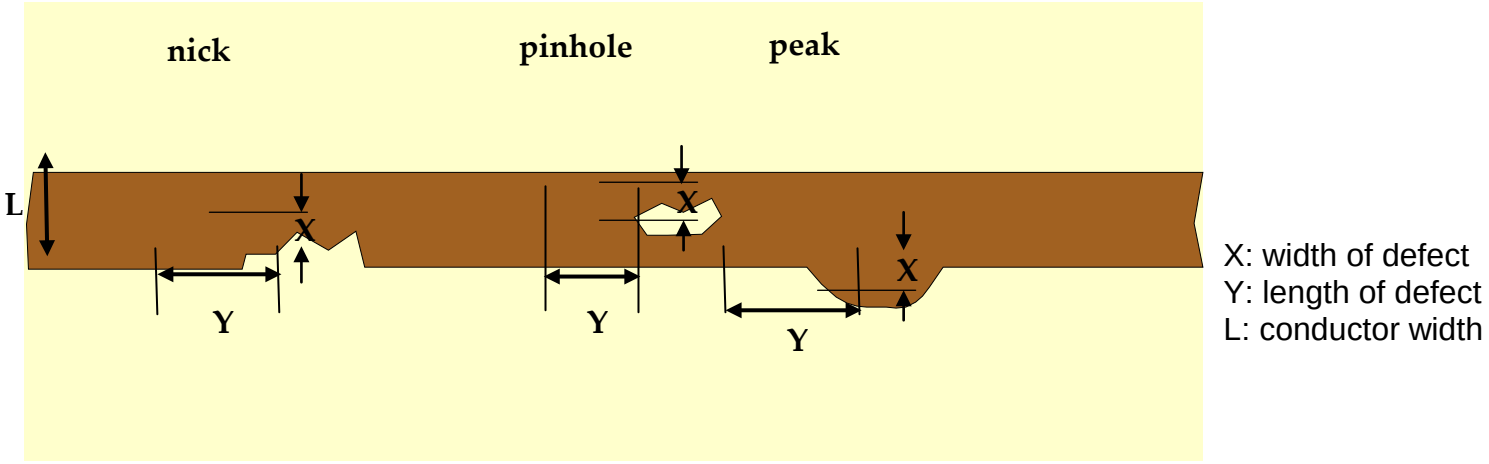


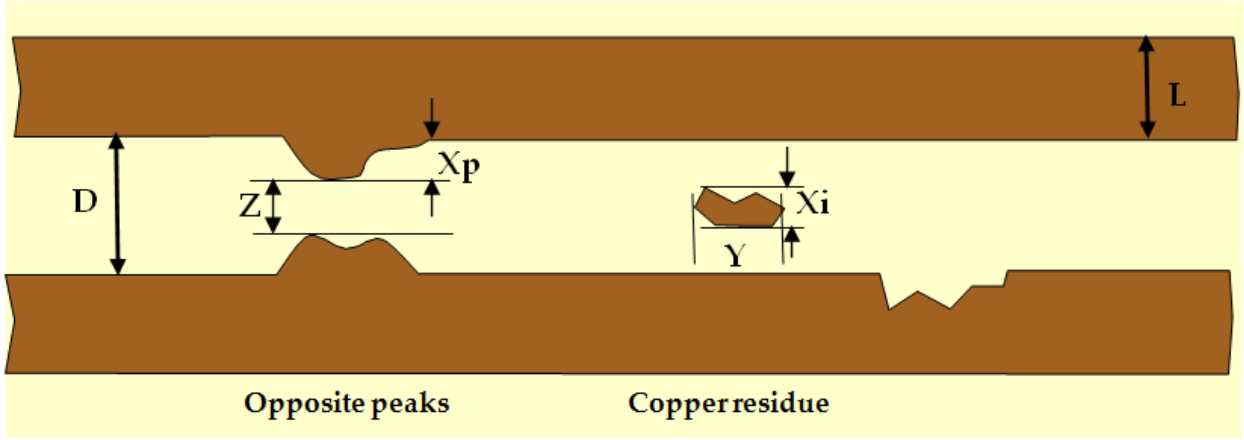
Figure 10-61: Conductor width

Note 1: Intermittent and irregular metallisation defects on conductors include edge roughness caused by peak (synonyms: spike, protrusions , unintentional pattern) or nick (synonyms: indentations, mouse bites, dents) and pinholes (synonyms: voids, pits). Conductors include pads.

Note 2: Probe marks from electrical test are not evaluated as a conductor imperfection.

Table 10-39: Conductor spacing

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Peaks	Acceptable if the following conditions are met: Opposite peaks: Z ≥ 80 % of D Isolated peaks: Xp ≤ 20 % of L minimum remaining spacing Z ≥ PCB definition dossier	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥10x D is the as-manufactured spacing
b.	Conducting island	Acceptable if the following conditions are met: (Xp + Xi) ≤ 20 % of D Xi ≤ 20% of D Y ≤ D Minimum remaining spacing (D – Xi) ≥ PCB definition dossier		
c.	Conductor spacing	Tolerance of conductor spacing is ≤ 20 % in conformance with Table 7-3 from ECSS-Q-ST-70-12		



Xp: width of peak
Xi: width of island
Y: length of defect
L: conductor width
D: insulation distance
Z: remaining insulation distance between defects

Figure 10-62: Conductor spacing

Note: Intermittent and irregular metallisation defects caused by peaks (synonyms: spikes, protrusions , unintentional pattern) or copper residue (synonyms: spurious copper, unintentional pattern, conducting island). Conductors include pads.

Table 10-40: Surface metallization

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Lifting or delamination of conductive pattern from substrate	Not accepted	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Copper or nickel visible on top surface plated areas	Not accepted		
c	Exposed copper on side of conductor	Acceptable		
d.	Corrosion of exposed copper	Not accepted		

Figure 10-63: Example of lifted land

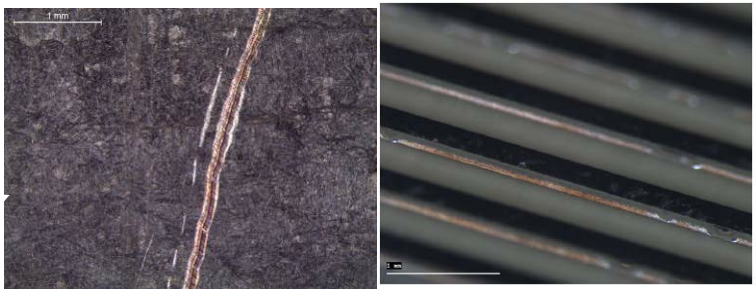


Figure 10-64: Example of visible copper on top surface (left) and on side of track (right)

Note:

Table 10-41: Measling, crazing, blistering, delamination

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Measling, crazing, blistering, delamination	Not accepted	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x

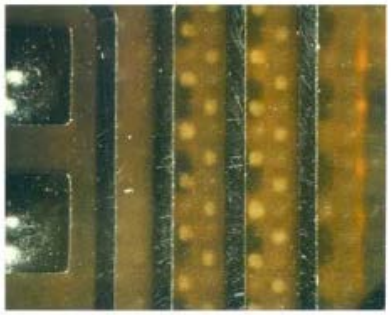
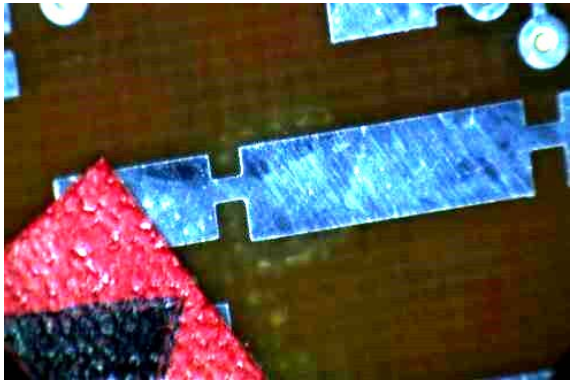


Figure 10-65: Example of measling



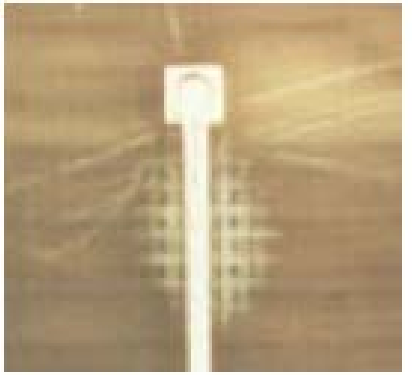


Figure 10-66: Examples of crazing

Note: An isolated white spot is not typical for measling or crazing. Instead, this can be a dry spot, which is not associated with thermal stress, and can be evaluated as inhomogeneity. Measling can be caused by soldering and inadequate bake out.

Table 10-42: Contamination, inhomogeneity

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Non-metallic contamination or inhomogeneity	Accepted with traceability in CoC in case the remaining insulation distance is in conformance with the PCB definition dossier. Numerous inclusions indication poor workmanship is not accepted	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Metallic contamination	Not accepted		
c.	Discoloured copper oxide on underlying layer	Accepted		

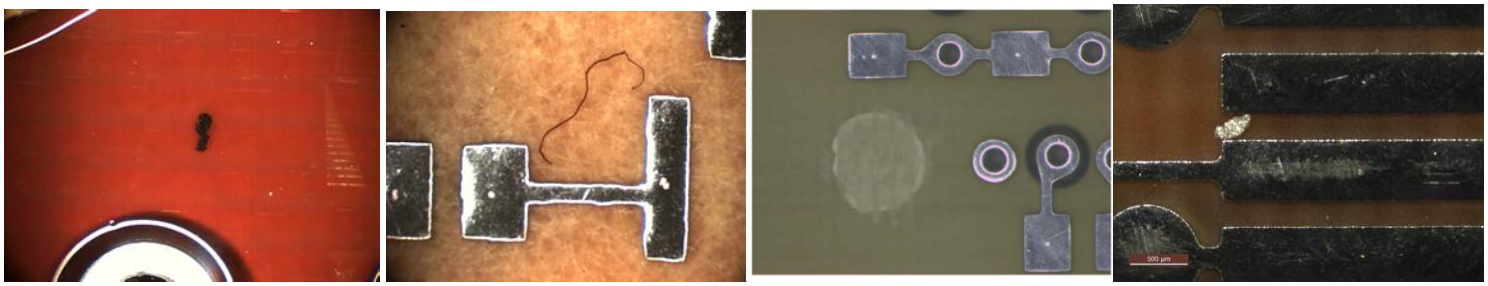


Figure 10-67: Examples of contamination and inhomogeneity

Note 1: The term inhomogeneity is used to describe a different aspect (such as colour) of dielectric material that can be intrinsic to the material, instead of caused by a foreign substance. Discoloured copper oxide is not an inhomogeneity in the dielectric.

Note 2: Occurrence of contamination is a process indicator of raw materials and PCB processes as described in clause 6.6.1

Table 10-43: Scratches

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Scratches on conductors	Target condition: no scratches Incidental superficial scratches are acceptable. Numerous superficial scratches indicating poor workmanship are not acceptable. Scratches exposing copper are not acceptable. Scratches causing smear of SnPb are not acceptable.	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Scratches on dielectric	Target condition: no scratches Incidental superficial scratches are acceptable. Numerous superficial scratches indicating poor workmanship are not acceptable. Scratches causing a sharp indentation or exposure of glass fibres (weave exposure) are not acceptable.		

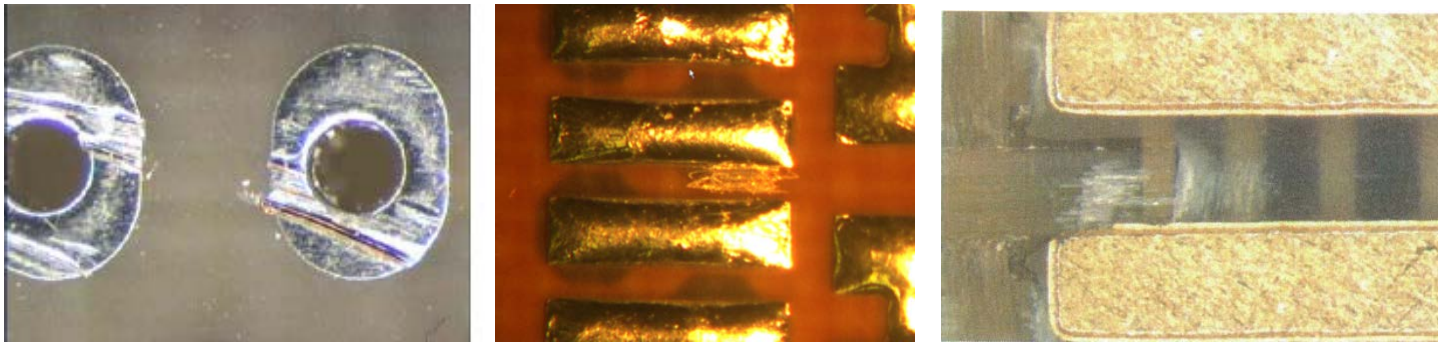


Figure 10-68: Example of scratches on conductors and dielectric

Note: The term scratch refers also to dents and indentations. A cut of conductors is evaluated as a scratch exposing copper. Intentional scratches caused by repair are covered by the clause 6.9. Exposed glass or re-enforcement in laminate not accepted, due to risk for moisture absorption.

Table 10-44: Weave exposure

Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Weave exposure	Not acceptable	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Weave texture	Acceptable		
Note: It can be difficult to distinguish weave texture from weave exposure. See IPC-A-600J clause 2.2.2.				

Table 10-45: Haloing at PCB edge and non-plated holes

Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Haloing adjacent to tracks, pads and planes	≤ 1,5mm into rigid section, and ≤ 50% of the insulation between edge of rigid section to pattern on external layer and the underlying layer.	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Haloing adjacent to footprint for stiffener	≤ 90% of the insulation between edge of rigid section to pattern on external layer ≤ 50% of the insulation between edge of rigid section to pattern on the underlying layer		

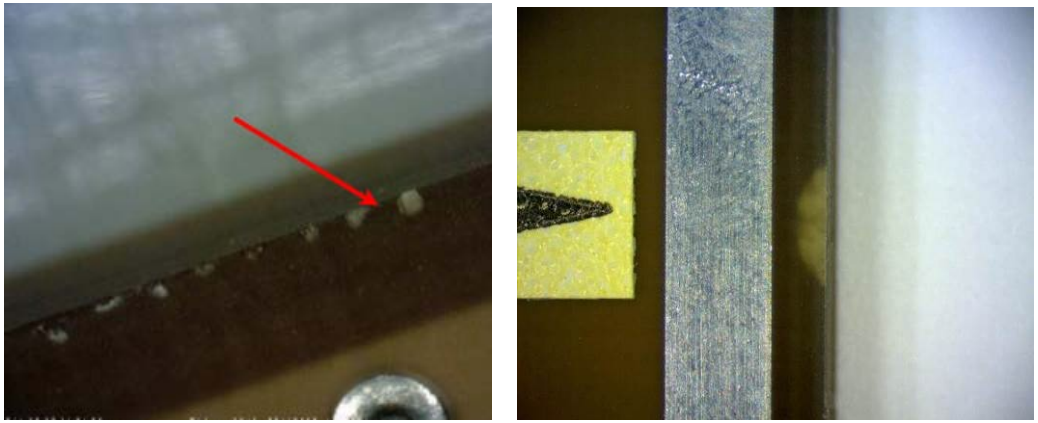


Figure 10-69: Haloing at edge

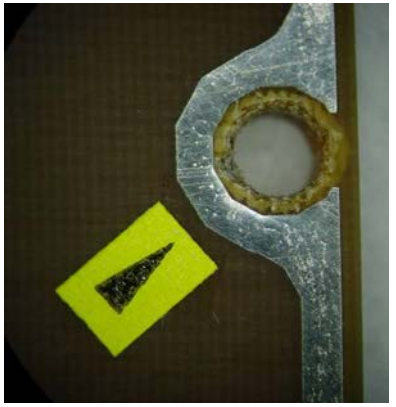


Figure 10-70: Haloing from non-plated hole to footprint for stiffener

Note 1: Depanelisation by cutting of support tabs can cause haloing.

Note 2: PCB edge can also include the edge of non-plated mechanical holes, cut-outs and depth-controlled milling.

Note 3: In case the minimum allowed insulation distance from conductor to PCB edge from clause 14.3.1 of ECSS-Q-ST-70-12 is used, there is almost no allowance for haloing. This is not considered reliable design and is typically indicated as risk factor during MRR.

Table 10-46 Tin-lead surface quality

Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Dewetting and non-wetting	Not accepted on solder pads	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Granular aspects in tin-lead	Accepted in case sample with granular aspect pass solderability test		

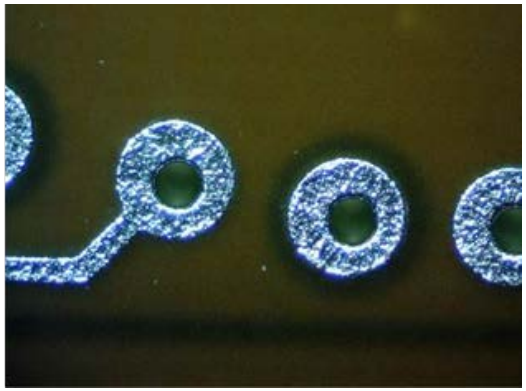


Figure 10-71: Granular aspect

Figure 10-72: Dewetting

Note:

Table 10-47 Marking, identification

Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Marking quality	Clear and legible marking	Location: PCB Condition: AR Frequency: 100 %	Visual inspection under binocular
 **Figure 10-73: Example of unclear marking**				
Note:				

Table 10-48: rigid-flex interface - misalignment of prepreg

Ref	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Resin squeeze out	≤ 1,5 mm	Location: PCB Condition: AR Frequency: 100 %	Visual inspection under binocular
b.	adhesive filet recession	≤ 0,5mm into rigid section		

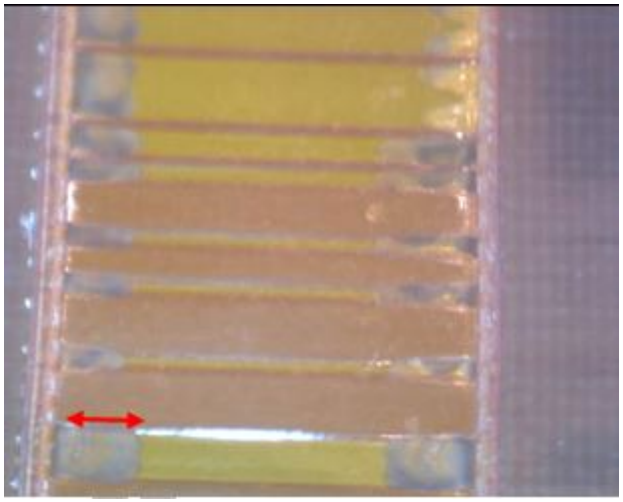


Figure 10-74: Example of resin squeeze out

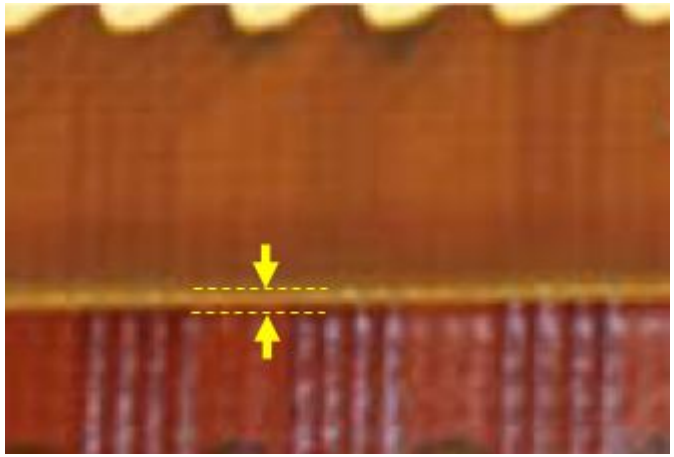


Figure 10-75: Example of adhesive filet recession into rigid section as observed in visual inspection

Note: Resin can be squeezed out of the prepreg during lamination and flow onto the coverlay of the flex section.

Table 10-49: rigid-flex interface - fibre protrusion

Ref	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Fibre protrusion	Target condition: smooth edge incidental fibre protrusion ≤ 1,5mm is acceptable	Location: PCB, rigid-flex coupon Condition: AR Frequency: 100 %	Visual inspection

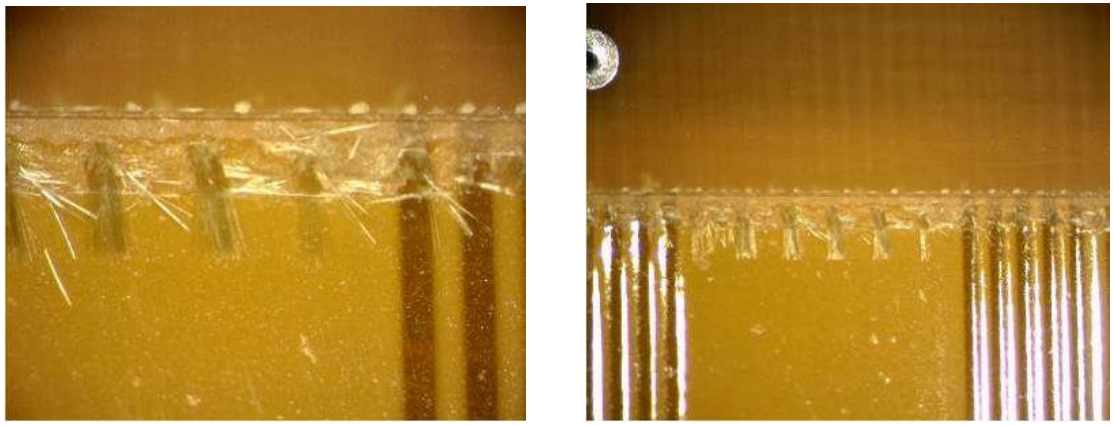


Figure 10-76: Examples of fibre protrusion

Note: Fibre protrusion can be caused by milling when resin is removed but fibres are not cut cleanly.

Table 10-50: Rigid-flex interface - haloing

Ref	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Haloing	≤ 1,0 mm into rigid section, and ≤ 50,% of the insulation between edge of rigid section to pattern on external layer and the underlying layer.	Location: PCB, rigid-flex coupon Condition: AR Frequency: 100 %	Visual inspection under binocular

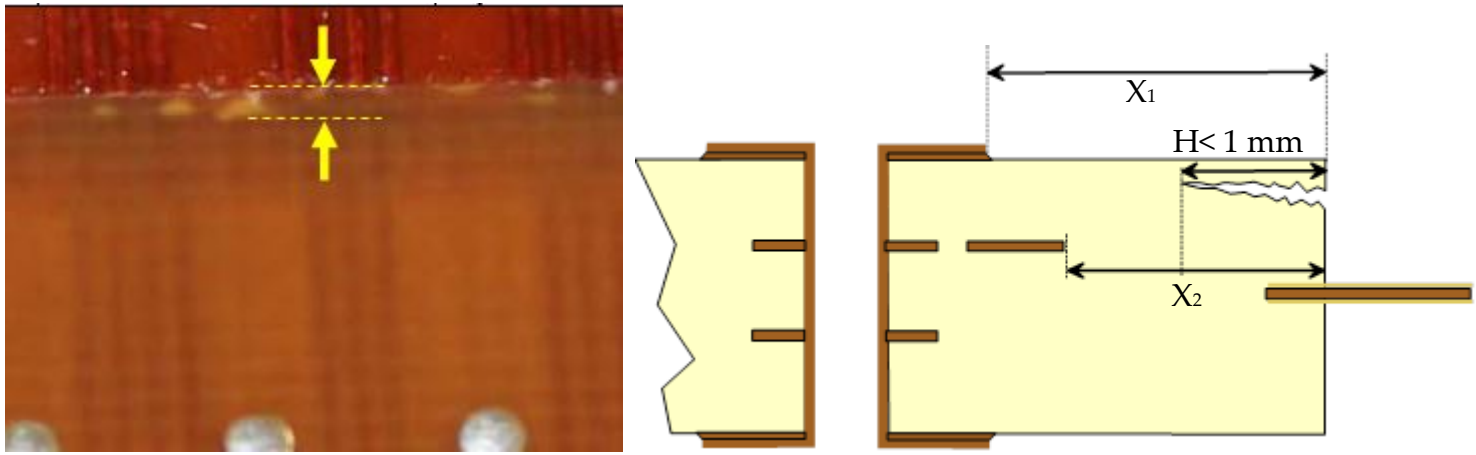


Figure 10-77: Example of acceptable incidental haloing ≤ 1 mm into rigid section

Note 1: Haloing can be seen on all rigid edges. At the rigid-flex interface haloing can be caused by the unsupported milling process. It is good practice to allow for haloing on rigid-to-flex interface and other PCB edges when designing insulation distance from the pattern on external layer and the underlying layer to the edge.

Smallest distance of via to rigid-flex-interface is 2 mm, thus X1 is 1,9 mm, thus H can be up to 1,0 mm, which leaves 0,9 mm remaining insulation distance. Smallest distance X2 of internal layer to rigid-flex interface is as for conductor to hole wall which is 154 µm as manufactured (180 as designed), which gives almost no allowance for haloing. It is needed that the design does not include any conductor (plane of track) closer to the rigid-flex interface than the nearest via.

Table 10-51: rigid-flex interface - aspect of flex laminate and coverlay

Ref	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Scratches, folding marks, blistering, nicks, contamination, voids, white spots	Target condition of coverlay shall be without defect. An incidental defect may be acceptable in accordance with the criteria specified hereunder.	Location: PCB, rigid-flex coupon Condition: AR Frequency: 100 %	Visual inspection under binocular
b.	Scratches, cuts	Accepted if superficial scratch Not accepted if a cut causes a sharp indentation or exposed copper		
c.	Folding marks	Accepted if remaining insulation distance is in conformance with PCB definition dossier.		
d.	Blistering (bubbles)	Accepted if remaining insulation distance is in conformance with PCB definition dossier.		
e	Delamination	not acceptable		
f.	Nicks and burrs on flex edge	acceptable if ≤ 50 % of the insulation between edge of flex section to pattern		
g.	Tear on flex edge	not acceptable		
h.	Voids or pinhole in the kapton of the coverlay	Voids or pinholes are acceptable in case: They are not above or exposing the copper circuit. They are not reducing insulation distance below the requirement specified in the PCB definition dossier.		
i.	Contamination below coverlay	Accepted if remaining insulation distance is in conformance with PCB definition dossier.		
j.	Voids in adhesive from coverlay	Voids of ≤ 80 µm are acceptable in case the insulation distance is in conformance with the PCB definition dossier		
k.	White spots below coverlay	Accepted if remaining insulation distance is in conformance with PCB definition dossier.		

Figure 10-78: Example of an acceptable superficial scratch

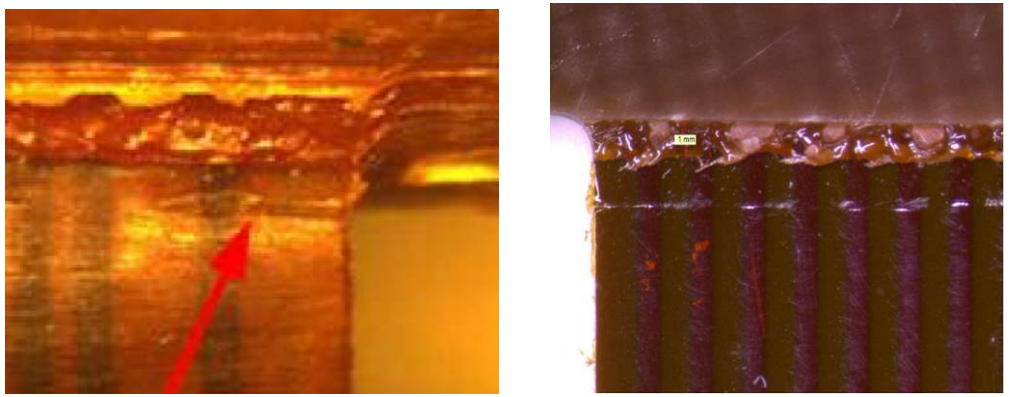


Figure 10-79: Examples of non-acceptable cut and blister, evident by a sharp indentation

Figure 10-80: Examples of burrs on edge of flex

Note 1:	The PCB definition dossier is in conformance with the DRD of ECSS-Q-ST-70-12 Annex A. The insulation distance specified in the PCB definition dossier is in conformance with ECSS-Q-ST-70-12 Table 13-7.
Note 2:	The procurement specification for coverlay is IPC-4203. Chapter 3.5.4. of this specification allows voids up to 75 µm. It is the PCB manufacturer's responsibility to meet the requirement of this table.
Note 3:	Voids in coverlay can be caused by the PCB manufacturer due to mechanical stress**.**

10.5 Visual inspection of sculptured flex PCB

a. For the technological feature misregistration of holes for sculptured flex PCB the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-52.

b. For the technological feature aspect of coverlay for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-53.

c. For the technological feature tin-lead infiltration for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-54.

d. For the technological feature bare copper for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-55.

e. For the technological feature misregistration between pads for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-56.

f. For the technological feature annular ring for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-57.

g. For the technological features conductor width and spacing for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-58.

h. For the technological feature adhesive in plated holes for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-59.

i. For the technological feature aspect of pads for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-60.

j. For the technological features copper wrinkle for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-61.

k. For the technological features aspect of mechanical holes and edge of coverlay for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-62.

l. For the technological feature scratch on coverlay for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-63.

m. For the technological feature aspect of finger after bending for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-64.

n. For the technological feature marking adhesion strength for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-65.

o. For the technological feature microsection for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-66.

Table 10-52: sculptured flex - misregistration of holes

Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method
a	Misregistration of coverlayers	Acceptable if hole diameter is in conformance with PCB definition dossier	Location: PCB Condition: AR Frequency: 100 %	Visual inspection
	Misregistration of hole to conductor	Acceptable if distance D between hole and conductor is ≥ 0,4 mm		

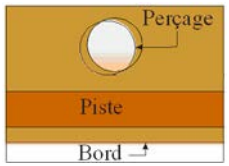


Figure 10-81: Misregistration of top and bottom coverlay

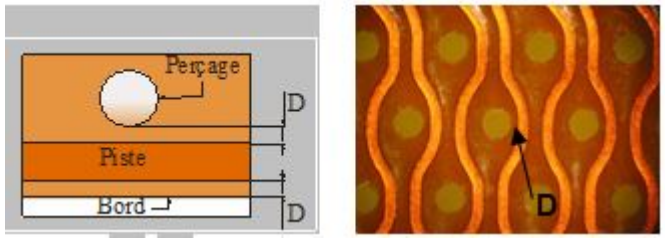


Figure 10-82: Misregistration of hole in coverlay to the conductor

Note:

Table 10-53: sculptured flex - aspect of coverlay

Ref.	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Scratches, folding marks, blistering, nicks, contamination, voids, white spots	Target condition of coverlay shall be without defect. An incidental defect may be acceptable in accordance with the criteria specified hereunder.	Location: PCB Condition: AR Frequency: 100 %	Visual inspection under binocular
b.	Scratches, cuts	Accepted if superficial scratch Not accepted if a cut causes a sharp indentation or exposed copper		
c.	Folding marks	Accepted if remaining insulation distance is in conformance with PCB definition dossier.		
d.	Blistering (bubbles)	not acceptable		
e	Delamination	not acceptable		
f.	Nicks and tears	≤ 50 % of the insulation between edge of flex section to pattern		
g.	Voids or pinhole in coverlay	Voids or pinholes are acceptable in case: They are not above or exposing the copper circuit. They are not reducing insulation distance below the requirement specified in the PCB definition dossier.		
h.	Black spot contamination below coverlay	Not acceptable		
i.	Fibre contamination below coverlay	acceptable if remaining insulation distance in conformance with PCB definition dossier		
j.	Voids in adhesive	Incidental voids of ≤ 80 µm are acceptable in case the insulation distance is in conformance with the PCB definition dossier		

k.	White spots below coverlay	Accepted if: - remaining insulation distance is in conformance with PCB definition dossier - distance to the edge of a conductor is ≥ 0.3mm - maximum two white spots per PCB		

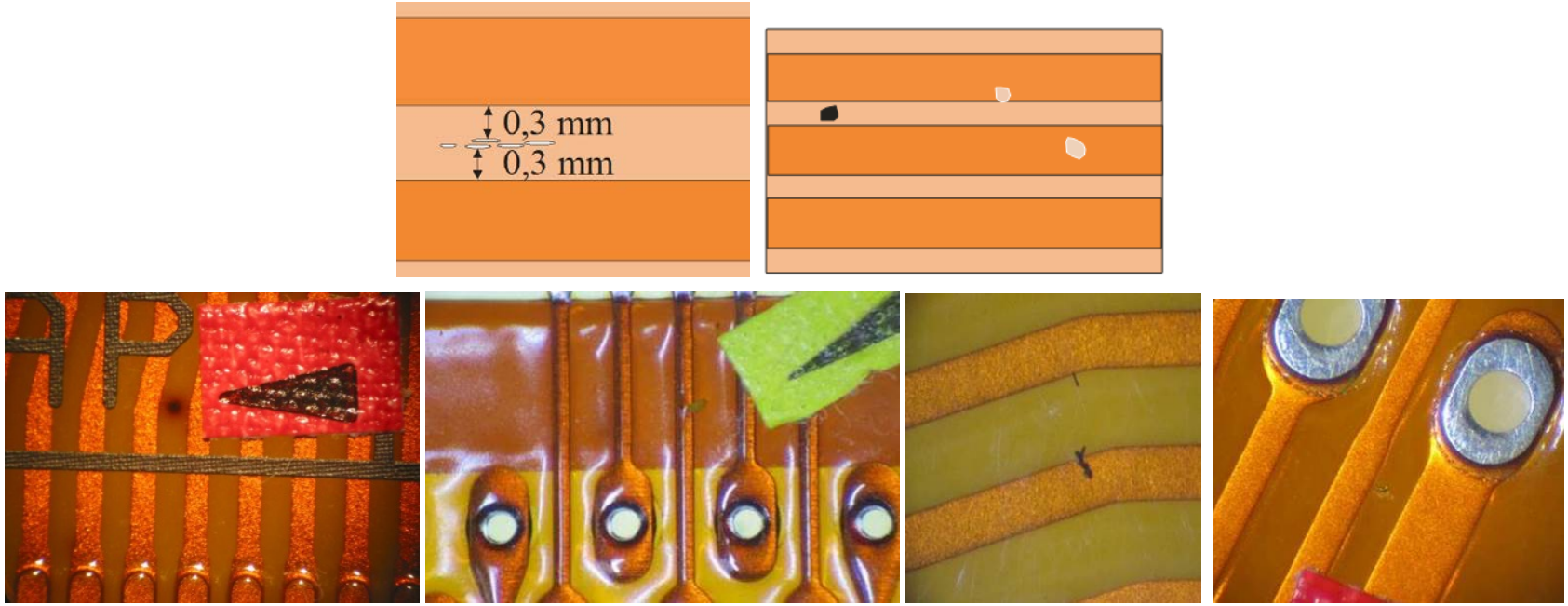


Figure 10-83: Examples of white spot configurations and black spot contamination

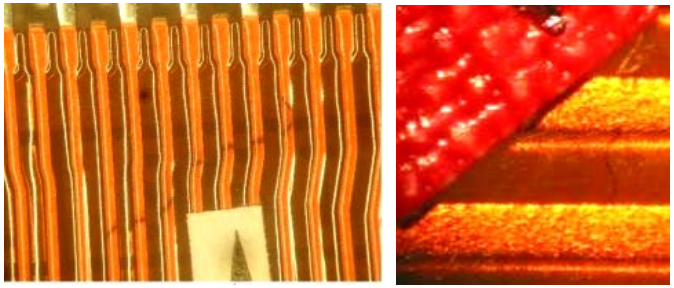


Figure 10-84: Examples of fibre contamination

Note:

Table 10-54: Sculptured flex - SnPb infiltration

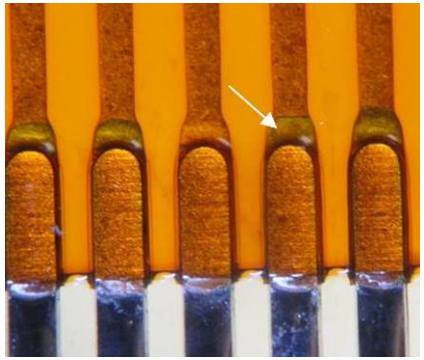
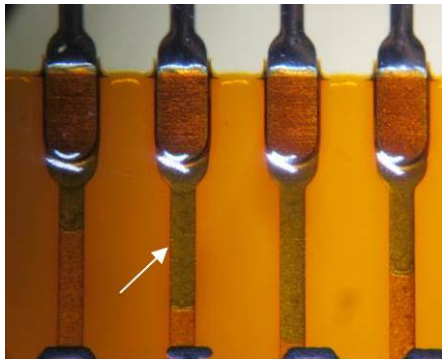
Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method
a.	SnPb infiltration below coverlay	Not acceptable	Location: PCB Condition: AR Frequency: 100 %	Visual inspection
  **Figure 10-85: Examples of SnPb infiltration on sculptured pad (left) and on tracks (right)**				
Note:				

Table 10-55: Sculptured flex - Bare copper on fingers and pads

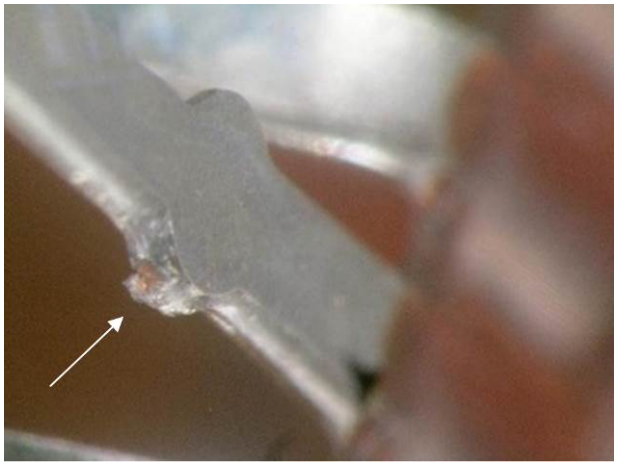
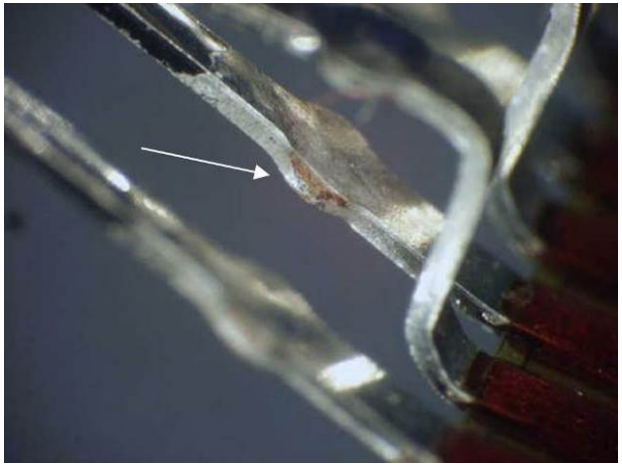
Ref nr	technological feature	Acceptance criteria	Inspection sample	Method
a.	Bare copper on fingers and pads	Not acceptable	Location: PCB Condition: AR Frequency: 100 %	Visual inspection
  **Figure 10-86: Bare copper on fingers**				
Note:				

Table 10-56: Sculptured flex – misregistration between pads

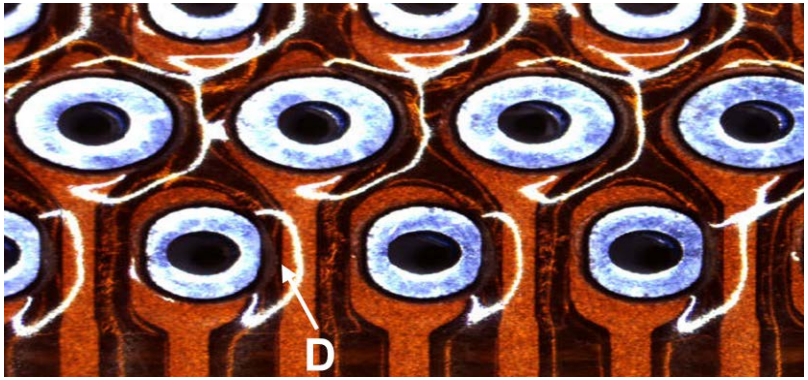
Ref nr	technological feature	Acceptance criteria	Inspection sample	Method
a.	Misregistration between top and bottom pads	Acceptable if - misregistration ≤ 100 µm - insulation distance D between pad and conductor in conformance with PCB definition dossier	Location: PCB Condition: AR Frequency: 100 %	Visual inspection
 **Figure 10-87: Misregistration of pads**				
Note:				

Table 10-57: Sculptured flex – annular ring

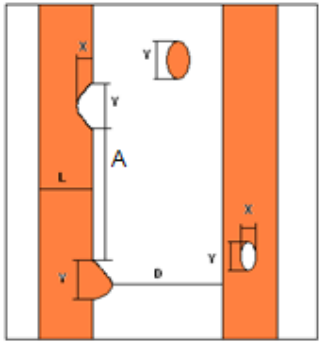
Ref nr	technological feature	Acceptance criteria	Inspection sample	Method
a.	Annular ring on oblong pad on solder side	≥ 150 µm on smallest side ≥ 250 µm on largest side	Location: PCB Condition: AR Frequency: 100 %	Visual inspection
b.	Annular ring on circular pad on solder side	≥ 250 µm		
c.	Annular ring on component side	tangency acceptable in case no adhesive inside the hole, in conformance with 8.7.5e of ECSS-Q-ST-70-12		
				
Note:				

Figure 10-88: Hole misregistration causing reduced annular ring

Table 10-58: Sculptured flex - Copper conductor width and spacing

Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Nicks, peaks and pinholes on conductors	acceptable if all the following are met For designed conductor width ≤ 0,8 mm - X ≤ 25 % of L - Y ≤ 0,5 mm - Z ≤ 50% of designed conductor thickness - distance A between two defects is ≥ 5 mm For designed conductor width ≥ 0,8 mm - X ≤ 20 % of L - X ≤ 0,25 mm - Y ≤ 1 mm. - Z ≤ 50% of designed conductor thickness - distance A between 2 defects is ≥ 5 mm	Location: PCB Condition: AR Frequency: 100 %	Visual inspection
b.	Peaks and copper residue	acceptable if For designed conductor thickness ≥ 250 µm - insulation distance D ≥ 300µm For designed conductor thickness ≥ 200µm - insulation distance D ≥ 250µm For designed conductor thickness ≥ 150µm - insulation distance D ≥ 200µm		
c.	Copper residue to the edge of the flex	acceptable if insulation distance D ≥ 400µm between residue and edge of flex		

Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method
d.	Bump on conductor due to local insufficient etching	Acceptable		
e.	Conductor width and spacing	tolerance of conductor width and spacing is ≤ 20 % in conformance with Table 7-3 from ECSS-Q-ST-70-12		



X: width of defect
Y: length of defect
L: conductor width
D: insulation distance
Z: depth of pinhole
A: distance between

Figure 10-89: Schematic of conductor width and spacing and local defects

Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method

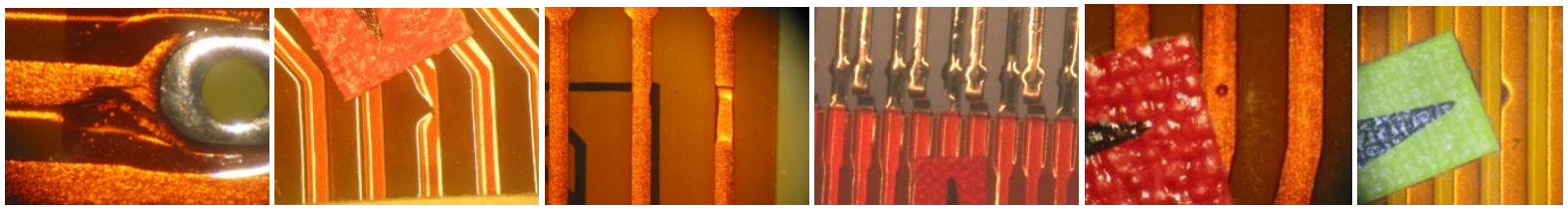


Figure 10-90: Examples of nick near pad, nick on conductor, overetching reducing thickness of conductor, nick on finger, pinhole and local reduced track width (left to right)

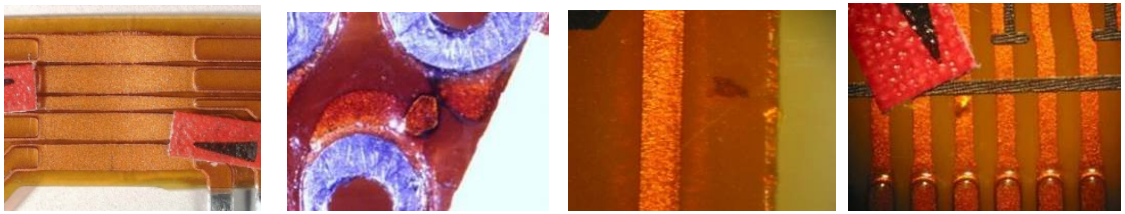


Figure 10-91: Examples of insufficient spacing between conductors, copper residue between pads, copper residue to edge of flex, bump on conductor (left to right)

Note:

Table 10-59: Adhesive in plated holes

Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Adhesive in plated holes	Acceptable if hole diameter is in conformance with PCB definition dossier	Location: PCB Condition: AR Frequency: 100 %	Visual inspection

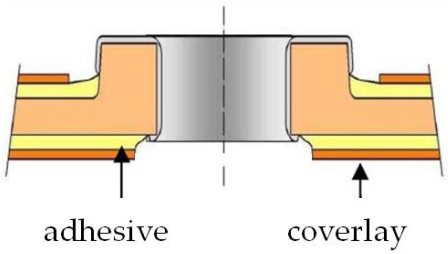
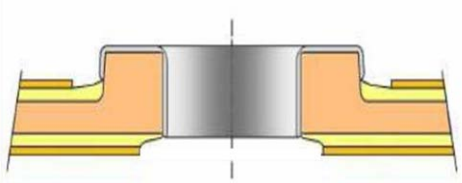
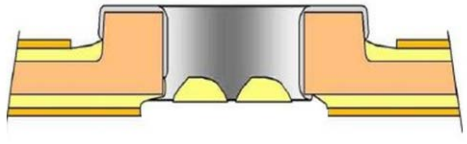
PREFERRED	ACCEPTED	REJECT
No adhesive on the edge of the hole  	Flow of adhesive on the edge of the hole, not reducing its diameter below the requirement. 	Flow of adhesive in the hole, reducing its diameter below the requirement. 

Figure 10-92: Adhesive in plated holes

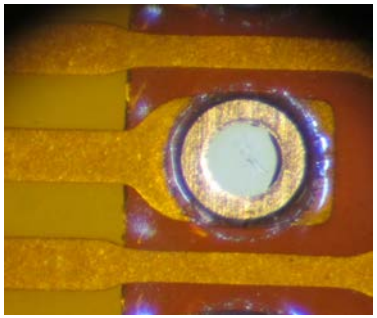


Figure 10-93: Example of adhesive in plated holes

Note:

Table 10-60: Sculptured flex – aspect of pads on solder side

Ref nr	technological feature	Acceptance criteria	Inspection sample	Method
a	Absence of SnPb on pads; Pad diameter reduction due to coverlay or adhesive	Remaining circular pad width ≥ 250 µm Remaining pad width on smallest side of oblong pad ≥ 150 µm Remaining pad width on largest side of oblong pad ≥ 250 µm	Location: PCB Condition: AR Frequency: 100 %	Visual inspection

Ref nr	technological feature	Acceptance criteria	Inspection sample	Method

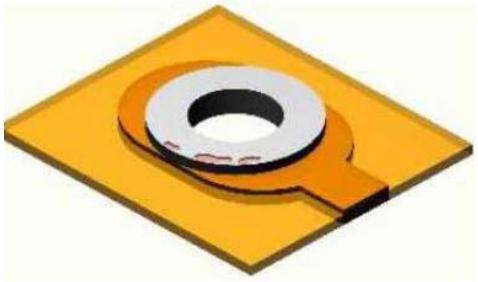
PREFERRED	ACCEPTED	REJECT
Full coverage of SnPb on pads 	Partial coverage of SnPb on pads. Remaining pad width: ≥ 250 µm 	Partial coverage of SnPb on pads. Remaining pad width: < 250 µm 

Figure 10-94: SnPb coverage on pads

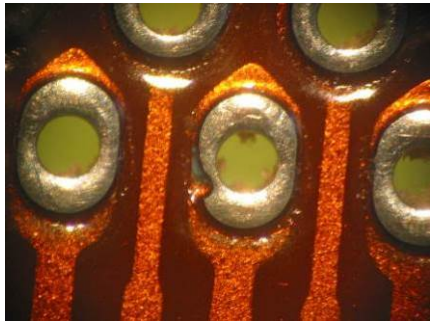


Figure 10-95: Pad diameter reduction due to local coverage by coverlay or resin squeeze out

Note:

Table 10-61: Sculptured flex - copper wrinkle

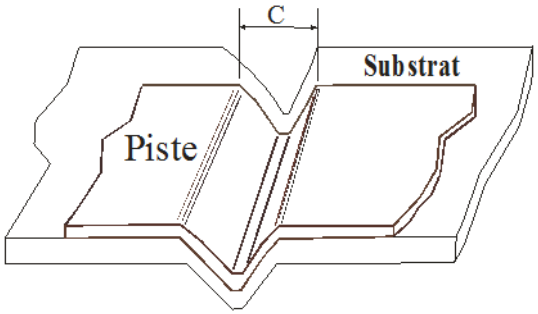
Ref nr	technological feature	Acceptance criteria	Inspection sample	Method
	Copper wrinkle	Not acceptable	Location: PCB Condition: AR Frequency: 100 %	Visual inspection
 **Figure 10-96: Copper wrinkle**				
Note:				

Table 10-62: Sculptured flex – aspect of mechanical holes and edge of coverlay

Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method
a.	nick, burr, tear in mechanical hole in coverlay or on edge of coverlay	Tear not acceptable.	Location: PCB Condition: AR Frequency: 100 %	Visual inspection
b.		Target condition: no burrs Incidental burr on hole acceptable in case diameter meets PCB definition dossier.		
c.		Target condition: no nicks Incidental nick on edge acceptable in case remaining insulation distance to copper ≥ 0,4 mm		

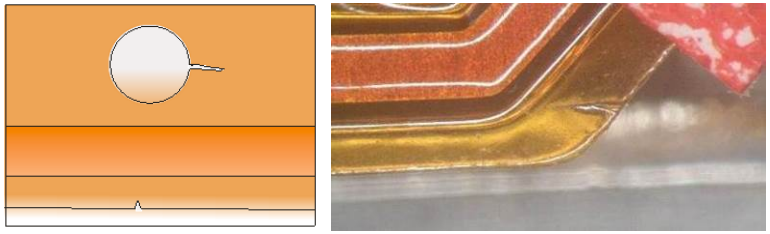


Figure 10-97: Tear in hole and edge of coverlay

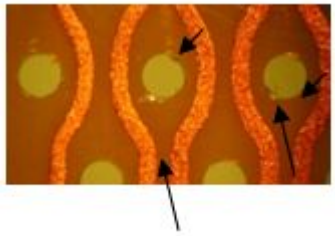


Figure 10-98: Burrs on holes

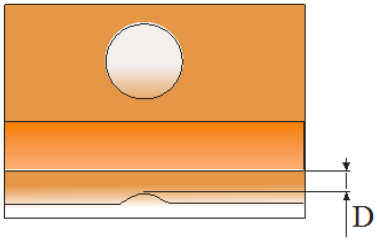


Figure 10-99: Nick on edge of coverlay

Note:

Table 10-63: Sculptured flex – scratch on coverlay

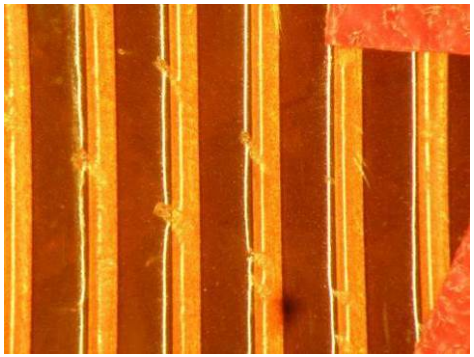
Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Scratches, cuts	Accepted if superficial scratch Not accepted if a cut causes a sharp indentation or exposed copper	Location: PCB Condition: AR Frequency: 100 %	Visual inspection
				
Note:				

Figure 10-100: Coverlay scratch – Non acceptable

Table 10-64: Sculptured flex - aspect of finger after bending

Ref nr	technological feature	Acceptance criteria	Inspection sample	Method
a.	Aspect of finger after bending and SnPb coverage	Exposed copper not acceptable Copper crack not acceptable	Location: PCB Condition: AR Frequency: 100 %	Visual inspection

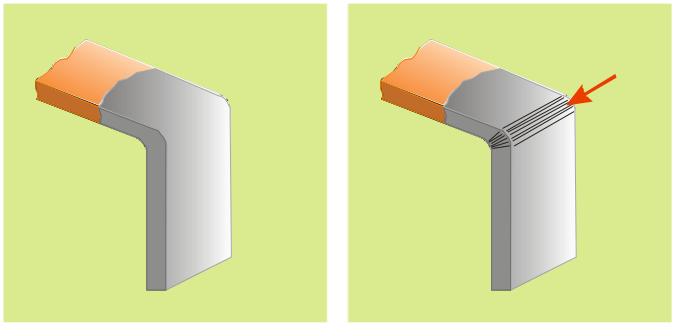


Figure 10-101: Acceptable aspect of finger after bending

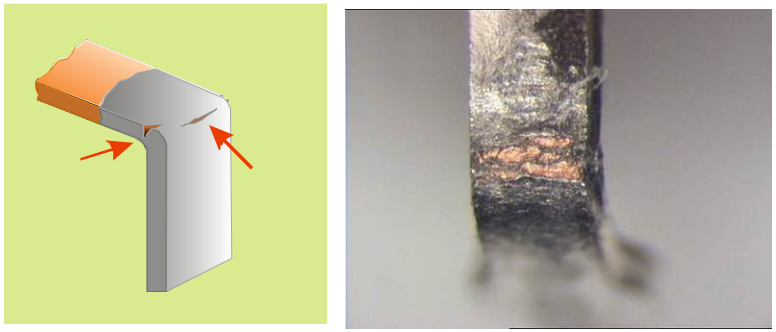


Figure 10-102: Unacceptable aspect of finger after bending

Note:

Table 10-65: Sculptured flex - marking adhesion strength

Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method
a	Marking adhesion strength	No lift of marking	Location: PCB Condition: AR Frequency: 1 per batch	See clause 9.4.5
Note:				

Table 10-66: Sculptured flex - microsection

Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method
a.	Bulk Copper Thickness	as per PCB definition dossier with a tolerance of ± 25 µm	Location: coupon Condition: AR Frequency: 1 per batch	See clause 9.4.5
b.	Copper Conductor Thickness	as per PCB definition dossier with a tolerance of ± 25 µm		
c.	Kapton Base and Coverlay Thickness	25 µm ± 5µm		
d.	Overall Assembly Thickness (No Conductor)	Calculated		
e.	Overall Assembly Thickness (With Conductor)	Calculated		
f.	Tin-Lead Thickness on Surface	7 µm minimum		
g.	Tin-Lead Thickness in Hole	5 µm minimum		
h.	Tin-Lead Thickness on Corners	1 µm minimum		
"Calculated" indicates the addition of individual elements of the build-up.				

Ref nr	Technological feature	Acceptance criteria	Inspection sample	Method

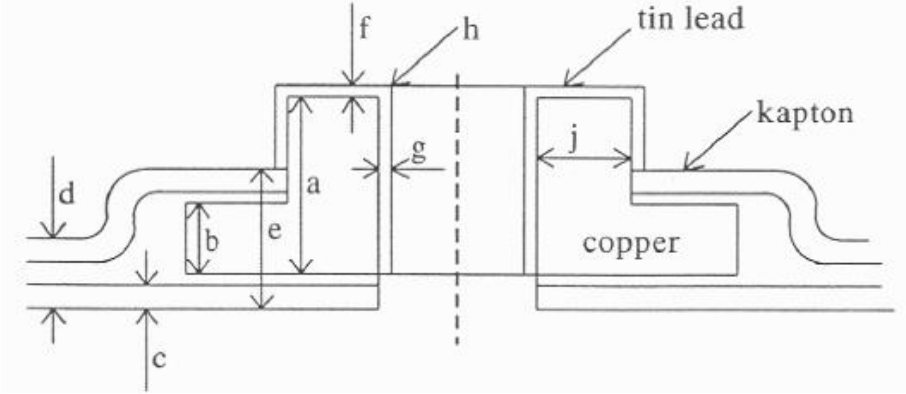


Figure 10-103: Cross section of hole: Copper conductor shown

Note: Ref d and e have been derived to ensure full encapsulation of conductors and total air exclusion from the bond interface by the allowance of use of additional thickness of acrylic adhesive applied on a case by case basis dependent on circuit.

10.6 Additional requirement to the tables

10.6.1 Annular ring

a. Annular ring shall be measured excluding the copper plating, except in the case of requirement 10.6.1b.

b. Annular ring on external layers shall be measured including the Cu plating.

NOTE The measurement method for annular ring is indicated in Table 10-1 and Table 10-2. The reason to include Cu plating in annular ring measurement on external pads is to enable annular ring measurement by visual inspection, whereas the other type of annular ring measurements are performed using microsectioning.

c. On layers without non-functional pad, the distance between the hole wall and the adjacent circuitry shall be in conformance with requirement 13.8.2.g from ECSS-Q-ST-70-12.

NOTE This limits the misregistration of that layer, which cannot be measured without the presence of a pad.

d. The internal annular ring may be ≥25 µm provided that the following conditions are met:

1. it is in conformance with requirement 11.5.2.a of ECSS-Q-ST-70-12;
2. the panel includes registration coupons on all four corners for verification of annular ring in the full circumference.

NOTE 1 The electrical coupon F or R from IPC-2221B allows for such verification. The IST coupon also includes a pattern for electrical registration. Alternatively the verification can be done by X-ray. Microscopic inspection of cross sections only verifies in one direction and does not assess the full circumference.

NOTE 2 Requirement 11.5.2.a of ECSS-Q-ST-70-12 includes teardrop reinforcement and identification of the review item for the PCB definition dossier. The requirement is specified for HDI technology. Therefore a PCB without microvias falls within the HDI technology in case it uses reduced annular ring.

NOTE 3 Table 10-6 and Table 10-26 specify that cracks and wicking cannot be more than the minimum annular ring. Therefore wicking is

limited to 25 µm in case such small annular ring is used.

NOTE 4 This requirement is valid for rigid and flex laminate. Larger movement of flex layers causes higher tolerances for annular ring. Therefore the requirement of 50 µm is reduced to 25 µm. However, this margin cannot be used to justify a design with a smaller pad diameter. The pad diameter is designed as if the annular ring was 50 µm, in conformance with the requirement 7.5.2.h from ECSS-Q-ST-70-12.

NOTE 5 It is preferred to implement the electrical registration coupon on all corners of the panel, which is deemed a more efficient verification of annular ring compared to microsectioning on 2 opposite corners. To accommodate the recurrent designs without electrical registration coupons, the annular ring requirement of 50 µm is maintained for that technology.

10.6.2 Pad lift and associated laminate cracks

a. Pad lift shall not be acceptable except for the case specified in Table 10-25.

NOTE 1 The types of pads for which allowance for pad lift is specified are specified in Table 10-25 ref a and ref b. This requirement does not include SMT pads. Pad lift on SMT pads evaluated in a PCB is, therefore, not acceptable. SMT pads are not included on coupons.

NOTE 2 The occurrence of pad lift on "blind via in SMT pad" is evaluated as for a component hole.

b. The height of the pad lift shall be in conformance with Table 10-25 requirement a.d.

c. The height of the pad lift shall include adhesive separation between pad and resin as well as cracks or voids due to cohesive separation inside the dielectric.

d. In case cohesive or adhesive separations are not clearly identifiable, the angle of the pad may be used to calculate the height of the pad lift.

e. The parts of cracks or voids protruding from underneath the pad shall be evaluated as dielectric cracks in conformance with the Table 10-26.

f. Cracks in the laminate underneath SMT pads shall be evaluated as dielectric cracks, in conformance with the Table 10-26.

g. Cracks associated with pad lift shall be evaluated after group 6 test.

NOTE This provides an evaluation that the cracks associated with pad lift do not propagate until the hole wall after group 6. Propagation of cracks until the hole wall increases the risk of further propagation along the hole wall and potential rupture of innerlayer connections.

h. Cracks associated with pad lift shall not reach the hole wall before or after thermal stress.

i. The parts of cracks or voids underneath the pad associated with pad lift shall not reduce the insulation distance to adjacent circuitry below the values specified by the PCB definition dossier, in the DRD of ECSS-Q-ST-70-12 annex A.

NOTE The insulation distance specified in the PCB definition dossier is in conformance with ECSS-Q-ST-70-12 Table 13-7.

NOTE It is good practice that technology prone to pad lift is designed with margin such that the potential pad lift does not reduce the insulation between component holes and adjacent circuitry.

NOTE Polyimide rigid-flex PCBs that use many layers of no-flow prepreg can be prone to pad lift due to high thermal expansion in z-direction and low Tg of the material. Alternative processes or materials can be investigated with the PCB manufacturer to avoid pad lift.

10.6.3 Miscellaneous

a. Any defects that are specified within ECSS-Q-ST-70-60 to be acceptable after group 6, shall also be acceptable after group 4.

b. The plating in microvias shall be evaluated in conformance with Table 10-11 in high density and low density footprint.

NOTE Microvias in low density footprint are included in coupons from set 1 and set 2. Microvias in high density footprint are included in the IST coupon, which can be microsectioned after IST test.

c. Remaining insulation distance shall be the sum of insulation distances to conductors that are not affected by cracks.

d. Insulation from crack to adjacent conductor of less than 20 µm shall not be included in the calculation of remaining insulation distance for ref g from Table 10-26.

NOTE This is specified because cracks closer than 20 µm to a conductor are at risk to be in contact with the conductor out-of-plane from the microsection. In case the crack is further separated from adjacent conductors than 20

µm, the remaining insulation distance can be calculated by addition of the insulation on both sides of the crack to adjacent conductors. An example is shown in Figure 10-104, which is a zoom from Figure 10-42. In case both a) and b) are > 20 µm, the remaining insulation distance equals c) minus the length of the crack. In case a) is < 20 µm, the remaining insulation distance equals b).

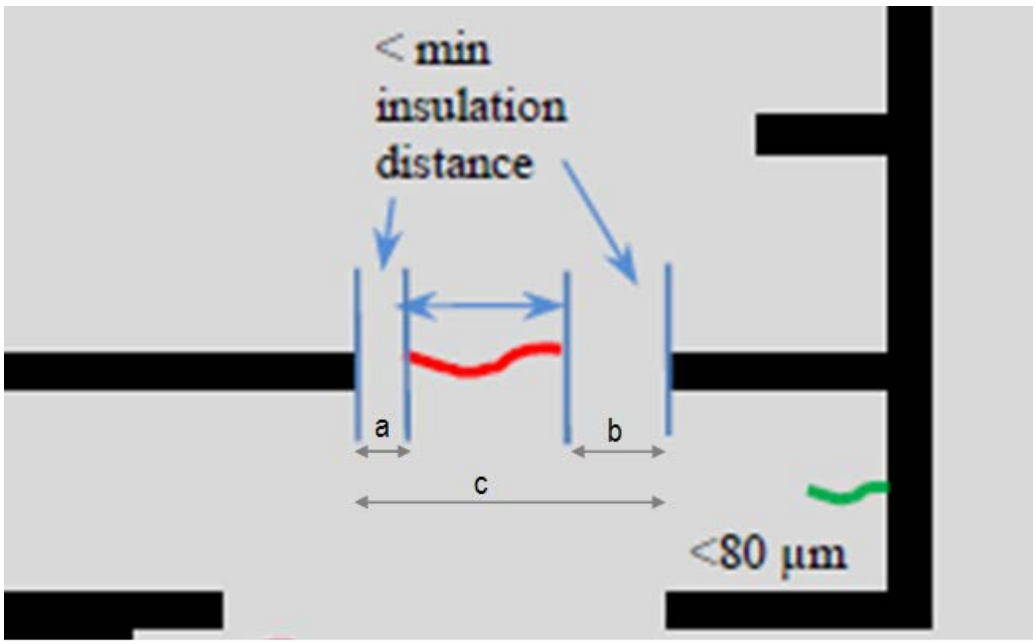


Figure 10-104: Calculation of remaining insulation distance

e. Component holes with a diameter of > 0,6 mm shall meet the requirement for finished hole diameter from the PCB definition dossier.

NOTE These hole diameters cannot be reduced by a bulb of SnPb.

f. Plated holes with a diameter ≤ 0,6 mm may have a reduced diameter due to blocking with SnPb.

NOTE In some applications, such as for nano-D connectors, PTH are used with a diameter ≤ 0,6 mm with SnPb surface finish. In this case it is important to review the finished hole diameter. It is the responsibility of the PCB manufacturer in case such design is specified in the PCB definition dossier and accepted in the MRR, in which case it is good practice to raise it as a review item.

g. Coverlay and its adhesive may partly cover the pad of flexible PCBs in case the annular ring is in conformance with clause 8.5.1 from ECSS-Q-ST-70-12 and Ref d from Table 10-2.

NOTE Minimum annular ring is 250 µm on a component hole and 100 µm on a non-soldering hole.

h. The customer may specify a requirement for maximum copper thickness in the PCB definition dossier.

NOTE ECSS-Q-ST-70-60 and ECSS-Q-ST-70-12 do not specify a maximum copper thickness for plated layers. This could be important for HDI layers, thermal performance of PCBs or for RF applications. Copper thickness on plated layers (internal/external) can be influenced by pattern design and value above maximum are acceptable in case all other requirements like dielectric thickness, undercut, conductor width/space are achieved.

i. In case of overhang of Au or Ni/Au in conformance with Table 10-15, the assembled PCB shall be conformal coated.

NOTE Overhang occurs when Au or Ni/Au is plated before etching. To avoid overhang, the plating can occur after etching, in which case the circuit to be plated is designed to enable electrical connection. Brushing of overhang is not allowed in conformance with requirement 6.9.2m and its note. Other surface finishes, such as ENEPIG, are available that do not cause any overhang. This is necessary on RF PCBs in case conformal coating is not desired.

Annex A (normative)
Qualification letter – DRD

A.1 DRD identification

A.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-60, requirement 5.11a.

A.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the qualification letter.

A.2 Expected response

A.2.1 Scope and content

a. The qualification letter shall contain the following:

1. Date of issue;
2. Contact details of PCB manufacturer and qualification authority;
3. Reference to request of qualification;
4. Reference to evaluation test report;
5. Reference to audit report;
6. Reference to qualification test report;
7. Qualified technology;
8. PID reference;
9. Qualification period.

A.2.2 Special remarks

None

Annex B (normative)
CoC – DRD

B.1 DRD identification

B.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-60, requirement 8.3a.

B.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the CoC and its lab reports.

B.2 Expected response

B.2.1 Scope and content

B.2.1.1. CoC

a. The CoC shall contain the following:
   1. Declaration of conformance, in conformance with B.2.1.1;
   2. Lab report for visual inspection of PCBs for qualitative aspects, in conformance with B.2.1.3;
   3. Lab report for visual inspection of PCBs for dimensional verification, in conformance with B.2.1.4;
   4. Lab report for microsection of coupons for qualitative aspects, in conformance with B.2.1.5;
   5. Lab report for microsection of coupons for dimensional verification, in conformance with B.2.1.6;
   6. Lab report for additional tests, in conformance with B.2.1.7.

b. The CoC shall cover the batch or a subset.

B.2.1.2. Declaration of conformance

a. The declaration of conformance shall include the following:
   1. Declaration of conformance to ECSS-Q-ST-70-60;
   2. Declaration of conformance to the PCB definition dossier;

3. Traceability reference to the PCB definition dossier from procurement authority including revision and issue number;

   NOTE This traceability reference can be named ‘part number’.

4. MRR reference;

5. In case of partial or noncompliance toB.2.1.2a1 B.2.1.2a2 reference to waiver request;

6. Purchase order number from procurement authority;

7. Traceability reference from PCB manufacturer;

   NOTE This traceability reference can be named ‘batch code’.

8. Date code, as per the following format: YYWW;

   NOTE YYWW indicates a two digit reference to year followed by a two digit reference to week number.

9. Quantity of delivered PCBs in the batch;

10. Serial numbers of delivered PCBs in the batch;

11. Signature from PCB manufacturer.

B.2.1.3. Lab report for visual inspection of PCBs for qualitative aspects

a. Lab report for visual inspection of PCBs for qualitative aspects shall include the following:

   1. Arbitrary defects of conductors and pads (mouse bites, dents, nicks, pinhole, unintentional pattern) in conformance with Table 10-38 and Table 10-39;

   2. Lifting of conductor pattern in conformance with Table 10-40;

   3. Copper or nickel visible on top surfaces in conformance with Table 10-40;

   4. Corrosion of copper in conformance with Table 10-40;

   5. Blistering or air bubbles in conformance with Table 10-41;

   6. Delamination in conformance with Table 10-41;

   7. Crazing and measling in conformance with Table 10-41;

   8. Surface contamination or inclusion of foreign matter in conformance with Table 10-42;

   9. Non-homogeneous colour of innerlayer copper in conformance with Table 10-42;

   10. Scratches in conformance with Table 10-43;

   11. Weave exposure in conformance with Table 10-44;

   12. Haloing in conformance with Table 10-45;

13. SnPb surface quality in conformance with Table 10-46;
14. Marking in conformance with Table 10-47;
15. Coverlay registration and annular ring of terminations on flexible PCB in conformance with Ref d from Table 10-2;
16. Rigid-to-flex interface, alignment of prepreg in conformance with Table 10-48;
17. Rigid-to-flex interface, fibre protrusion in conformance with Table 10-49;
18. Rigid-to-flex interface, haloing in conformance with Table 10-50;
19. Rigid-to-flex interface, aspect of flex laminate and coverlay in conformance with Table 10-51;

b. The visual inspection of qualitative aspects shall include the review items from the MRR.

c. The acceptance criteria for visual inspection for qualitative aspects shall cover all PCBs in the batch by providing a pass/fail evaluation.

NOTE Inspection and evaluation of requirements is performed on all PCBs in the batch, whereas the reporting provides a summary.

B.2.1.4. Lab report for visual inspection of PCBs for dimensional verification

a. The sampling plan for performing visual inspection of PCBs for dimensional aspects shall be as specified in Table 8-1.

b. The lab report for visual inspection for dimensional verification shall include the following:

1. the PCB thickness is a representative measurement;
2. the PCB length and width are representative measurements;
3. specific dimensional features from the PCB definition dossier are representative measurements;
4. the warp and twist are the maximum measurements recorded on the worst-case PCB;
5. diameter of plated and non-plated holes for all diameters is a pass/fail evaluation, except for ≤ 0,6mm holes with SnPb in conformance with 10.6.3f;
6. external annular ring for all plated-hole types is a pass/fail evaluation;
7. external conductor width and spacing is a pass/fail evaluation for minimum width and spacing;
8. comparison of lay-out to the drawing for the presence of plated and non-plated holes and milling is a pass/fail evaluation.

NOTE 1 Comparison of lay-out to the drawing is performed as in-process inspection in conformance with 6.3f.7.

NOTE 2 Pass/fail evaluations provide an assessment of dimensions with respect to their tolerances specified in the PCB definition dossier.

NOTE 3 In case an external conductor is indicated as critical in the PCB definition dossier it can be inspected on all PCBs.

NOTE 4 Specific dimensional features can include cut-out or radius of PCB edge.

B.2.1.5. Lab report for microsection of coupons for qualitative aspects

a. The lab report for microsection for qualitative aspects shall include the following:

1. Blind and buried via filling in conformance with Table 10-17;Cap lift and planarity of blind via in conformance with Table 10-18 and Table 10-19;
2. Burrs and nodules in conformance with Table 10-20;
3. Voids or inclusions in copper plating in conformance with Table 10-21;
4. Wedge voids in conformance with Table 10-22;
5. Resin voids in conformance with Table 10-23;
6. Delamination, blistering, crazing, measling in conformance with Table 10-24;
7. Pad lift in conformance with Table 10-25;
8. Dielectric cracks in conformance with Table 10-26;
9. Cracks and separation in copper in conformance with Table 10-27;
10. ICD in conformance with Table 10-28;
11. Smear in conformance with Table 10-29;
12. HWPA and resin recession in conformance with Table 10-30;
13. Nail heading in conformance with Table 10-31;
14. CIC in conformance with Table 10-32;
15. Inhomogeneity in dielectric in conformance with Table 10-33;
16. Contamination or inclusion in conformance with Table 10-34;
17. Delamination between coverlay and prepreg in conformance with Table 10-35;
18. Adhesive voids in coverlay and bond-ply in conformance with Table 10-36;

19. Misalignment of prepreg in rigid-flex-interface in conformance with Table 10-37;

b. The lab report for microsection for qualitative aspects shall include the review items from the MRR.

c. The acceptance criteria for microsection for qualitative aspects shall cover all microsections of coupons in the batch by providing a pass/fail evaluation.

NOTE Inspection and evaluation of requirements is performed on all microsections of coupons in the batch, whereas the reporting provides a summary.

d. The lab report for microsection for qualitative aspects shall include the following representative pictures of microsections covering the batch, except in case this is specifically waived by the customer in the PCB definition dossier:

1. Overview of PTH after SB in dark field showing laminate integrity, build-up;
2. 500x magnification after SB in bright field showing interconnect and absence of ICD;
3. 500x magnification as received in bright field showing SnPb on corner;
4. Overview of rigid-to-flex interface after SB in dark field showing laminate integrity and absence of delamination.

B.2.1.6. Lab report for microsection of coupons for dimensional verification

a. The microsection of coupons for dimensional verification shall be performed for all panels.

b. The summary in the lab report shall be for a representative measurement covering all panels.

c. The lab report for visual inspection for dimensional verification shall include the following:

1. Annular ring internal and external in conformance with Table 10-1 and Table 10-2;
2. Copper foil thickness in conformance with Table 10-3;
3. Copper plating thickness in conformance with Table 10-4;

Etchback in conformance with

4. Table 10-5;
5. Wicking in conformance with Table 10-6;
6. Wrap copper in conformance with Table 10-7;
7. Dielectric thickness in conformance with Table 10-8 and Table 10-9;

8. Microvias dimensions and plating voids in conformance with Table 10-10 and Table 10-11;
9. SnPb thickness in conformance with Table 10-12;
10. Electrolytic Ni and Au dimensions in conformance with Table 10-13;
11. Undercut and overhang in conformance with Table 10-14 and Table 10-15;
12. Dimensions of rigid-flex-interface in conformance with Table 10-16.

B.2.1.7. Additional tests

a. The lab report for additional tests shall include the following:

1. Solderability in conformance with 9.4.11 in case this is applicable as specified in Table 10-12;
2. High resistance electrical test in conformance with 9.3.7.2 including serial numbers of accepted PCBs;
3. IST in conformance with 9.5.5.

B.2.2 Special remarks

The example test reports in Table B-1 to Table B-7 can be used.

Table B-1: Example of a declaration of conformance

Declaration of Conformance:	
☐ In conformance with ECSS-Q-ST-70-60	
☐ In conformance with PCB definition dossier	
Reference to waiver request, if applicable:	
MRR reference:	
Report reference number:	
Issue date of report:	
Purchase order:	
PCB Manufacturer & location:	
Customer Part Number (PCB definition dossier)	
PCB definition dossier and issue nr	
Batch code from PCB manufacturer	
Date code of PCB manufacture (YYWW)	
Serial number (S/N):	
Quantity ordered	
Quantity delivered	
Signature	

Table B-2: Example of a lab report for visual inspection of PCBs for qualitative aspects

Lab report for visual inspection of PCBs for qualitative aspects	Sampling	Requirement references	Value	Pass	Fail
Arbitrary defects of conductors, and pads (mouse bites, dents, nicks, pinhole, unintentional pattern)	100%	Table 10-38 + Table 10-39			
Lifting of conductor pattern	100%	Table 10-40			
Copper or nickel visible on top surface	100%	Table 10-40			
Corrosion of copper	100%	Table 10-40			
Blistering or air bubbles	100%	Table 10-41			
Delamination	100%	Table 10-41			
Crazing and measling	100%	Table 10-41			
Surface contamination or inclusion of foreign matter	100%	Table 10-42			
Non-homogeneous colour (oxidation of innerlayer copper, white spots)	100%	Table 10-42			
Scratches	100%	Table 10-43			
Weave exposure	100%	Table 10-44			
Haloing	100%	Table 10-45			
SnPb surface quality	100%	Table 10-46			
Marking	100%	Table 10-47			
Coverlay registration and annular ring of terminations on flexible PCB	100%	Table 10-2			
Rigid-to-flex interface, alignment of prepreg	100%	Table 10-48			
Rigid-to-flex interface, fibre protrusion	100%	Table 10-49			
Rigid-to-flex interface, haloing	100%	Table 10-50			
Rigid-to-flex interface, aspect of flex laminate and coverlay	100%	Table 10-51			
Review items from MRR	100%	B.2.1.3b			

Table B-3: Example of a lab report for visual inspection of PCBs for dimensional verification

Lab report for visual inspection of PCBs for dimensional verification	Sampling 1 PCB/batch	Requirement references	Value	Pass	Fail
PCB thickness, ☐ over laminate, ☐ over surface finish	s/n:	9.3.3.1b			
PCB length	s/n:	9.3.3.1c			
PCB width	s/n:	9.3.3.1c9.3.3.1c			
specific dimensional features from the PCB definition dossier (e.g. cut-out, radius)		B.2.1.4b3			
Warp and twist (maximum measurements recorded on the worst-case PCB)	s/n:	9.3.3.2-9.3.3.3			
Diameter of plated and non-plated holes for all diameters >0.6mm	s/n:	9.3.3.1d			
Diameter of plated holes ≤0.6mm if specified in PCB definition dossier	100%	10.6.3f			
External annular ring for all plated-hole types	s/n:	10.6.1b			
External conductor width and spacing on minimum dimensions	s/n:	9.3.3.1g, 9.3.3.1h, 9.3.3.1i, 9.3.3.1j			
External conductor width and spacing fine pitch on minimum dimensions	100%	9.3.3.1g, 9.3.3.1h, 9.3.3.1i, 9.3.3.1j			
Comparison of lay-out to the drawing (presence of plated and non-plated holes and milling)	s/n:	6.3f.7			

Table B-4: Example of a Lab report for microsection of coupons for qualitative aspects

Lab report for microsection of coupons for qualitative aspects	**Inspection**	**Requirement references**	**Pass**	**Fail**
			as per flow from Figure 8-1	
Blind and buried via filling	each panel	Table 10-17		
Cap lift and planarity of blind via	each panel	Table 10-18 + Table 10-19		
Burrs and nodules	each panel	Table 10-20		
Voids in copper plating	each panel	Table 10-21		
Wedge voids	each panel	Table 10-22		
Resin voids	each panel	Table 10-23		
Delamination, blistering, crazing, measling	each panel	Table 10-24		
Pad lift	each panel	Table 10-25		
Dielectric cracks	each panel	Table 10-26		
Cracks and separation in copper	each panel	Table 10-27		
ICD	each panel	Table 10-28 + Table 10-10 ref E		
Smear	each panel	Table 10-29		
HWPA and resin recession	each panel	Table 10-30		
Nail heading	each panel	Table 10-31		
CIC	each panel	Table 10-32		
Inhomogeneity in dielectric	each panel	Table 10-33		
Contamination or inclusion	each panel	Table 10-34		
Delamination between coverlay and prepreg	each panel	Table 10-35		
Adhesive voids in coverlay and bond-ply	each panel	Table 10-36		
Misalignment of prepreg in rigid-flex-interface	each panel	Table 10-37		
Review items from MRR	each panel	B.2.1.5b		
Comments:				
Pictures of microsections in conformance with B.2.5.d:				

Table B-5: Example of a lab report for microsection of coupons for dimensional verification

Lab report for microsection of coupons for dimensional verification	Requirement references	pass	fail		Requirement references	Measured value
	covers 100%			measure 1 per batch		
Annular ring internal	Table 10-1			s/n:	50 µm	
Annular ring internal reduced	Table 10-1			s/n:	ref E, 25 µm	
Annular ring microvia capture pad	Table 10-1			s/n:	ref D, 10 µm	
Annular ring external blind via	Table 10-2			s/n:	ref E, 100 µm	
Annular ring external microvia	Table 10-2			s/n:	ref F, 10 µm	
Copper foil thickness	Table 10-3			s/n:		build-up report
Copper plating thickness, PTH and via	Table 10-4			s/n:	ref A, B, C	
Copper plating thickness, blind and buried via	Table 10-4			s/n:	ref D	
Etchback	Table 10-5			s/n:	ref A	
Wicking	Table 10-6			s/n:		
Wrap copper	Table 10-7			s/n:		
Dielectric thickness	Table 10-8 + Table 10-9			s/n:		build-up report
Dielectric thickness - number of prepreg	Table 10-8 + Table 10-9			s/n:	ref B	
Microvias dimple and bump	Table 10-10			s/n:	ref A, B	
Microvias aspect ratio	Table 10-10			s/n:	ref C	
Microvias diameter to capture pad	Table 10-10			s/n:	ref D	
Microvias plating voids	Table 10-11			s/n:		

Lab report for microsection of coupons for dimensional verification	**Requirement references**	**pass**	**fail**		**Requirement references**	**Measured value**
	covers 100%			**measure 1 per batch**		
SnPb thickness PTH hole wall	Table 10-12			s/n:	ref C	
SnPb thickness PTH corner	Table 10-12			s/n:	ref D	
SnPb thickness PTH pads	Table 10-12			s/n:	ref E	
Electrolytic Ni	Table 10-13			s/n:	ref A	
Electrolytic Au	Table 10-13			s/n:	ref B, C	
Undercut	Table 10-14			s/n:		
Overhang	Table 10-15			s/n:	ref B	
Dimensions of rigid-flex-interface	Table 10-16			s/n:	ref A, B	

Table B-6: Example of a build-up report

Layer	Layer stacking	Thickness requirements			Measured value (µm) on s/n: ……..	Pass / Fail
		Nominal (µm)	Tolerances (µm)			
			min	max		
1	copper					
	dielectric					
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						
16						
17						
18						
19						
20						
21						
22						

Table B-7: Example of a lab report for additional tests

Lab report for additional tests		**Pass**	**Fail**	
Solderability	9.4.13			
High resistance electrical test	9.3.7.2			list of s/n:
IST	9.5.5			report reference:
Comments:				

Annex C (normative)
Qualification test report – DRD

C.1 DRD identification

C.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-60 requirement 5.9c.

C.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the qualification test report.

C.2 Expected response

C.2.1 Scope and content

a. The qualification test report shall include:
   1. Description and history of the samples.
   2. Reference to the approved qualification test plan.
   3. All results from the qualification tests in conformance with requirements from clause 7.2.
   4. Photographic documentation of results obtained from microsectioning.

b. The photographic documentation of microsections from the qualification test report shall use magnification level, lighting, micro-etchant and surface preparation in conformance with clauses 9.5.2.5 and 10.2.

C.2.2 Special remarks

a. The qualification test report shall be maintained under configuration control.

Annex D (normative) Process Identification Document (PID) for PCB manufacturing – DRD

D.1 DRD identification

D.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-60 requirement 5.8c.1.

D.1.2 Purpose and objective

The purpose of the PID is to specify the manufacturing processes, materials and equipment of the qualified PCB technology. It also specifies the technological parameters of the qualified design.

The PID consist of a general part and specific parts. A general part of the PID describes the company, whereas specific parts of the PID describe each qualified technology.

D.2 Expected response

D.2.1 Scope and content

D.2.1.1. General part of the PID

a. The general part of the PID shall include the following information:

1. Description of the company: history in business, products, staff, customers and the qualified site, in case of multiple sites;
2. Technology road map;
3. Organization chart with names and functions of key personnel;
4. Quality certifications;
5. Description of the process flow for order treatment, including the following:
   (a) Design review in conformance with the clause 5.2 of ECSS-Q-ST-70-12;

(b) MRR in conformance with the clause 5.2 of ECSS-Q-ST-70-12;

(c) Outgoing inspection and CoC in conformance with the clause 8;

6. List of main equipment for the production of PCBs, including type and brand name;

7. List of test and control equipment with their capabilities;

8. List of work instructions for manufacture and control of PCBs, with document numbers and issue references.

NOTE 1 For D.2.1.1a7, examples of test capabilities are metallographic examination, chemical analysis, failure analysis, mechanical and electrical test including functional testing of PCBs.

NOTE 2 For D.2.1.1a8, the work instructions include the process description.

D.2.1.2. Specific parts of the PID

a. Specific parts of the PID shall include:

1. Manufacturing and quality control flow charts with reference to applicable work instructions;

2. List of base materials and chemicals with brand name, type, and supplier;

3. Production flow-chart, including in-process inspections and reference to work instructions in conformance with D.2.1.1a8;

4. Description of qualified domain in conformance with the items specified in requirement G.2.1b.

5. Description of any review items that have been specifically qualified, as specified in clause <7>a of Annex A of ECSS-Q-ST-70-12;

6. Subcontracted processes.

D.2.2 Special remarks

a. If several technologies are qualified, the general part of the PID may be a separate document to avoid duplication in the PIDs for each technology.

b. All PIDs shall have an identification of the issue, revision number and date, and a page showing the modifications introduced at each revision.

c. The modifications introduced since the previous revision of a PID shall be identified with specific marks or font.

Annex E (normative)
Process change notice (PCN) – DRD

E.1 DRD identification

E.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-60, requirement 5.12f and F.2.1a.1.

E.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the process change notice (PCN).

E.2 Expected response

E.2.1 Scope and content

a. Process changes shall include process parameters, chemistry, material, equipment, process flow and inspections.

b. The PCN shall contain the following:

1. Categorisation of process change as “major” or “minor”;
2. Justification for categorisation;
3. Description of old and new process;
4. Justification for change;
5. Reference to work instruction in PID;
6. In case of minor process change, results of verification tests and inspections;
7. Request for major process change including qualification test plan;
8. Request for approval of implementation of the major process change including qualification test report;
9. Optional approval from procurement authority for major process change in conformance with requirement 5.12h.

E.2.2 Special remarks

None.

Annex F (normative)
QA report – DRD

F.1 DRD identification

F.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-60, requirement 5.13a.

F.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the QA report.

F.2 Expected response

F.2.1 Scope and content

a. The QA report shall contain the following:

1. Status of process changes, including associated process change notices in conformance with the DRD in Annex E;
2. Overview of internal nonconformances, scrap, cause, yield and corrective action;
3. Overview of external nonconformances, cause and corrective action;
4. Overview of KPIs including OTD;
5. Overview of planned and implemented investments;
6. Changes in personnel and organigram;
7. Overview of major visits by procurement authority, qualification authority or by certification bodies.

F.2.2 Special remarks

a. Nonconformances and KPIs should be expressed per month in absolute numbers and relative to the production in accordance with applicable PIDs for each technology.

Annex G (normative)
PCB approval sheet – DRD

G.1 DRD identification

G.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-60 requirement 6.13h for the PCB approval sheet part 1 and is called from ECSS-Q-ST-70-60 requirement 6.13j for the PCB approval sheet part 2.

G.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the PCB approval sheet part 1 and part 2.

G.2 Expected response

G.2.1 Scope and content

a. The PCB approval sheet part 1 shall contain the following information:

1. Identification of the PCB reference;
2. PCB manufacturer and country;
3. Backup PCB manufacturer and country;
4. PCB technology as specified in requirement 5.10b;
5. PCB procurement specification in conformance with 6.2.2a;
6. Listing of the qualification status of PCB manufacturer on public web portal;
7. Identification of the PID reference;
8. Associated delta qualification and RFA.

NOTE 1 The customer can be the prime contractor, space agency or the next industry in the contractual chain.

NOTE 2 The public web portal can be www.escies.org.

b. The PCB approval sheet part 2 shall contain the following information

1. PCB technology as specified in requirement 5.10b;

2. Number of rigid layers;
3. Number of flex layers;
4. Number of plating sequences;
5. Number of lamination sequences;
6. Length and width of PCB and manufacturing panel;
7. Thickness of PCB;
8. Thickness of outer layer copper foil and copper plating;
9. Minimum and maximum copper thickness of internal layers;
10. Identification of material reference for:
    (a) Epoxy;
    (b) Polyimide;
    (c) Flexible layers;
    (d) RF materials;
    (e) Mixed materials;
    (f) Metal core;
11. Identification of the used surface finishes, including but not limited to the following:
    (a) Hot oil reflowed tin-lead;
    (b) Electroplated hard gold and soft gold with possible nickel underplating;
    (c) Soldermask;
    (d) Tin diffusion layer;
    (e) ENIG, ENEPIG, ENIPIG;
12. Minimum external and internal track width;
13. Minimum external and internal insulation distance;
14. Minimum insulation distance in Z-direction;
15. Minimum finished holes sizes and maximum aspect ratio for:
    (a) PTH;
    (b) Blind via;
    (c) Buried via;
    (d) Microvia;
16. List of review items from MRR in conformance with clause A.2<7> of ECSS-Q-ST-70-12.

c. The PCB approval sheet part 2 shall provide confirmation for each aspect in conformance with requirements from G.2.1b1 to G.2.1b16 that it is within the qualified domain from the PID of the PCB manufacturer.

d. The PCB approval sheets part 1 and part 2 shall contain the approval signatures from the procurement authority and customer

NOTE The customer can be the prime contractor, space agency or the next industry in the contractual chain.

G.2.2 Special remarks

Examples of a PCB approval sheet part 1 and part 2 are given in the Table G-1 and Table G-2.

Table G-1: Example of a PCB approval sheet part 1

PCB Approval sheet part 1	
PCB reference	
Manufacturer / country	
Backup manufacturer	
PCB technology description	Polyimide sequential rigid Polyimide sequential rigid/flex Epoxy sequential rigid Epoxy multilayer rigid/flex HDI with microvias RF PCBs Flex and sculptured flex
Generic specification ECSS-Q-ST-70-60?	(Y/N)
Approval status of PCB manufacturer	
PCB manufacturer listed on ESCIES.org?	(Y/N)
PID reference	
Delta qualification required?	(Y/N)
If yes, reference of the RFA	
Approval signature	
Procurement authority approval	Date
Customer approval	Date

Table G-2: Example of a PCB approval sheet part 2

PCB approval sheet part 2			
PCB summary drawing sheet			
PCB reference(s)			
		Actual value worst case as designed	PID qualified domain
Number layers/sequence	Rigid		
	Flex		
	Plating sequences		
	Lamination sequences		
Thickness/size	PCB Size (mm)		
	PCB Thickness (mm)		
	External Cu thickness foil and plating (µm)		
	Internal min Cu thickness (µm)		
	Internal max Cu thickness (µm)		
Material (Commercial reference Manufacturer name)	Epoxy		
	Polyimide		
	Flexible		
	RF materials		
	Mixed materials		
	Metal core		
	other		
Surface finish	Sn/Pb hot oil reflow		
	Ni/Au electroplated (hard/soft)		
	Soldermask		
	Tin diffusion layer		
	ENIG, ENIPIG, ENEPIG		
	other		

Minimum design features (μm)	External track width		
	External insulation distance		
	Internal track width		
	Internal insulation distance		
	Insulation distance in z-direction		
Minimum finished hole size (μm)	PTH		
	Blind		
	Buried		
	Microvia		
Aspect ratio	PTH		
	Blind		
	Buried		
	Microvia		
Review items from MRR as per clause A.2<7> of ECSS-Q-ST-70-12	(Y/N)		
	If yes, provide list of review items from MRR and verify against PID when applicable		

Approval signature

Procurement authority approval Date

Customer approval Date

Annex H (informative)
Example of plated-through hole microsection

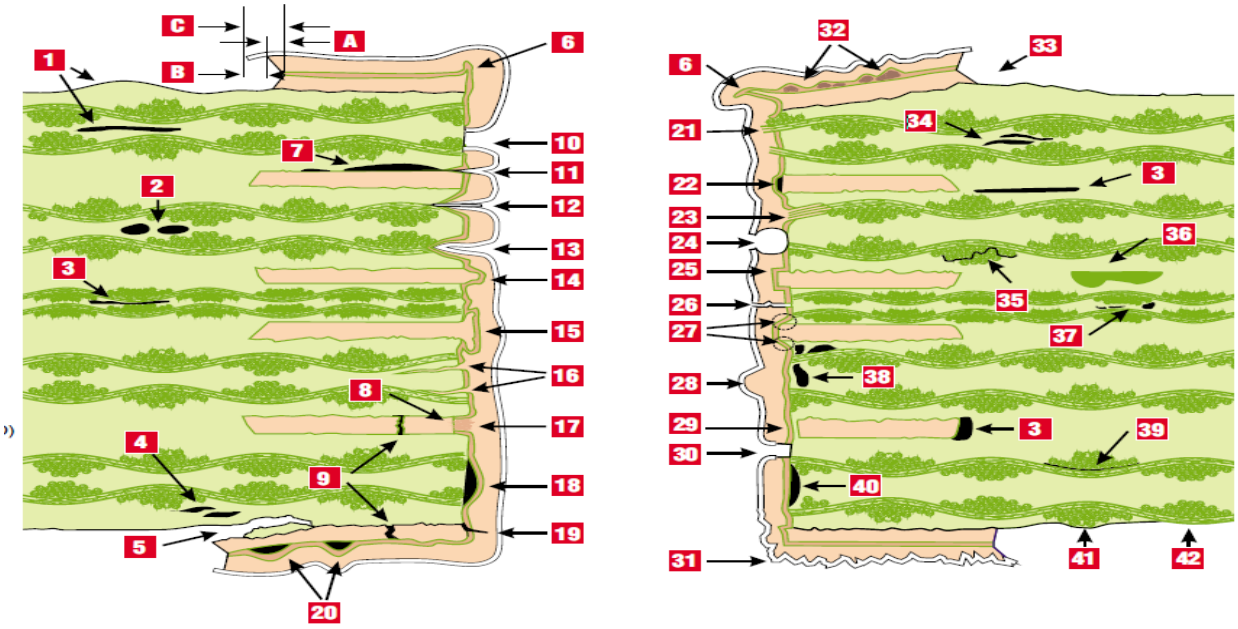


Figure H-1: Typical phenomena in cross section of PTH. Not all phenomena are specified in ECSS-Q-ST-70-60 in the same way.

Annex I (informative) Cleanliness requirements for laminate and prepreg

I.1 Introduction

The text from this annex is cited from Appendix A from IPC-4101E and was originally drafted by European space industry. The text is provided for information. The full standard and any future revisions can be obtained from IPC.

I.2 Citation of Appendix A from IPC-4101E

APPENDIX A from IPC-4101E supplemental inspection requirements if required in purchase order or master drawing.

A.1 - SCOPE

This Appendix A defines supplemental requirements to this standard [IPC-4101E] with the purpose to define a high quality for base materials to be used for high reliability PWBs for critical applications. PWBs designed with small spacing or used in high voltage applications can be subject to failure of insulation resistance due to breakdown or inclusion of foreign material.

Printed boards that meet the requirements of IPC-6012DS ‘‘Space and Military Avionics Applications Addendum, Section 0.1.1 Purpose,’’ are not allowed to have foreign inclusions that reduce dielectric spacing to below the minimum requirement. The requirements on base materials in this appendix aim to prevent and to detect such non-conformance earlier in the supply chain.

If the user of material wishes to acquire laminate, prepreg or both that meet the requirements of this Appendix A, then this Appendix A shall be specifically called out in the purchase order or the master drawing. Further, this Appendix A shall not be assumed to be in force if it is not specifically called out in the purchase order or the master drawing.

A.2 - PREPREG

A.2.1 Acceptance Criteria for Prepreg Requirements 3.8.3.2.1 and 3.8.3.2.2 shall apply for inclusions and imperfections in prepreg.

A.2.2 Test Method for Prepreg Prepreg shall be tested in accordance with Table 3-2 for visual properties, with the following modification:

a. – Conformance testing of visual properties shall be performed on 100% of the units in a lot using IPC-TM-650, Method 2.1.5, or an equivalent

method AABUS. Modify Method 2.1.5 by changing the particulate inspection magnification to 50X.

b. A.2.3 Rejection Criteria for Prepreg Section 4.4.3 shall be discarded for rejected lots. The following modification shall apply:

c. – Material with non-conformances shall be discarded from the batch. The remainder of the batch shall be compliant with this Appendix A.

A.3 - LAMINATE

A.3.1 Acceptance Criteria for Laminate The requirements of 3.8.3.1.6 shall apply for imperfections on laminate, with the following modification:

– Requirement 'f' shall be deleted and the following shall apply: Opaque foreign matter shall not exceed 0.50 mm [0.019 in]. Opaque foreign inclusions <0.13 mm [0.005 in] shall not be counted. Opaque foreign inclusions sized between 0.13 mm [0.005 in] and ≤0.50 mm [0.019 in] shall average no more than two spots per 300 mm x 300 mm [11.81 in x 11.81 in] area inspected.

A.3.2 Test Method for Laminate Laminate shall be tested in accordance with Table 3-1 for surface and sub-surface imperfections, with the following modification:

– The conformance testing of surface and sub-surface imperfections shall be performed on ≥2% of the total area of the lot.

A.3.3 Rejection Criteria for Laminate Section 4.4.3 shall be discarded for rejected lots. The following modification shall apply:

– All base material in the lot shall be non-compliant to this Appendix A if non-conformances are observed in the lot.

A.3.4 In-Process Requirement for Laminate For the manufacture of copper clad laminate, the base material supplier shall use prepreg that is inspected and evaluated in accordance with A.2 or AABUS.

A.3.5 Hi-Pot Test for Laminate Hi-Pot testing as per IPC-TM-650, Method 2.5.7.2, can be performed AABUS on 100% of the copper clad laminate with a nominal thickness of ≤0.119 mm [0.0047 in]. The preparation of edges of the laminate, the bake out, the electrical test parameters and the acceptance criteria are AABUS.

A.4 - APPLICABILITY

Section 4.2 shall apply for the responsibility of conformance testing performed by the base material manufacturer, with the following modification:

– The procurement authority has the right to perform inspections set forth in this Appendix A to verify acceptability of the lot, in which case the requirements of this Appendix A shall apply.

A.5 - CERTIFICATE OF CONFORMANCE

Section 4.4.5 shall apply for the certificate of conformance, with the following modification:

– The certificate of conformance shall include a statement of compliance to this Appendix A.

A.6 - QUALITY CONFORMANCE INSPECTION AND FREQUENCY

Sections 4.4 and 4.4.1 shall apply for quality conformance inspection and frequency with the following modification:

– The manufacturer's quality system shall not take precedence over the requirements in Appendix A.

Table A-1 Summary Table of Modifications in Appendix A

Tests	Requirement paragraph IPC-4101E	Test Method	Qualification Testing	Conformance Testing	Conformance Testing Frequency	Inspected specimens
Visual properties for prepreg	3.8.3.2	2.1.5 or AABUS	✓	✓	Lot	100% of the lot as per A.2.2
Surface and Sub-Surface Imperfections for laminate	3.8.3.1.6 and A.3	2.1.5 or AABUS	✓	✓	Lot	≥2% of the lot as per A.3.2
Hi-Pot electrical test on laminate	A.3.5	2.5.7.2 or AABUS	AABUS	AABUS	-	100% or AABUS

Bibliography

ECSS-S-ST-00	ECSS system – Description, implementation and general requirements
ECSS-Q-ST-70-07	Space product assurance — Verification and approval of automatic machine wave soldering
ECSS-Q-ST-70-28	Space product assurance — Repair and modification of printed circuit board assemblies for space use
ECSS-Q-ST-70-38	Space product assurance —High reliability soldering for surface mount and mixed technology printed circuit boards
IEC 60068-2-3 (1969-01)	Environmental testing. Part 2: Tests. Test Ca: Damp heat, steady state
IEC 60068-2-14-am 1 (1986-01)	Environmental testing. Part 2: Tests. Test N: Change of temperature
IEC 60068-2-20-am 2 (1987-01)	Environmental testing. Part 2: Tests. Test T: Soldering
IEC 60249-1-am 4 (1993-05)	Base materials for printed circuits. Part 1: Test methods
IEC 60326-5-am 1 (1989-10)	Printed boards. Part 5: Specification for single and double sided printed boards with plated-through holes
IEC 60326-8 (1981-01)	Printed boards. Part 8: Specification for single and double sided flexible printed boards with through connections
IEC 60326-11 (1991-03)	Printed boards. Part 11: Specification for flex-rigid multilayer printed boards with through connections
IEC 62326-4 (1996-12)	Printed boards. Part 4: Rigid multilayer printed boards with interlayer connections - Sectional specification
MIL-P-50884C (1984)	Printed wiring, flexible and rigid-flex
IPC-J-STD-003C (2013)	Solderability test for printed boards
IPC-2221B (2012)	Generic standard on printed board design
IPC-5703 (2013)	Cleanliness guidelines for printed board fabricators
IPC-5704 (2009)	Cleanliness requirements for unpopulated printed boards
IPC-6011 (1996)	Generic performance specification for printed boards
IPC-6013CS (to be issued)	Space and military avionics applications addendum to IPC-6013C
IPC-9252B (2016)	Requirements for electrical testing of unpopulated printed boards
IPC-9691B (2016)	User Guide for the IPC-TM-650, Method 2.6.25, Conductive Anodic Filament (CAF) Resistance and Other Internal Electrochemical Migration Testing