ECSS-Q-ST-70-38C Rev.1 Corrigendum 1
12 September 2018

Space product assurance

High-reliability soldering for surface-mount and mixed technology

ECSS Secretariat
ESA-ESTEC
Requirements & Standards Division
Noordwijk, The Netherlands

Foreword

This Standard is one of the series of ECSS Standards intended to be applied together for the management, engineering and product assurance in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards. Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

This Standard has been prepared by the ECSS Executive Secretariat, reviewed by the Document and Discipline Focal point, and approved by the ECSS Technical Authority.

Disclaimer

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Change log

ECSS-Q-70-38A 26 October 2007	First issue
ECSS-Q-70-38A Rev.1 5 December 2007	Second issue Requirement 14.9.2 d. added
ECSS-Q-70-38B	Never issued
ECSS-Q-ST-70-38C 31 July 2008	Third issue Editorial changes.
ECSS-Q-ST-70-38C Rev.1 15 September 2017	Third issue, Revision 1 Major changes of this version with regard to the previous version are: • ECSS-Q-ST-70-38 is dealing with qualification of Surface Mount Component Assembly for electronics equipment. For this technology, many new types of components have been introduced in the design of electronic boards and thus needed to follow a qualification process to warranty reliable assembled boards. • As complexity of electronics component is widely increasing so is the packaging of the integrated circuit and the way to mount it on a board. Notion of sensitive device has been identified for those which are difficult to assemble and inspect by visual means. • Main changes in the document, have been introduced in clause 14 which describes precisely the verification programme for qualification including the pass/fail criterion per type of component. The goal of all discussions within the Working Group was to have a good trade-off between reliability and cost for European Equipment manufacturers to stay competitive against the « rest of the World ». • Clause 16 deleted and moved into clause 14.7.2 and Annex I; • Annex A deleted; Annex B deleted; Annex C deleted • Normative Annex F "Process Identification Document (PID) - DRD" added • Normative Annex G "Verification programme report – DRD" added • Normative Annex H "SMT summary table – DRD" added • Informative Annex I "Visual and X-ray workmanship standards" added (partially created from former clause 16)

Detailed changes:

Added requirements

- 5.1.2b-d; 6.1b; 6.7.1e-f; 6.8.1b; 7.9.1j-o; 7.10i-m; 8.1.4b-d; 8.5d-f; 9.7.1d-f; 9.7.4e-f; 9.7.6g (created from deleted requirement 9.7.6h); 9.7.6h; 11.5.1g-o; 11.5.3b; 11.5.4b; Table 11-4; Figure 11-4; 11.5.6b; 11.5.8c; 11.5.9a-b; Table 11-9; Figure 11-11; 11.5.10a-c; Table 11-10; Figure 11-12; 11.5.11a-b; Table 11-11; Figure 11-13; 11.5.12a-d; Table 11-12; Figure 11-14; 11.5.13a-b; 13.1f-h; 13.4b; 13.5b-c; 14.1m-x; Table 14-1; 14.2.1a-b; 14.2.2a-f; 14.3c-s; 14.4.1a-l; Figure 14-2; 14.5b-j; 14.6e; 14.7.1a-c; 14.7.2a-o; Table 14-2; 14.9.3a-c; Figure 14-3; 14.9.4a-I; 14.9.5a-m; 14.10h-o; Table 14-3; 14.13a-I; Table 14-4; 14.14a-b; 14.15.1a-c; 14.15.2a-b; 14.15.3a-d; 14.15.4a; 14.15.5a-b; 14.15.6a-c; 15.8d; 15.9d; Annex F; Annex G; Annex H.

Modified requirement

- 5.1.2a; 5.1.4a; 5.3a, c and e; 6.1a; 6.2a; 6.3a; 6.4a; 6.5a; 6.6.1a; 6.6.2a; 6.6.3a; 6.6.4a; 6.6.5a; 6.6.6a; 6.6.7a; 6.6.7b NOTE; 6.6.9a; 6.7.1a and c; 6.7.2a; 6.7.3a; 6.7.4a; 6.7.6a; 6.7.7a; 6.8.2a; 6.8.5a; 6.8.7a-d; 6.8.8a; 7.1a; 7.2.1b; 7.2.2a; 7.2.4e; 7.3.1a; 7.3.2a; 7.4a; 7.5a; 7.6a; 7.7a; 7.8a-c; 7.9.1a, c and e; 7.9.3a-b; 7.10b, e NOTE, f and g; 8.1.1a; 8.1.2a; 8.1.3a; 8.2a; 8.3a; 8.4a; 8.5b and c; 9.1a; 9.2a; 9.3a; 9.4a; 9.5a; 9.6a; 9.7.1a NOTE added; 9.7.2a; 9.7.3a and b; 9.7.4d; 9.7.5b NOTE deleted; 9.7.6c, e and f; 9.7.7a; 9.7.9a, c-e; 10.a; 11.1a; 11.3a; 11.4a; 11.5.1b-e; 11.5.2b and c NOTE; Table 11-1 updated (including caption); 11.5.3a; Table 11-2 updated (including caption); 11.5.4a; Table 11-3 updated (including caption); Figure 11-3 updated; 11.5.5a (reference to Table and Figure changed and NOTE2 deleted); Table 11-5 updated (including caption and table number); Figure 11-5 (change of figure number); 11.5.6a; Table 11-6 updated (including caption and table number); Figure 11-6 (change of caption and figure number); 11.5.7a (reference to of Table and Figure changed); Table 11-7 updated (including caption and table number); Figure 11-7 (change of figure number); 11.5.8a and b; Table 11-8 updated (including caption and table number); Figure 11-9 (change of figure number);Figure 11-1 (change of figure number); 12.1a; 12.2a; 12.3a; 13.1a, d and e; 13.2a; 13.3a; 13.4a; 14.1a, b, f, g, k and l; 14.3a; Figure 14-1 updated including caption; 14.5a; 14.6a-c; 14.10c-d; 14.11a and d; 15.1a; 15.2a; 15.3a; 15.4a; 15.5a; 15.6b NOTE; 15.8a-c.

Deleted requirements

- 5.1.3a-b; 5.1.4b; 5.2a-e; 5.3d; 6.6.8a; 6.7.5a; 6.8.4a; 7.2.3a; Table 7-1; 7.2.4e; 7.8.1a-c; Table 7-2; 7.8.2a; 7.8.3a; 7.8.4a; 7.8.5a; 7.8.6a; 7.9.1b, d, g and h; 7.9.2a-c; 7.9.4a-e; 8.1.4a; 8.5a; 9.7.1b; 9.7.6b; 9.7.8a; 9.7.9b; 9.7.9f (and created as recommendation in 9.7.9g); 11.2a; Figure 11-8 (in Issue C Figure 11-7: Typical plastic ball grid array (PBGA); 11.6a-b; Figure 11-15; 11.7a; 11.8.a; 13.1b-c; 13.5a; 14.1c-e, h-j; 14.2a-k; 14.4a; 14.6d; 14.7a-e; 14.8a-b; 14.9.2a-e; 14.10a, f-g; Figure 14-4 (former Figure 14-2); 14.11b-c; 15.6a; 15.7c; 15.9a-c (correctly created as 15.9d).

Editorial modifications and corrections:

- Introduction updated; Normative references updated; Terms, definitions and abbreviated terms updated; Nomenclature added; terms replaced in document: "pad" by "footprint" and "part" "device"; Annex D marked as "informative" in title; Annex E.1 deleted; Bibliography updated.

Text of Clause headings modified:

- Clause 6.6.2; 6.6.9; 7.9; 7.9.3; 7.10; 8.5; 9.7.3; 9.7.9; 11; 11.5.4; 11.5.6; 14.3; 14.4; 14.5; 14.9; 14.10.

ECSS-Q-ST-70-38C Rev.1 Corrigendum 1 12 September 2018	Corrigendum 1 of Third issue, Revision 1 Approved by the Technical Authority on 12 September 2018. Correction of requirement 14.2.2c.1: Incorrect text: *"1. device size is between the length Lmax and the width Wmax of the verified component,"* Corrected text: *"1. the device size length is between Lmin and Lmax and the device size width is between Wmin and Wmax of the ones of the verified component,"*

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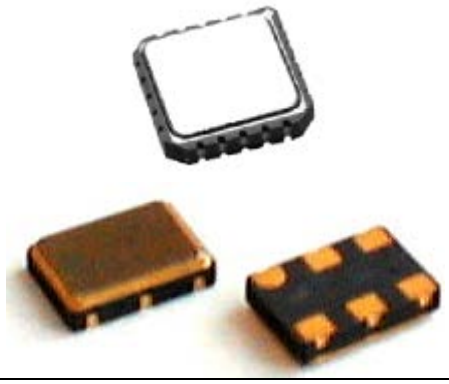
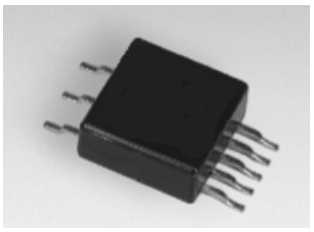
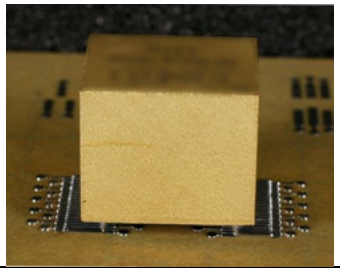
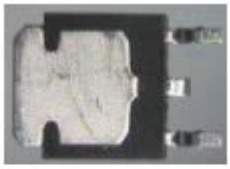
Introduction

This Standard prescribes requirements for electrical connections of leadless and leaded surface mounted devices (SMD) on spacecraft and associated equipment, utilising a range of substrate assemblies and employing solder as the interconnection media. The principal types of SMDs can be gathered in the following families:

Rectangular and square end-capped or end-metallized device with rectangular body, leadless chip (see 11.5.2) e.g. end capped chip resistors and end capped chip capacitors.	
Cylindrical and square end-capped devices with cylindrical body, leadless chip (see 11.5.4) e.g. MELF for cylindrical end capped or e.g. D-5A for square end capped	 
Bottom terminated chip device (see 11.5.3) This type of device has metallised terminations on the bottom side only. e.g. inductors and SMD0.5, SMD1, SMD2, SMD0.2, SMD0.22 e.g. Quad Flat Pack No lead (QFN)	  

Castellated chip carrier device (see 11.5.5) The main device of this type is leadless ceramic chip carrier (LCCC). e.g. LCC6	
Flat pack and gull-wing leaded device with round, rectangular , ribbon leads (see 11.5.6) e.g. small-outline transistor (SOT), small—outline package (SO), flat pack and quad flat pack (QFP) and SMD connectors with stress-relief. This family also comprises devices for through-hole mounting that have been reconfigured to surface mounting.	
Moulded magnetics (see 11.5.13) e.g. 1553 interface transformers or specific transformers	 
"J" leaded device (see 11.5.7) e.g. ceramic leaded chip carriers (CLCC) and plastic leaded chip carriers (PLCC).	

Area array devices (AAD) (see 11.5.8) The interconnections between solder footprints on the devices and solder footprints on the PCB consist entirely of solder. The devices have either solder balls (Ball Grid Array - BGA) or solder columns (Column Grid Array - CGA) applied to the solder footprints on the devices prior to mounting on a PCB (normally done by the device manufacturer). The solder balls on the BGAs can consist of either eutectic solder or high temperature solder (5 - 10 % Sn) whereas the solder columns on the CGAs always consist of high temperature solder. Although BGAs are usually presented as a device family, there exist a large number of BGA devices with wide-ranging properties. The vast majority of BGA devices are non hermetic.	
Devices with ribbon terminals without stress relief (flat lug leads) (see 11.5.9) This package has flat leads extending from the sides	
Device with Inward formed L-shaped leads (see 11.5.10) e.g. moulded tantalum chip capacitors.	
Stacked modules devices with leads protruding vertically from bottom (see 11.5.11)	
Leaded device with plane termination (see 11.5.12) e.g. Diode PAcKage (DPAK or TO252)	  DPAK

1 Scope

This Standard defines the technical requirements and quality assurance provisions for the manufacture and verification of high-reliability electronic circuits based on surface mounted device (SMD) and mixed technology.

The Standard defines acceptance and rejection criteria for high-reliability manufacture of surface-mount and mixed-technology circuit assemblies intended to withstand normal terrestrial conditions and the vibrational g-loads and environment imposed by space flight.

The proper tools, correct materials, design and workmanship are covered by this document. Workmanship standards are included to permit discrimination between proper and improper work.

The assembly of leaded devices to through-hole terminations and general soldering principles are covered in ECSS-Q-ST-70-08.

Requirements related to printed circuit boards are contained in ECSS-Q-ST-70-10, ECSS-Q-ST-70-11 and ECSS-Q-ST-70-12 . The mounting and supporting of devices, terminals and conductors prescribed herein applies to assemblies at PCB level designed to continuously operate over the mission within the temperature limits of -55 °C to +85 °C.

For temperatures outside this normal range, special design, verification and qualification testing is performed to ensure the necessary environmental survival capability.

Special thermal heat sinks are applied to devices having high thermal dissipation (e.g. junction temperatures of 110 °C, power transistors) in order to ensure that solder joints do not exceed 85 °C.

Verification of SMD assembly processes is made on test vehicles (surface mount verification samples). Temperature cycling ensures the operational lifetime for spacecraft. However, mechanical testing only indicates SMD reliability as it is unlikely that the test vehicle represents every flight configuration.

This Standard does not cover the qualification and acceptance of the EQM and FM equipment with surface-mount and mixed-technology.

The qualification and acceptance tests of equipment manufactured in accordance with this Standard are covered by ECSS-E-ST-10-03.

This standard may be tailored for the specific characteristics and constraints of a space project, in accordance with ECSS-S-ST-00.

2
Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references the latest edition of the publication referred to applies.

ECSS-S-ST-00-01	ECSS system — Glossary of terms
ECSS-M-ST-40	Space project management — Configuration and information management
ECSS-Q-ST-10-09	Space product assurance — Nonconformance control system
ECSS-Q-ST-20	Space product assurance — Quality assurance
ECSS-Q-ST-60	Space product assurance — Electrical, electronic and electromechanical (EEE) components
ECSS-Q-ST-60-05	Space product assurance — Generic requirements for hybrids
ECSS-Q-ST-60-13	Space product assurance - Commercial electrical, electronic and electromechanical (EEE) components
ECSS-Q-ST-70	Space product assurance — Materials, mechanical parts and processes
ECSS-Q-ST-70-01	Space product assurance — Cleanliness and contamination control
ECSS-Q-ST-70-02	Space product assurance — Thermal vacuum outgassing test for the screening of space materials
ECSS-Q-ST-70-08	Space product assurance — Manual soldering of high–reliability electrical connections
ECSS-Q-ST-70-10	Space product assurance — Qualification of printed circuit boards
ECSS-Q-ST-70-11	Space product assurance — Procurement of printed circuit boards
ECSS-Q-ST-70-12	Space product assurance — Design rules for printed circuit boards
ECSS-Q-ST-70-28	Space product assurance — Repair and modification of

	printed circuit board assemblies for space use.
ECSS-Q-ST-70-71	Space product assurance —Materials processes and their data selection
MIL-STD-883 Method 2009	Test Method Standard, Microcircuits
IPC-TM-650: 2.6.3.3 Issue 2004	Test methods manual. Surface Insulation Resistance, Fluxes

3
Terms, definitions and abbreviated terms

3.1 Terms from other standards

a. For the purpose of this Standard, the terms and definitions from ECSS-S-ST-00-01 apply.

b. For the purpose of this Standard, the terms and definitions from ECSS-Q-ST-60 apply, in particular for the following term(s):

1. commercial component

c. For the purpose of this Standard, the terms and definitions from ECSS-Q-ST-70-28 apply, in particular for the following term(s):

1. repair
2. rework

3.2 Terms specific to the present standard

3.2.1 approval authority

entity that reviews and accepts the verification programme, evaluating the test results and grants the final approval

3.2.2 bonding

application process of adhesive under a SMD package for mechanical or thermal purpose where adhesive joint is not visible

3.2.3 co-planarity

maximum distance between lowest and highest termination when device rests on flat surface

3.2.4 collective assembled devices

set of components that are soldered to PCB in one operation

3.2.5 critical zone

area in the solder joint in which the existence and magnitude of cracks is subject to acceptance or rejection

3.2.6 device

package, component or part

3.2.7 dynamic wave soldering machine

system that achieves wave soldering and which consists of stations for fluxing, preheating, and soldering by means of a conveyer

3.2.8 electrical clearance

spacing between non-common electrical conductors on external layers of a printed circuit board assembly

NOTE The distance between conductors depends on the design voltage and DC or AC peaks. Any violation of minimum electrical clearance as a result of a nonconformance is a defect condition.

3.2.9 reprocessing

preparatory operation done on a device prior to assembly

NOTE Retinning, degolding, lead forming are examples of reprocessing.

3.2.10 scavenging (leaching)

basis metal or metallization partly or wholly dissolved in melted solder during a soldering operation

3.2.11 selective plating

tin-lead plated solder footprints connected to gold plated copper tracks

NOTE It is usually related to RF circuits.

3.2.12 sensitive devices

device prone to have cracks in solder joint exceeding 75 % of acceptance criteria or showing nonconformance outside the component manufacturer limit

NOTE 1 ESA list of sensitive devices is published on ESCIES for information, see www.escies.org.

NOTE 2 Each company maintains its own list of sensitive devices in the PID.

3.2.13 solder balling (solder balls)

numerous spheres of solder having not melted in with the joint form and being scattered around the joint area normally attached by flux residues

NOTE Can be caused by incorrect preheating or poor quality solder.

3.2.14 stacking

application process of adhesive at extremities of a SMD package for mechanical purpose where adhesive joint is partially visible

3.2.15 solder stand-off

thickness of solder between the underside of the device termination and the surface of the PCB footprint

3.2.16 test vehicle

substrate assembled with Surface Mounted Devices subjected to a verification programme

3.2.17 tombstoning

chip devices lifting off one of their two terminal footprints causing the chip to stand up like a tombstone

NOTE Normally caused by:

- bad design where one footprint reaches solder reflow temperature before the other;
- different quantities of solder paste on each footprint;
- different solderability of one footprint or one termination with respect to the other.

3.2.18 underfill

encapsulant material deposited between a device and substrate

3.3 Abbreviated terms

For the purpose of this Standard, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
AAD	area array device
BGA	ball grid array
CBGA	ceramic ball grid array
CCGA	ceramic column grid array
CGA	column grid array
CLCC	ceramic leaded chip carrier
CTE	coefficient of thermal expansion
DPAK	diode package
DRD	document requirement definition
FM	flight model or flight hardware
FP	flat pack package
JEDEC	Joint Electron Device Engineering Council
LCCC	leadless ceramic chip carrier
MELF	metal electrode face bonded NOTE: Also known as minimelf or micromelf
MIP	mandatory inspection point
PCB	printed circuit board
PLCC	plastic leaded chip carrier

Abbreviation	Meaning
PID	process identification document
QFN	quad flat pack no leads
QFP	quad flat pack
r.m.s.	root-mean-square
SIR	surface insulation resistance
SMD	surface mounted device
SMT	surface-mount technology
SO	small outline
SOD	small outline device
SOT	small outline transistor
SOP	small outline package
TO	transistor outline
TSOP	thin small outline package

3.4 Nomenclature

3.4.1 Formal verbs

The following nomenclature apply throughout this document:

a. The word "shall" is used in this document to express requirements. All the requirements are expressed with the word "shall".

b. The word "should" is used in this document to express recommendations. All the recommendations are expressed with the word "should".

NOTE It is expected that, during tailoring, all the recommendations in this standard are either converted into requirements or tailored out.

c. The words "may" and "need not" are used in this document to express positive and negative permissions respectively. All the positive permissions are expressed with the word "may". All the negative permissions are expressed with the words "need not".

d. The word "can" is used in this document to express capabilities or possibilities, and therefore, if not accompanied by one of the previous words, it implies descriptive text.

NOTE In ECSS "may" and "can" have a complete different meaning: "may" is normative (permission) and "can" is descriptive.

e. The present and past tense are used in this document to express statement of fact, and therefore they imply descriptive text.

4
Principles of reliable soldered connections

The following are the general principles to ensure reliable soldered connections:

- Reliable soldered connections are the result of proper design, control of tools, materials, processes and work environments, and workmanship performed in accordance to verified and approved procedures, inspection control and precautions.
- The basic design concepts to ensure reliable connections and to avoid solder joint failure are as follows:
  - Stress relief is an inherent part of the design, which reduces detrimental thermal and mechanical stresses on the solder connections.
  - Where adequate stress relief is not possible materials are so selected that the mismatch of thermal expansion coefficients is a minimum at the constraint points in the device mounting configuration.
- The assembled substrates are designed to allow easy inspection.
- Since only the outer row of solder joints to area array packages can be visually inspected, inner rows are inspected using X-ray techniques. To facilitate X-ray inspection of the solder joints to BGAs, the solder footprints can have a teardrop design.
- Circuit designs for area array devices, (e.g. BGA, CGA) have clearance around the perimeter of these packages to ensure that reflow nozzles can perform rework or repair operations (see ECSS-Q-ST-70-28). The clearance depends on the equipment used for reworking and the height of adjacent components.

  NOTE Unpopulated areas on the underside of the substrate assist indirect heating for removal of these packages.
- Soldering to gold using tin-lead alloy can cause failure.

5
Process identification document (PID)

5.1 General

5.1.1 Purpose

The purpose of the PID is to ensure that a precise reference is established for the assembly processes approved in accordance with this Standard.

The PID provides a standard reference against which any anomalies occurring after the approval can be examined and resolved.

5.1.2 Document preparation

a. The supplier shall prepare the PID in conformance with DRD from Annex F.

b. The supplier shall provide a draft PID prior to any start of verification to the Approval Authority.

c. The first issue of the PID shall fully comply to this standard.

d. For supplier, already approved on the basis of reliable tests results which supported the approval of any deviation finally recorded in the PID, then the PID may supersede the corresponding requirements from this standard.

5.1.3 <<deleted>>

a. <<deleted>>

b. <<deleted>>

5.1.4 Approval

a. The PID shall be submitted to the Approval Authority for approval.

NOTE The approval can be achieved by PID signature or minutes of meeting being signed by the Approval Authority.

b. <<deleted>>

5.1.5 SMT contact person

a. The supplier shall appoint a contact person for SMT topics.

5.2 <<deleted>>

a. <<deleted>>

b. <<deleted>>

c. <<deleted>>

d. <<deleted>>

e. <<deleted>>

5.3 Process identification document updating

a. The PID shall be managed in accordance with ECSS-M-ST-40.

b. A PID shall represent the current verified manufacturing processes and production controls.

c. Any proposed change to the PID shall be agreed by the Approval Authority.

d. <<deleted>>

e. The supplier shall initiate a review of the PID, the SMT summary table and the relevant applicable documents at least every two years for agreement by the Approval Authority.

6 Preparatory conditions

6.1 Calibration

a. The supplier shall maintain records of tool calibration and verification.

b. Requirements from clause 5.1 from ECSS-Q-ST-70-08 shall apply for "Calibration".

6.2 Facility cleanliness

a. Requirements from clause 5.2 from ECSS-Q-ST-70-08 shall apply for "Facility cleanliness".

6.3 Environmental conditions

a. Requirements from clause 5.3 from ECSS-Q-ST-70-08 shall apply for "Environmental conditions".

6.4 Precautions against static charges

a. Requirements from clause 5.5 from ECSS-Q-ST-70-08 shall apply for "Precautions against static charges".

6.5 Lighting requirements

a. Requirements from clause 5.4 from ECSS-Q-ST-70-08 shall apply for "Lighting requirements".

6.6 Equipment and tools

6.6.1 Brushes

a. Requirements from clause 5.6.2 from ECSS-Q-ST-70-08 shall apply for "Brushes".

6.6.2 Cutters and Pliers

a. Requirements from clause 5.6.3 from ECSS-Q-ST-70-08, shall apply for "Cutters and Pliers".

6.6.3 Bending tools

a. Requirements from clause 5.6.4 from ECSS-Q-ST-70-08 shall apply for "Bending tools".

6.6.4 Clinching tools

a. Requirements from clause 5.6.5 from ECSS-Q-ST-70-08 shall apply "Clinching tools".

6.6.5 Insulation strippers

a. Requirements from clause 5.6.6 from ECSS-Q-ST-70-08 shall apply for "Insulation strippers".

6.6.6 Soldering tools

a. Requirements from clause 5.6.8 from ECSS-Q-ST-70-08 shall apply for "Soldering tools".

6.6.7 Soldering irons and resistance soldering equipment

a. Requirements from clause 5.6.7 from ECSS-Q-ST-70-08 shall apply for “Soldering irons and resistance soldering equipment”.

b. For surface mounted devices, the soldering tip shall not exceed 340 °C.

NOTE Based on the device manufacturer’s recommendations, solder iron can be substituted by applying, for instance, hot air in order to avoid thermal shock.

6.6.8 <<deleted>>

a. <<deleted>>

6.6.9 Solder baths for degolding and pretinning

a. Requirements from clause 7.2.3.2.2 from ECSS-Q-ST-70-08 shall apply for "Solder baths" for degolding and pretinning.

6.7 Soldering machines and equipment

6.7.1 General

a. Machines and equipment used to solder surface mount devices shall either be a type incorporating dynamic single or dual solder wave, or be of the solder reflow type.

b. The soldering machine shall be grounded in order to avoid electrostatic discharge.

c. The supplier shall ensure that the soldering conditions do not exceed the values given by the individual device data sheets

NOTE Examples of soldering conditions include. maximum temperature to avoid internal melting, removal of marking ink, degradation of encapsulating plastic.

d. Temperature and time profiles for assembly shall be identified by the supplier and approved by the Approval Authority.

e. The supplier shall identify changes and implement a verification programme in compliance with the requirements from clause 14.13.

f. The supplier shall demonstrate the reproducibility of their reflow processes.

6.7.2 Dynamic wave-solder machines

a. Dynamic soldering machines shall be of automatic type and of a design offering the following:

1. Controllable preheating to drive off volatile solvents and to avoid thermal shock damage to the PCB and device packages.
2. The capacity to maintain the solder temperature at the printed circuit board assembly to within 5 °C of the established bath temperature throughout the duration of any continuous soldering run when measured 3,0 mm below the surface of the wave.
3. A wave system that limits shadowing and allows solder fillet formation.
4. Carriers made from a material that cannot contaminate, degrade or damage the printed circuit board or substrate nor transmit vibrations or shock stress from the conveyors to a degree permitting physical, functional or electrostatic damage to devices, board or substrate during transport through preheating, soldering and cooling stages.
5. An extraction system, either integral or separate, conforming to the requirements of clauses 6.2a and 6.3a.

6.7.3 Condensation (vapour phase) reflow machines

a. Condensation reflow machines shall conform to the following requirements:

1. Not transmit a movement or vibration into the assemblies being soldered that result in misalignment of devices or disturbed solder joints.
2. Be capable of preheating an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering.
3. Use a reflow fluid whose boiling point is a minimum of 12 °C above the melting point of the solder being used.
4. Maintain the preselected temperature to within ±5 °C in the reflow zone during soldering.
5. Include an extraction system that conforms to requirements 6.2a and 6.3a.

6.7.4 Hot gas reflow machines

a. Hot gas reflow machines shall conform to the following requirements:

1. Does not transmit movement or vibration to the assemblies being soldered which result in misalignment of devices or disturbed solder joints.
2. Preheats an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering.
3. <<deleted>>
4. Prevents the reflow of adjacent devices.
5. Maintains the preselected reflow temperature within ±5 °C as measured at the substrate surface.

6.7.5 <<deleted>>

a. <<deleted>>

6.7.6 Convection and radiation reflow systems

a. Convection and radiation reflow machines shall be of design such that the system meets the following requirements:

1. Provides a controlled temperature profile and does not transmit movement or vibration into the assembly being soldered.
2. Preheats an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering.

3. Heats the area of the assembly to be soldered using focused or unfocussed energy, to a preselected temperature that is a minimum of 12 °C above the melting point of the solder being used as measured at laminate or substrate surface.

4. Maintains the preselected temperature to within ±5 °C in the reflow zone during soldering.

6.7.7 Other equipment for reflow soldering

a. Other solder reflow systems may be approved for use by the Approval Authority, if compliance with clauses 6.7.1 to 6.7.6 is demonstrated.

6.8 Ancillary equipment

6.8.1 General

a. Equipment shall not generate, induce or transmit electrostatic charges to devices being placed.

b. The supplier shall demonstrate the reproducibility of their SMT processes.

6.8.2 Solder deposition equipment

a. Equipment used to deposit solder pastes shall be of a screening, stencilling, dispensing, roller coating, dotting or jet printing type.

b. Equipment shall apply pastes of a viscosity and quantity such that the positioned device is retained on the board before and during soldering operations, ensuring self-centring and solder fillet formation.

c. Equipment used to apply solder preforms shall ensure alignment of the preform with the land or device lead and termination.

6.8.3 Automatic device placement equipment

a. Automatic or computer controlled equipment used for device placement shall be of the coordinate-driven pick-and-place type or of the robotic type.

b. The placement equipment used shall be of a type that:

1. prevents device or board damages

2. indexes devices with respect to the circuit

3. aligns the device leads or castellations with the board terminal areas.

6.8.4 <<deleted>>

a. <<deleted>>

6.8.5 Cleanliness testing equipment

a. Requirements from clause 11.3.1 from ECSS-Q-ST-70-08 shall apply for "Cleanliness testing".

6.8.6 Magnification aids

a. Clause 13.1 shall apply.

6.8.7 X-ray inspection equipment

a. The maximum dose during X-Rays inspection shall be less than 5 % of the eligible dose of the most sensitive component according to its specification.

b. X-ray equipment shall be calibrated in order to evaluate the total dose received by the devices during the inspection.

NOTE In order to minimize the dose given to the device, it is good practice to:

- Record the total dose received.
- Use off-line image analysis as much as possible.
- Use filters, optimizing the direction of the X-ray beam and masking sensitive areas.

c. The resolution of the X-ray equipment shall be able to detect solder balls having a diameter of 0,03 mm.

d. The sensitivity shall be demonstrated by means of actual 0,03 mm diameter solder balls, stuck to adhesive tape, attached to the multilayer board assembly being inspected.

NOTE <<deleted>>

6.8.8 Metallographic equipment

a. The metallographic equipment shall enable cross-sectioning and polishing of the moulded solder interconnections.

7
Material selection

7.1 General

a. Material selection shall be performed in accordance with ECSS-Q-ST-70-71 and ECSS-Q-ST-70.

7.2 Solder

7.2.1 Form

a. Solder paste, ribbon, wire and preforms shall be used provided that the alloy and flux meet the requirements in clause 7.2.2.

b. Alloy for use in solder baths shall be supplied as ingots (without flux) and be compliant with requirements from clause 7.2.2.

7.2.2 Composition

a. The solder alloy shall have a composition specified in Table 7-1.

NOTE 1 Use EN 61190-1-3 for solder and EN 61190-1-1 for flux, EN 61190-1-2 for solder paste.

NOTE 2 The solder alloy used depends upon the application. See Annex E.2 for Guide for choice of solder type.

7.2.3 Solder paste

a. <<deleted>>

b. The metal purity shall be as specified in Table 7-1.

Table 7-1: Chemical composition of spacecraft solders

ESA designation	Sn min % - max %	Pb max %	In min % – max %	Sb max %	Ag min % – max %	Bi max %	Cu max %	Fe max %	Zn max %	Al max %	As max %	Cd max %	Other max %
63 tin solder	62,5-63,5	remainder	-	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
62 tin silver loaded	61,5-62,5	remainder	-	0,05	1,8-2,2	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
60 tin solder	59,5-61,5	remainder	-	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
96 tin solder	remain	0,10	-	0,05	3,5-4,0	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
75 indium lead	max 0,25	remainder	74,0-76,0	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
70 indium lead	0,00-0,10	remainder	69,3-70,7	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
50 indium lead	0,00-0,10	remainder	49,5-50,5	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
10 tin lead	9,0-10,5	remainder	-	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08

7.2.4 Maintenance of paste purity

a. When purchased premixed or mixed in house, the purity of solder paste shall be maintained.

b. Manufacturers' instructions shall be applied for the handling and storage of containers of solder paste purchased premixed.

c. Refrigerated solder paste shall reach room temperature before opening the container.

d. Neither paste purchased premixed nor paste mixed in-house shall be used if the use-by date or shelf life recommended by the manufacturer of the paste or paste constituents has expired.

e. When the solder paste's shelf life has expired it shall not be used unless:

   1. relifing is performed

   2. tests that include visual inspection and viscosity measurements (according to the manufacturer's recommendations) are passed successfully.

f. When relifing is performed, and the material passes the specified tests, the new shelf life shall be half the initial shelf life.

g. Tools used for removing solder paste from the container shall not contaminate the paste dispensed or that remaining within.

7.3 Flux

7.3.1 Rosin based flux

a. Requirements from clause 6.3.1 from ECSS-Q-ST-70-08 shall apply for "Rosin based flux".

7.3.2 Corrosive acid flux

a. Requirements from clause 6.3.2 from ECSS-Q-ST-70-08 shall apply for "INH1 Corrosive acid flux".

7.3.3 Flux controls for wave-soldering equipment

a. A controlled method shall be established and implemented for wave-soldering machines such that the flux is not contaminated with remaining residues from previous non-space works.

7.4 Solvents

a. Requirements from clause 6.4 from ECSS-Q-ST-70-08 shall apply for "Solvents".

7.5 Flexible insulation materials

a. Requirements from clause 6.5 from ECSS-Q-ST-70-08 shall apply for "Flexible insulation materials".

7.6 Terminals

a. Requirements from clause 6.6 from ECSS-Q-ST-70-08 shall apply for "Terminals".

7.7 Wires

a. Requirements from clause 6.7 from ECSS-Q-ST-70-08 shall apply for "Wires".

7.8 Printed circuit substrates

a. Printed Circuit Boards shall be designed in conformance with the requirements of clause 14 of ECSS-Q-ST-70-12.

b. Printed Circuit Boards shall be made of materials and manufactured in conformance with the requirements of clause 9 of ECSS-Q-ST-70-10.

c. Printed Circuit Boards shall be procured in conformance with the requirements of clauses 5 and 6 of ECSS-Q-ST-70-11.

7.8.1 <<deleted>>

a. <<deleted>>

b. <<deleted>>

c. <<deleted>>

Table 7-2: <<deleted>>

7.8.2 <<deleted>>

a. <<deleted>>

7.8.3 <<deleted>>

a. <<deleted>>

7.8.4 <<deleted>>

a. <<deleted>>

7.8.5 <<deleted>>

a. <<deleted>>

7.8.6 <<deleted>>

a. <<deleted>>

7.9 Devices

7.9.1 General

a. Devices and their finishes shall be selected from those approved in conformance with requirements from clauses 4, 5 and 6 of ECSS-Q-ST-60, for "manufacturer and component evaluation" and "Procurement control".

b. <<deleted>>

c. Solder may be applied to the terminations by hot dipping or by electroplating from a solution.

NOTE Devices with terminations finished by electroplating can impact the device wetting.

d. <<deleted>>

e. The incoming inspection of each device batch shall include the verification by test of the termination composition, to avoid assembly of pure tin finish, in accordance with requirement 4.3.7b from ECSS-Q-ST-60.

f. Pure tin finish with more than 97 % purity shall not be used.

NOTE This is due to the possibility of whisker growth and transformation to grey tin powder at low temperatures.

g. <<deleted>>

h. <<deleted>>

i. Devices shall be capable of withstanding cleaning processes currently used in space projects.

j. Parts with silver palladium finish shall not be used.

k. Reprocessing shall not damage the device.

NOTE Reprocessing of ceramic chip capacitors is advised to be avoided due to potential crack formation.

l. If devices initially designed for insertion-mount application are used for surface mounting, they shall be of a type that can be surface-mount adapted.

m. The adaptation specified in the requirement 7.9.1l shall not functionally or physically degrade the device or the substrate to which the adapted device is to be attached.

n. Connectors shall be of a configuration incorporating either male or female quick-disconnect contacts and stress relief provision for the soldered connection of each individual contact when such connections are completed.

o. Type II chip ceramic capacitors shall not be reworked.

7.9.2 <<deleted>>

a. <<deleted>>

b. <<deleted>>

c. <<deleted>>

7.9.3 Moisture sensitive devices

a. Moisture sensitive devices shall be stored and handled in conformance with the device manufacturer's recommendations. .

NOTE Many types of plastic encapsulated devices, particularly some plastic BGAs, are moisture sensitive.

b. When moisture sensitive devices are used, bakeout shall be performed in accordance with clause 8.5b.

7.9.4 <<deleted>>

a. <<deleted, modified and moved to 7.9.1l>>

b. <<deleted, modified and moved to 7.9.1m>>

c. <<deleted>>

d. <<deleted>>

e. <<deleted and moved to 7.9.1n>>

7.10 Adhesives, encapsulants and conformal coatings

a. Adhesives shall be dispensable, non-stringing, and have a reproducible dot profile after application.

b. Adhesives, encapsulants and conformal coating shall be non-corrosive to devices and substrates.

c. The uncured strength shall be capable of holding devices during handling prior to curing.

d. Adhesives, encapsulants and conformal coatings shall conform to the outgassing requirements of ECSS-Q-ST-70-02.

e. Adhesives, encapsulants and conformal coatings shall have no adverse effects upon materials used on the substrate, or devices attached thereon.

NOTE The effects of some conformal coatings on the reliability of mounted SMDs are described in ESA SP-1173.

f. Adhesives, encapsulants and conformal coatings shall be selected based on their thermal conductivity and dielectric properties.

NOTE Some thermally conductive adhesives used to dissipate Joule heating are listed in ESA STM-265 "Evaluation of Thermally Conductive Adhesives as Stacking Compounds during the Assembly of Spacecraft Electronics".

g. The capability of the adhesives to meet their requirements shall be demonstrated by means of a verification programme in conformance with clause 14.

NOTE <<deleted>>

h. Stress relief of device leads shall not be negated by the encapsulants or conformal coatings.

NOTE 1 This is particularly important at low service temperatures.

NOTE 2 The coefficient of expansion, glass transition temperature and modulus of adhesives used under devices for thermal reasons, for achieving stand-off heights or mechanical support during vibration, can be considered to ensure that the additional stress put on the solder joints does not degrade the solder joint reliability.

i. Adhesive shall not be in contact with terminal of component.

j. Bonding shall not be performed on fused tin lead unless the tin lead surface is limited to < 25 % by area of the bonding surface and demonstrated by verification as specified in clause 14.

k. Spread of bonding material onto surrounding areas shall not be accepted unless it does not reduce the volume of the initial bonding joint.

l. Bonding material shall not be in contact to surrounding devices.

m. Bonding with epoxy adhesive directly to glass bodied devices shall not be used.

NOTE It is good practice to use a sleeve between glass and the epoxy adhesive.

8
Preparation for soldering

8.1 Preparation of devices and terminals

8.1.1 Preparation of wires and terminals

a. Requirements from clause 7.2 from ECSS-Q-ST-70-08, clause "Preparation of conductors, terminals and solder cups" shall apply.

8.1.2 Preparation of surfaces to be soldered

a. Requirements from clause 7.2.2 from ECSS-Q-ST-70-08, clause "Surfaces to be soldered" shall apply.

8.1.3 Degolding and pretinning of conductors

a. Requirements from clauses 7.2.3 and 7.2.4 from ECSS-Q-ST-70-08 shall apply for "Degolding and pretinning of conductors".

8.1.4 Alloying of pure tin finish

a. <<deleted>>

b. Pure tin device terminations shall be pretinned with full tin lead solder coverage.

c. Pure tin device terminations shall be in compliance with requirements from clauses 7.2.4 and 7.2.6 of ECSS-Q-ST-70-08 and requirement 8.1a from ECSS-Q-ST-60-13.

NOTE 1 Pure tin terminations can be dipped into liquid solder as described in ECSS-Q-ST-70-08, clause 7.2.6 in order to replace the tin with tin-lead alloy.

NOTE 2 Reprocessing of ceramic chip capacitors is not recommended due to potential crack formation.

d. The reprocessing process shall be verified by micro sectioning and SEM/EDX with respect to alloying and full coverage.

8.2 Preparation of solder bit

a. Requirements from clause 7.3 from ECSS-Q-ST-70-08 shall apply for "Preparation of solder bit".

8.3 Handling

a. Requirements from clause 7.5 from ECSS-Q-ST-70-08 shall apply for "Handling".

8.4 Storage

a. Requirements from clause 7.6 from ECSS-Q-ST-70-08 shall apply for "Storage".

8.5 Baking of PCBs and moisture sensitive devices

a. <<deleted>>

b. Baking of moisture sensitive devices shall be implemented before any reprocessing or assembly process in conformance with JEDEC classification.

NOTE This is to counteract the "popcorn" effect in soldering using oven or vapour phase reflow techniques.

c. Baking times and temperatures, for moisture sensitive devices, shall be in compliance with manufacturer recommendations and baking times as specified in J-STD-033 and documented.

NOTE 1 Typical baking conditions are from 6 h to 24 h at 125 °C depending on the JEDEC classification, except for devices delivered in reels for which a lower temperature and longer time are used.

NOTE 2 It is good practice to store devices under nitrogen, dry air (20 % RH maximum) or partial vacuum.

d. Baking of unpopulated PCBs should be made as a minimum of 8 hours at 120 °C.

e. Baking of populated PCBs shall be performed when the PCB has been kept under clean room conditions for more than 72 hours.

NOTE Storage of PCBs in dry cabinet interrupts the accumulated baking time.

f. Baking of populated PCB shall be made at a temperature which does not degrade the devices or assembly.

NOTE To limit the bake out operation, which can induce later failure, the PCB can be stored in dry environment after the baking.

9
Mounting of devices prior to soldering

9.1 General requirements

a. Requirements from clause 8.1 from ECSS-Q-ST-70-08, “Mounting of components – General” shall apply.

9.2 Lead bending and cutting requirements

a. Requirements from clause 8.2 from ECSS-Q-ST-70-08, clause “Lead bending requirements” shall apply.

9.3 Mounting of terminals to PCBs

a. Requirements from clause 8.3 from ECSS-Q-ST-70-08 shall apply for "Mounting of terminals to PCBs".

9.4 Lead attachment to through holes

a. Requirements from clause 8.4 from ECSS-Q-ST-70-08 shall apply for "Lead attachment to through holes".

9.5 Mounting of devices to terminals

a. Requirements from clause 8.5 from ECSS-Q-ST-70-08 shall apply for "Mounting of components to terminals".

9.6 Mounting of through hole connectors to PCBs

a. Requirements from clause 8.6 from ECSS-Q-ST-70-08 shall apply for "Mounting of through hole connectors to PCBs".

9.7 Surface mount requirements

9.7.1 General

a. Devices to be mounted shall be designed for, and be capable of withstanding the soldering temperatures of the particular process being used for fabrication of the assembly.

NOTE Surface mounted devices can be mounted on either one side or both sides of a printed circuit assembly.

b. <<deleted>>

c. Devices incapable of withstanding machine soldering temperatures shall be hand soldered in a subsequent operation.

d. Supplier shall ensure that degolding, pretinning, reprocessing and soldering conditions do not exceed the device suppliers mandated processing conditions.

NOTE 1 In case of non-compliant mounting procedure with a component manufacturer, a company can apply different soldering temperature compliant with clause 6 after successful verification tests as described in clause 14 and dedicated tests at component levels showing there is no degradation of these components.

NOTE 2 To mount component by hand soldering at very low temperature can degrade reliability of component and PCB by increasing the duration of soldering necessary to obtain an acceptable solder joint.

e. Supplier shall ensure that degolding and pretinning has been performed such that the solder fillet is not in contact with the gold or AuSn intermetallic.

f. Supplier shall ensure repeatability of the mounting when artificial standoff is adopted.

9.7.2 Stress relief

a. When PCBs with high CTE compensation are employed, the supplier shall accommodate CTE mismatch by the mounting technology.

NOTE 1 Pure eutectic tin-lead solder or indium-lead solder provide better stress relief (due to their ductility) than those with additional elements, e.g. antimony, gold.

NOTE 2 Leadless devices with e.g. end-cap terminations, metallization, can have some stress relief (such as additional foil or wire

leads, possibly attached by welding or high melting point solder).

NOTE 3 A solder stand-off (see Figure 11-1, dimension "X") can assist stress relief; in this situation, the CTE mismatch strain is taken up by the ductile solder.

NOTE 4 <<deleted>>

9.7.3 Registration of devices and footprints

a. Devices shall be mounted on their associated terminal footprints .

b. The spacing between conductive elements shall not be reduced below the minimum electrical spacing specified in clause 7.3 of ECSS-Q-ST-70-12.

NOTE Some surface mounted devices that are not bonded to the PCB can self-align during the soldering process. It is the registration after soldering that is important.

9.7.4 Lead forming

a. The leads of leaded surface mount devices shall be formed to their final configuration prior to mounting.

b. Forming shall not degrade the solderability or cause loss of plating adhesion to the leads.

c. Forming shall not cause mechanical damage to the leads or attachment seals.

d. Leads of dual-in-line and gull-wing packages, flat-packs and other multileaded devices shall be dressed, mechanically re-aligned to ensure co-planarity providing that the lead to package connection is not subjected to plastic deformation.

e. Formed leads shall not be re-bent.

f. Lead forming shall be symmetrical.

9.7.5 Mounting devices in solder paste

a. Both leaded and leadless surface mounted devices shall be mounted in solder paste prior to reflow soldering.

NOTE It is good practice to optimize the pick and place mounting force on the device lead, ball or column.

b. The solder paste deposited on each solder land shall be visually inspected for registration and coverage by the operator prior to mounting the devices.

NOTE <<deleted>>

9.7.6 Leadless devices

a. Devices shall not be stacked.

b. <<deleted>>

c. The active element shall be mounted with that surface facing away from the printed circuit board or substrate, except the case specified in the requirement 9.7.6g.

NOTE See Figure 9-1 for details.

d. Devices that are bonded to the PCB prior to wave- or reflow-soldering shall be placed so that the requirements after soldering given in clause 11 are met.

e. The adhesive shall not extend onto the solder footprints.

f. Artificial solder stand-off shall be reproducible.

NOTE Artificial solder stand-off can be achieved by removable spacers or other techniques in conformance with assembly process procedures.

g. The active element may be facing the substrate in case required by electrical performance.

NOTE For example: RF applications.

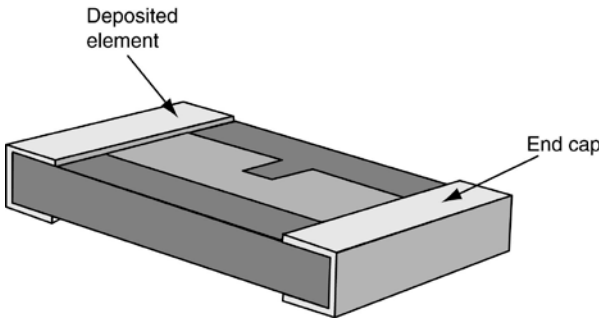


Figure 9-1: Exposed element

9.7.7 Leaded devices

a. Surface mounting of leaded (round or rectangular cross section) devices shall be parallel to the board surface.

9.7.8 <<deleted>>

a. <<deleted>>

9.7.9 Stacking and bonding of heavy devices

a. Adhesive shall be selected in conformance with clause 7.10.

NOTE Some surfaces can be prepared to enhance the adhesion (e.g. by mechanical abrasion).

b. <<deleted>>

c. Adhesive shall be mixed and cured in accordance with the manufacturer's procedures.

d. The process of applying the adhesive shall be documented by a written procedure or by configured drawings which define the location of the adhesive, the shape and the spread area (between device bottom surface and substrate upper surface).

e. The adhesive shall not be in contact with the terminal or negate the stress relief of the device, nor come into contact with surrounding devices.

f. <<deleted and created as recommendation 9.7.9g>>

g. All devices weighing more than 5 g should be stacked.

NOTE 1 This is to minimize shock and vibration loading on the leads.

NOTE 2 The adhesive compound can be applied either before or after soldering in conformance with the supplier's process identification document.

h. Stacking and bonding shall be performed on clean surfaces.

10
Attachment of conductors to terminals, solder cups and cables

a. Requirements from clause 9 from ECSS-Q-ST-70-08 shall apply for "Attachment of conductors to terminals, solder cups and cables".

11 Soldering to printed circuit boards

11.1 General

a. Requirements from clause 10.1 from ECSS-Q-ST-70-08, clause “Soldering to terminals and printed circuit boards – General” shall apply.

11.2 <<deleted>>

a. <<deleted>>

11.3 Solder applications to PCBs

a. Requirements from clause 10.3 from ECSS-Q-ST-70-08 shall apply for "Solder applications to PCBs".

11.4 Wicking

a. Requirements from clauses 10.3.1, 10.3.2, 10.3.4 and 10.4 from ECSS-Q-ST-70-08 shall apply for "Wicking".

11.5 Soldering of SMDs

11.5.1 General requirements

a. Devices shall not be mounted on flexible substrates as defined “flexible printed boards” in ECSS-Q-ST-70-10.

b. Soldering to gold with tin-lead alloys shall not be performed.

NOTE 1 See also requirement 11.5.1h.

NOTE 2 See also clause 8.1.3 "Degolding and pretinning of conductors".

c. Devices shall not be stacked nor bridge the space between other devices or terminals.

d. Positioning of devices shall not reduce the specified minimum electrical clearance to adjacent tracks or other metallized elements in conformance with requirements from clause 13 and clause 14 of ECSS-Q-ST-70-12.

e. Non-axial-leaded devices shall be mounted with all leads seated on a terminal area to ensure mechanical strength.

f. Solder shall cover and wet the solderable surfaces as specified in clause 13.2.

g. The footprint shall be designed as the entire terminal of the device lies on its associated footprint on the finished board.

h. Soldering to gold finish with tin-lead shall not be performed unless the gold finish is thinner than 0,1 µm and all the following conditions are met:

1. PCB is qualified in compliance with the requirements of clause 6 of ECSS-Q-ST-70-10,
2. Assembly verification programme is reviewed and accepted by the Approval Authority, and
3. Assembly verification is compliant to requirements of clause 14.

i. The device footprint on FM shall be same as used in verification programme.

j. Devices verified by similarity shall use same design principle for the footprint.

k. The device positioning shall be such that visual inspection can be undertaken.

l. If visual inspection of a fully populated assembly is not possible, the assembly and inspection shall be made in steps enabling visual inspection.

m. Artificial stand-off value shall be documented in procedure.

n. The footprint design shall be done in such way as to avoid, during soldering, contact between the device and the soldering tip.

o. Any deviation to requirements from clauses 11.5.2 to 11.5.11 shall be demonstrated by verification in compliance with requirements from clause 14.

11.5.2 End-capped and end-metallized devices

a. There shall be no discernible discontinuities in the solder coverage of the terminal areas of devices.

b. Solder shall not encase any portion of the body of the device following reflow.

c. The solder joints to these devices shall meet the dimensional and solder fillet requirements of Table 11-1 and Figure 11-1.

NOTE End-capped and end-metallized devices having terminations of a square or rectangular

configuration (such as chip resistors, chip capacitors and similar leadless discrete devices) can have three or five face terminations, as shown in "a" and "b" in Figure 11-1.

Table 11-1: Dimensional and solder fillet for rectangular and square end capped devices

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
End overhang	B	Not permitted
Minimum lap contact	L	75% single terminal length only Entire terminal of device for sensitive device
Minimum fillet height	E	X + 0,3 × H or X + 0,5 mm whichever is less
Solder Stand-off (elevation)	X	Present
Maximum tilt limit	C	10°

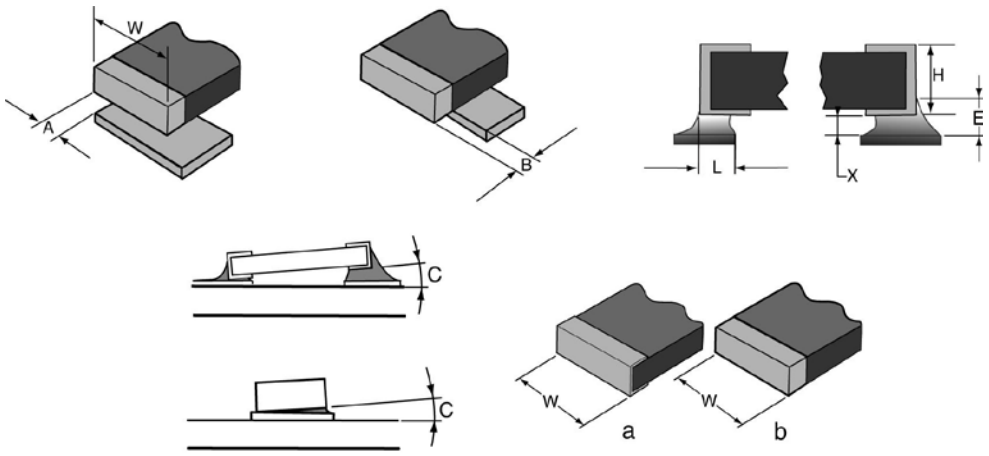


Figure 11-1: Mounting of rectangular and square end-capped and end-metallized devices

11.5.3 Bottom terminated chip devices

a. Devices having metallized terminations on the bottom side only shall meet the dimensional and solder fillet requirements of Table 11-2 and Figure 11-2.

b. Solder fillet shall show acceptable wetting on all visible sides.

Table 11-2: Dimensional and solder fillet for bottom terminated chip devices

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
End overhang	B	Not permitted
Minimum lap contact	L	Entire terminal of device
Solder Stand-off (elevation)	X	Present
Maximum tilt limit		10°

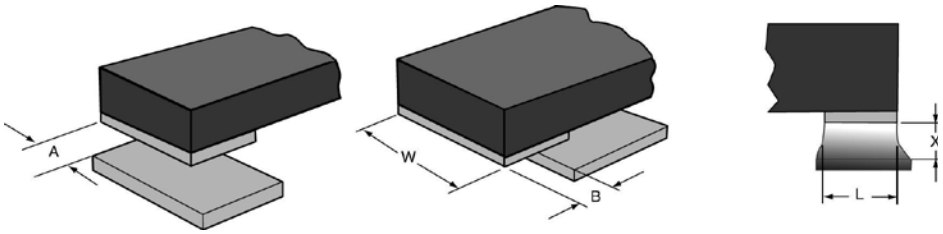


Figure 11-2: Mounting of bottom terminated chip devices

11.5.4 Cylindrical and square end-capped devices

a. Solder joints to devices having cylindrical terminations shall meet the dimensional and solder fillet requirements of Table 11-3 and Figure 11-3.

Table 11-3: Dimensional and solder fillet for cylindrical end-capped devices

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,25 × D
End overhang	B	Not permitted
Minimum fillet width	F	0,5 × D
Minimum fillet height	E	X + 0,3 × D or X + 1,0 mm whichever is less
Minimum side fillet length	L	0,5 × T
Stand-off (elevation)	X	Present up to 0,75 mm

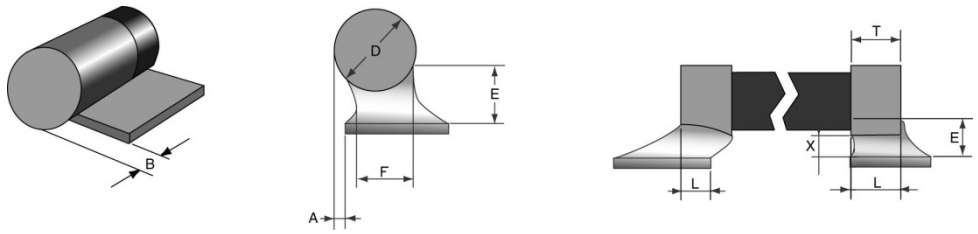


Figure 11-3: Mounting of cylindrical end-capped devices

b. Solder joints to devices having square terminations shall meet the dimensional and solder fillet requirements of Table 11-4 and Figure 11-4.

Table 11-4: Dimensional and solder fillet for square end-capped devices

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,25 × W (square width)
End overhang	B	Not permitted
Minimum fillet width	F	0,5 × W
Minimum fillet height	E	X + 0,3 × W or X + 1,0 mm whichever is less
Minimum side fillet length	L	0,5× T
Stand-off (elevation)	X	Present up to 0,75 mm

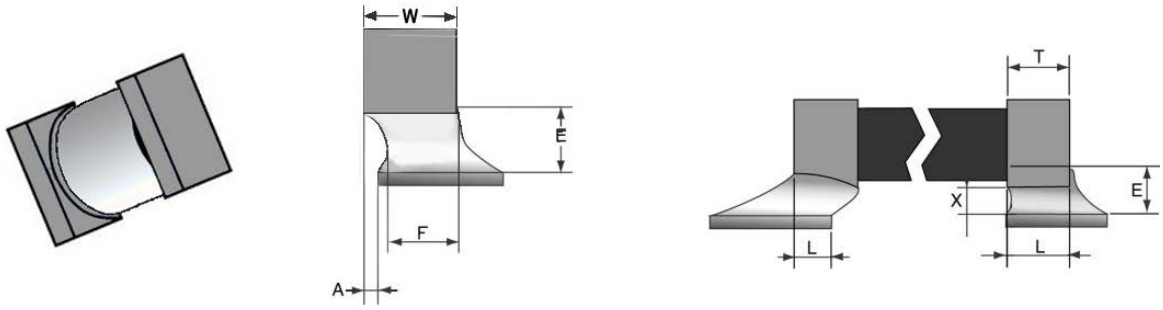


Figure 11-4: Mounting of square end-capped devices

11.5.5 Castellated chip carrier devices

a. Joints to castellated device terminations shall meet the dimensional and solder fillet requirements of Table 11-5 and Figure 11-5.

NOTE 1 The stand-off enables adequate cleaning beneath the assembled LCCC and also to enhance solder fatigue life (see also clause 9.7.6f)

NOTE 2 <<deleted>>

Table 11-5: Dimensional and solder fillet for castellated chip carrier devices

Parameter	Dimension	Dimension limits
Maximum side overhang	A	Zero
Maximum fillet length	F	P (length of the pad)
Minimum fillet height	E	0,50 × H (H= Castellation metallisation height)
Solder Stand-off (elevation)	X	Present
Underneath lap connection		Entire terminal of device

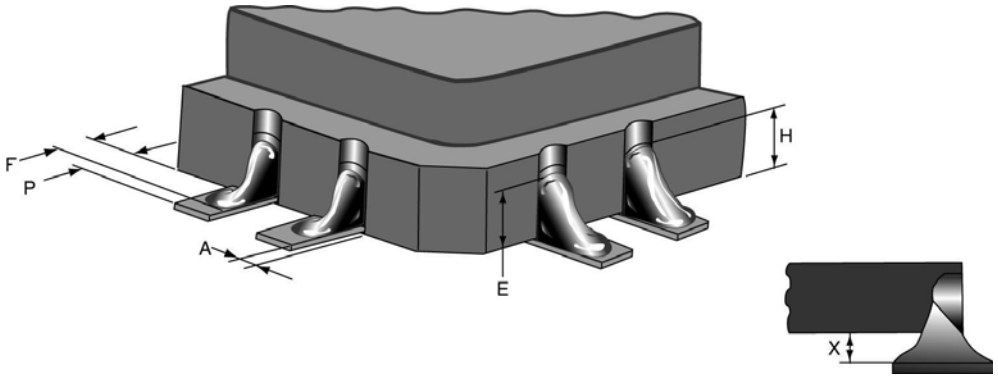


Figure 11-5: Mounting of castellated chip carrier devices

11.5.6 Flat pack and Gull-wing leaded devices with round, rectangular, ribbon leads

a. Solder joints formed to flat pack and gull-wing leaded devices with round, rectangular, ribbon leads shall meet the dimensional and solder fillet requirements of Table 11-6 and Figure 11-6.

b. Solder fillet shall be visible on the side of the terminal lap connection.

Table 11-6: Dimensional and solder fillet for gull-wing leaded devices with round, rectangular, ribbon leads

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum distance to footprint edge at toe	B	0,20 mm
Minimum distance to footprint edge at heel	L	0,5 × W
Minimum side joint length	D	full lap connection soldered
Minimum heel fillet height	E	X + T
Solder Stand-off	X	Present

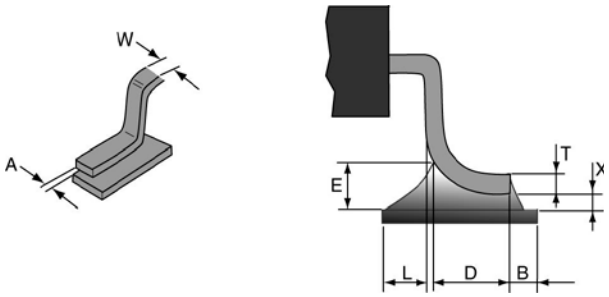


Figure 11-6: Mounting of gull-wing leaded devices with round, rectangular, ribbon leads

11.5.7 Devices with "J" leads

a. Solder joints formed to "J" and "V" shaped leads shall meet the dimensional and solder fillet requirements of Table 11-7 and Figure 11-7.

Table 11-7: Dimensional and solder fillet for devices with "J" leads

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum side joint length	L	1,5 × W
Minimum heel fillet height	M	X + T
Maximum stand-off	X	Present

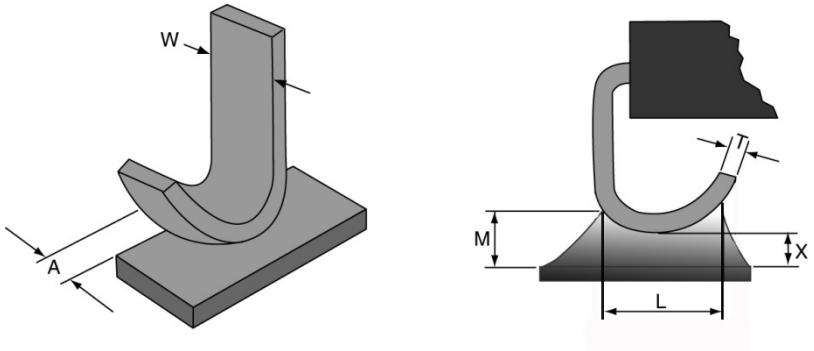


Figure 11-7: Mounting of devices with "J" leads

11.5.8 Area array devices

a. The outer row of solder joints to area array devices shall be visually inspected by looking from the side in accordance with the requirements in 11.5.1 and Table 11-8 and with the rejection criteria specified in clauses 13.3 and 13.4.

b. Solder joints shall be inspected using X-ray techniques in accordance with clause 6.8.7 and Table 11-8.

NOTE 1 <<deleted>>

NOTE 2 As it is impossible to visually inspect solder joints to area array devices, reliability of these devices cannot be assured by inspection and rework. Even using X-ray techniques, some types of defect are difficult to detect. Therefore, reliability of these solder joints can only be assured by robust process control.

NOTE 3 Examples of typical area array devices are shown in Figure 11-8, Figure 11-9 and Figure 11-10.

c. X-ray techniques shall be used to verify the acceptable wetting, the absence of bridge, solder balls and minimum electrical clearance.

Table 11-8: Dimensional and solder fillet for area array devices

Parameter	Dimension limits
Misalignment	No footprint overhang
BGA ball	Collapse of BGA ball does not violate minimum electrical clearance or become less than 0,10 mm.
Maximum device height	Overall height of device does not exceed maximum specified.
Soldered connection	a. BGA balls contact and wet to the land forming a continuous connection b. CGA solder columns contact and wet to the land forming a continuous connection
Solder balls	No solder balls.
Maximum CGA column tilt	10 degrees
D = Ball or column diameter	

Figure 11-8: <<deleted>>

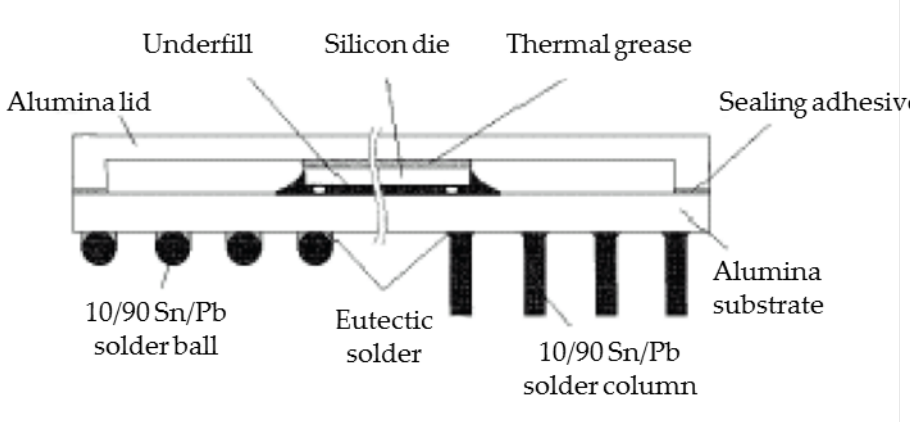


Figure 11-9: Typical ceramic area array showing ball grid array configuration on left and column grid array on right (CBGA & CCGA)

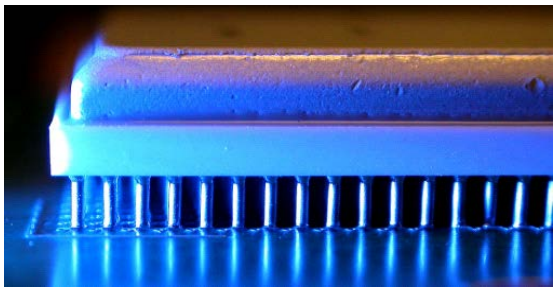


Figure 11-10: Typical assembled CCGA device

11.5.9 Devices with ribbon terminals without stress relief

a. Solder joints formed shall meet the dimensional and solder fillet requirements of Table 11-9 and Figure 11-11.

b. The degolding and pretinning zone shall be outside the PCB footprint.

NOTE This is to ensure that the degolding and pretinning has been performed such that the solder fillet is not in contact with the gold or AuSn intermetallic.

Table 11-9: Dimensional and solder fillet for devices without stress relief

Parameter	Dimension	Dimensions Limits
Maximum side overhang	A	≤ 0,1 x W
Minimum distance to footprint edge at toe	B	≥ 0,20 mm
Stand-off	X	Present
Minimum side joint fillet	D	3xW with full lap soldered connection
Maximum tilt	C	10°

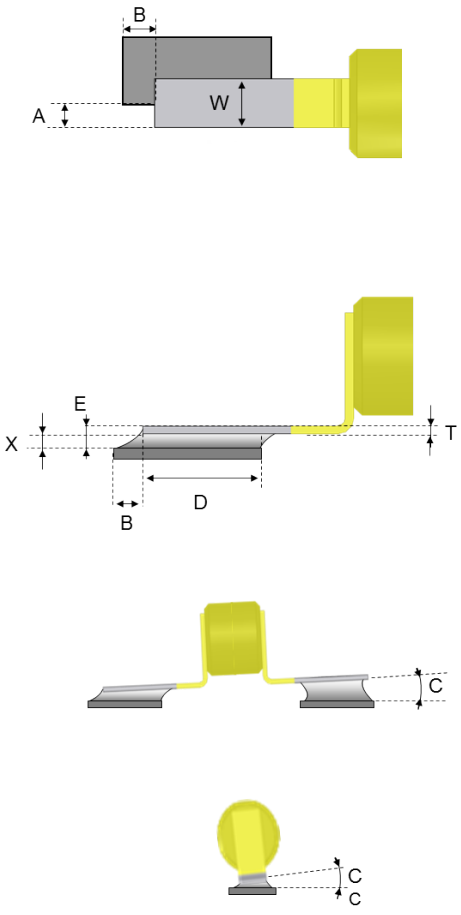


Figure 11-11: Mounting of devices without stress relief

11.5.10 L-Shape inwards devices

a. Devices having L-shape inwards terminals shall meet the dimensional and solder fillet requirements of Table 11-10 and Figure 11-12.

b. Solder fillet shall be visible on the side of the terminal on the connection.

c. The device shall be centred on its footprints such as the minimum lap contact length is fulfilled.

Table 11-10: Dimensional and solder fillet for "L-shape inwards" devices

Parameter	Dimension	Dimension limits
Minimum fillet height, heel	E	(0,25 x H)+X or X +1mm whichever is less
Minimum distance to footprint edge	K	0,2 mm
Minimum Lap contact length	L	75% terminal of device, limited to one side
Stand-off (elevation)	X	Present
Side of terminal wetting		Evidence of solder wetting

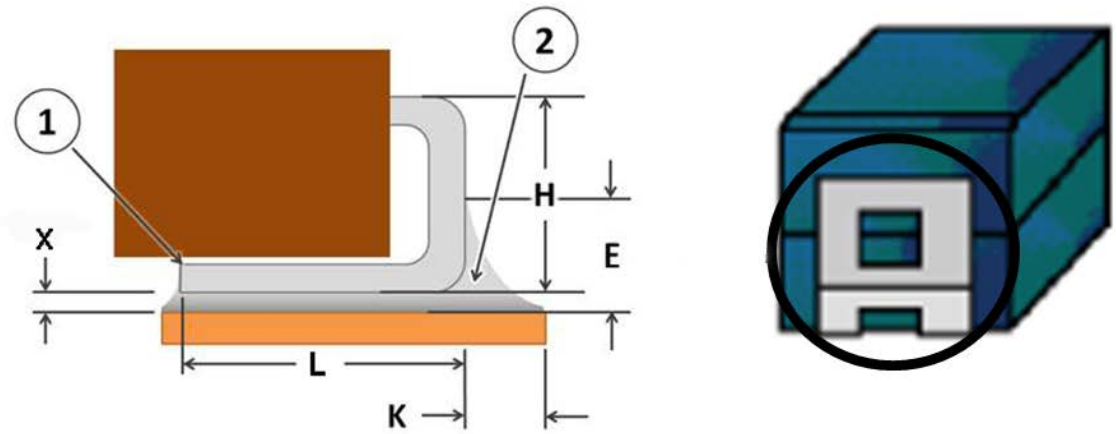


Figure 11-12: Mounting of devices with "L-shape inwards" leads (1 = Toe, 2 = Heel)

11.5.11 Stacked modules devices with leads protruding vertically from bottom

a. Stacked modules devices shall meet the dimensional and solder fillet requirements of Table 11-11 and Figure 11-13.

b. Solder fillet shall be visible in the heel fillet.

Table 11-11: Dimensional and solder fillet for stacked modules devices with leads protruding vertically from bottom

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum distance to footprint edge at toe	B	0,20 mm
Minimum distance to footprint edge at heel	L	0,5 × W
Minimum side joint length	D	full lap connection soldered
Minimum heel fillet height	E	Wetting solder visible in the heel fillet, X+ 0,5T
Solder Stand-off	X	Present
Lead thickness	T	

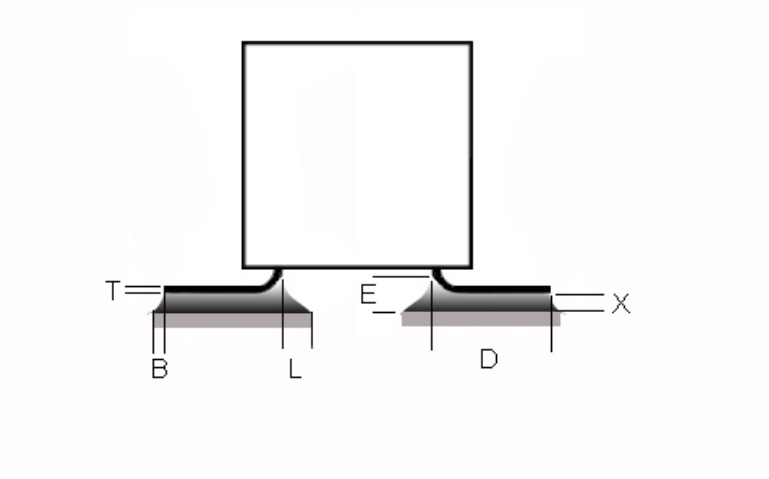


Figure 11-13: Mounting of stacked modules devices with leads protruding vertically from bottom

11.5.12 Leaded device with plane termination

a. Leaded devices with plane termination shall meet the dimensional and solder fillet requirements of Table 11-12 and Figure 11-14.

b. Solder fillet shall be visible in the heel fillet.

c. Termination plane shall be inspected with X-ray equipment according to clause 6.8.7.

d. Plane termination shall meet X-ray criterion according to requirements 13.4a.2 to 13.4a.5.

Table 11-12: Dimensional and solder fillet for leaded devices with plane termination

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum distance to footprint edge at toe	B	0,20 mm
Minimum distance to footprint edge at heel	L	0,5 × W
Minimum side joint length	D	full lap connection soldered
Minimum heel fillet height	E	X + T
Solder Stand-off	X	Present

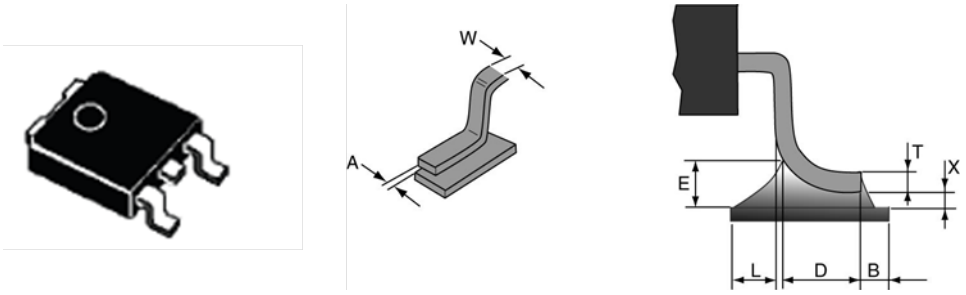


Figure 11-14: Mounting of leaded devices with leads with plane termination

11.5.13 Moulded magnetics

a. Moulded magnetics devices shall meet the dimensional and solder fillet requirements of Table 11-11 and Figure 11-6.

b. Solder fillet shall be visible in the heel fillet.

11.6 <<deleted>>

a. <<deleted>>

b. <<deleted>>

Figure 11-15: <<deleted>>

11.7 <<deleted>>

a. <<deleted>>

11.8 <<deleted>>

a. <<deleted>>

12
Cleaning of PCB assemblies

12.1 General

a. Requirements from clause 11.1 from ECSS-Q-ST-70-08, clause “Cleaning of PCB assemblies – General” shall apply.

12.2 Ultrasonic cleaning

a. Requirements from clause 11.2 from ECSS-Q-ST-70-08 shall apply for "Ultrasonic cleaning".

12.3 Monitoring for cleanliness

a. Requirements from clause 11.3 from ECSS-Q-ST-70-08 shall apply for "Monitoring for cleanliness".

13
Final inspection

13.1 General

a. Each soldered connection shall be visually inspected in accordance with the criteria specified in the requirements 13.1d, 13.1e, and 13.1f

b. <<deleted>>

c. <<deleted>>

d. Devices and conductors shall not be physically moved to aid inspection.

e. The substrate, solder joint, devices and device position, shall be inspected in accordance with the requirements in clause 11.5.

NOTE Annex I includes examples of acceptable and unacceptable workmanship.

f. The assembly shall be visually inspected in two steps with the following methodology:

1. Visual inspection of the assembly is aided by magnification appropriate to the size of the connections between 4x and 10x.
2. Detailed inspection is performed with a minimum magnification 20x.

g. Additional magnification shall be used to resolve suspected anomalies or defects up to 40x.

h. X-ray inspection shall be applied when there are hidden solder joints that are not visually accessible.

13.2 Acceptance criteria

a. Acceptable solder connections shall be characterised by:

1. clean, smooth, satin to bright undisturbed surface,
2. solder fillets between conductor and termination areas as described in clause 11.5,
3. visible contour of wires and leads such that their presence, direction of bend and termination end can be determined,
4. complete wetting as evidenced by a low contact angle between the solder and the joined surfaces,

5. acceptable amount and distribution of solder in accordance with clause 11.5,

6. absence of any of the defects mentioned in clauses 13.3 and 13.4.

NOTE Annex I includes examples of acceptable and unacceptable workmanship.

13.3 Visual rejection criteria

a. The following are some characteristics of unsatisfactory conditions, any of which shall be cause for rejection:

1. charred, burned or melted insulation of devices,
2. conductor pattern separation from circuit board,
3. burns on base materials,
4. <<deleted>>
5. excessive solder (including peaks, icicles and bridging), see clause 11.5,
6. flux residue, solder splatter, solder balls, or other foreign matter on circuitry, beneath devices or on adjacent areas,
7. dewetting,
8. insufficient solder, see clause 11.5,
9. pits, holes or voids where bottom is not visible,
10. granular or disturbed solder joints,
11. fractured or cracked solder connection,
12. cut, nicked, gouged or scraped conductors or conductor pattern,
13. <<deleted>>
14. <<deleted>>
15. damaged conductor pattern,
16. bare copper or base metal, excluding the ends of cut wire or leads or sides of tracks and soldering footprints on substrate,
17. soldered joints made directly to gold-plated terminals or gold-plated conductors using tin-lead solders,
18. cold solder joints,
19. device body embedded within solder fillet,
20. open solder joints (e.g. tombstoning),
21. probe marks present on the metallization of chip devices caused by electrical testing after assembly,
22. glass seal does not conform to MIL-STD-883 Method 2009,
23. any nonconformance with clause 11.5,
24. measling which violates the minimum insulation distance,

25. delamination, except within region of the breakout regions for multi-panel processed,
26. exposed base metal excluding area of cut leads in the soldered connection,
27. cracks detected in glass diodes outside the relevant devices procurement standard,
28. bent connector pins outside the relevant devices procurement specification,
29. damage of the lead, device or PCB beyond that defined in the procurement standard of the item,
30. degraded insulation material of the connector in contact area,
31. bubble or void in the conformal coating or potting that are bridging conductive elements,
32. bubble, void or delamination in conformal coating and or potting between high voltage conductors,
33. lack of intended conformal coating,
34. unintended and continuous adhesive forming a bridge in contact with terminals, component body or solder joints,
35. excessive degolding,
36. insufficient degolding,
37. direct bonding on glass device body with epoxy,
38. separation of adhesive from the bonded surface,
39. separation of conformal coating from the surface,
40. any longitudinal misalignment on sensitive devices,
41. longitudinal misalignment of end capped and end metallized devices,
42. presence of cracks in the ceramic of devices or cover of device.

NOTE 1 For requirement 13.3a.29, end cap metallization peeling crack in device, missing metallization are examples of damage.

NOTE 2 For requirement 13.3a.29, cracks in ceramics mainly occur in chip capacitors, and leadless device with thermal plane termination.

NOTE 3 For the requirement 13.3a.32, high voltage applications are defined in ECSS-E-HB-20-05.

13.4 X-ray rejection criterion

a. The following are some characteristics of not acceptable conditions from X-ray inspection, utilizing equipment defined in clause 6.8.7, any of which shall be cause for rejection:

1. criteria and dimensions outside the limits given in Table 11-8 for area array devices,
2. bridges and other unintended metallic materials,
3. non-wetting of the solder,
4. cumulative voids greater than 25 % by area of the solder joint,
5. a single void which traverses either length or width of the terminal and exceed 10 % of the total area.

NOTE For the requirement 13.4a.2 solder balls are a typical example of unintended metallic material.

b. Any deviation to requirement 13.4a.4 shall be demonstrated by verification in compliance with requirements from clause 14.

13.5 Warp and twist of populated boards

a. <<deleted>>

b. The PCB assembly shall be supported during handling and transportation in order to avoid any mechanical stress on the assembly or component damage.

NOTE Mechanical support can be provided by spacer and frame.

c. The PCB shall not be forced during integration to compensate warp and twist.

NOTE Shims or spacers can be used to accommodate warp and twist during integration.

13.6 Inspection records

a. The result of the final inspection shall be recorded on the shop traveller.

14
Verification procedure

14.1 General

a. The supplier shall establish a verification programme in accordance with the DRD from Annex G for approval by the Approval Authority.

NOTE Requirement G.2.1b gives possibility to tailor verification programme.

b. The supplier shall demonstrate verification for each combination of substrate material, PCB footprint, SMD type, soldering technique applied, stacking and bonding, lead forming configuration, , solder mask and conformal coating as used on FM.

NOTE Substrate materials are defined in Table 6-1 of ECSS-Q-ST-70-12.

c. <<deleted>>

d. <<deleted>>

e. <<deleted>>

f. The verification shall be performed on at least three devices except for the sensitive devices where five parts are used per configuration in the verification programme.

NOTE 1 For the devices listed in the ESCIES sensitive list that have not been demonstrated to be none sensitive by the supplier the first verification test plan is with five devices.

NOTE 2 Machine reflow, hand soldering are examples of different assembly methods.

g. The supplier's repair process including removing and replacing of one of each type of mounted device shall be submitted to verification testing.

NOTE 1 Verification of the number of repairs as permitted in ECSS-Q-ST-70-28.

NOTE 2 The supplier has the option to perform more than one repair for each type of device.

h. <<deleted>>

i. <<deleted>>

j. <<deleted>>

k. Verification testing of commercial devices shall be performed for each lot in conformance with this clause.

l. A repair, not included in ECSS-Q-ST-70-28, shall be submitted to a verification programme.

m. Verification of the assembly shall be performed with a nominal method and a repair method for each device.

NOTE Standard manual method can cover a range of processes in addition to hand soldering e.g. hot gas station, IR station.

n. Collective assembled devices shall not be reworked neither repaired.

o. The PCB verification test vehicle shall be representative of the FM footprint configuration and connections of the hardware.

p. Terminations to be microsectioned shall be connected to the internal PCB layers.

NOTE The terminations to be microsectioned are described in Table 14-2.

q. The verification of area array devices shall meet the requirements of clause 14.9.

r. For each type of device, the repair shall be performed on the largest device.

s. The repair shall be performed only on the devices being assembled by standard manual method.

NOTE No repair verification is needed on the devices being assembled by machine method as this is covered under the standard manual soldering verification method.

t. The supplier shall maintain a list of sensitive devices.

u. Sensitive devices shall be submitted to re-verification every four years to monitor the stability of the assembly.

v. The re-verification of sensitive devices specified in the requirement 14.1u may be performed on limited verification programme performed on worst case configuration identified during initial verification.

NOTE 1 One substrate, one package per device type, three samples per device.

NOTE 2 For leadless devices, mechanical testing can be omitted.

NOTE 3 Non-destructive characterization can be proposed as alternative to microsection.

w. The verification sample shall be submitted to two nominal soldering method reflows when reflow is performed on the both PCB sides of the FM.

NOTE The supplier has the option to flip the board for the second reflow to demonstrate the flight configuration.

x. The device type classification shall be in accordance with Table 14-1.

Table 14-1: Device type classification

Device type	Classification
Rectangular and square end-capped or end-metallized device with rectangular body	Leadless chip
Cylindrical and square end-capped devices with cylindrical body	Leadless chip
Bottom terminated chip device	Leadless
Castellated chip carrier device	Leadless
Flat pack and Gull-wing leaded device with round, rectangular, ribbon leads	Leaded
Moulded magnetics	Leaded
"J" leaded device	Leaded
Area array devices	AAD
Devices with ribbon terminals without stress relief (flat lug leads)	Leaded
Device with Inward formed L-shaped leads	Leaded
Stacked modules devices with leads protruding vertically from bottom	Leaded
Leaded device with plane termination	Leaded

14.2 Verification by similarity

a. <<deleted>>

b. <<deleted>>

c. <<deleted>>

d. <<deleted>>

e. <<deleted>>

f. <<deleted>>

g. <<deleted>>

h. <<deleted>>

i. <<deleted>>

j. <<deleted>>

k. <<deleted>>

14.2.1 General

a. A package shall be identified as the same family in case the following conditions are met:

1. the lead pitch, nominal thickness, nominal width and materials composition are identical,
2. the coated lead finishes on the termination are identical,
3. the bending dimensions and shape are identical,

4. the packages are constructed from the same materials.

NOTE 1 Glass to metal sealed, glass sealed side-brazed, top-brazed, and bottom-brazed packages are different families.

NOTE 2 Dual side pin arrangements are different to quad side pin families.

b. For flat pack, verification by similarity may apply even if the lead materials are different.

14.2.2 Conditions for similarity

a. Verification by similarity shall not apply to commercial devices.

b. Verification by similarity shall not apply to castellated devices.

NOTE Some resistors networks and LCCs are castellated devices examples

c. Verification by similarity for leadless chip devices shall not be declared successful until the following conditions are met:

1. the device size length is between Lmin and Lmax and the device size width is between Wmin and Wmax of the ones of the verified component,
2. the device is thinner than the maximum height verified,
3. the ceramic material type is identical,
4. the metallization of the termination and the barrier layers on devices is identical,
5. the device manufacturer is identical.

NOTE 1 for item 1: for example, 0402 – 2220 does not qualify 1825 as the width is outside the max 20 verified.

NOTE 2 for item 2: ceramic chip capacitors can be very sensitive to mounting conditions. Generally, type 1 chip capacitors show less sensitivity to mounting constraints than Barium Titanate based type 2 chip capacitors. This sensitivity is design and process related and can therefore vary from one manufacturer to another. Within a manufacture type 2 range, one or more ceramic material can be used but one can say that generally the highest end of the capacitance ranges is the most sensitive to mounting conditions. In order to increase capacitance value for a given chip format with a specified maximum chip thickness, manufacturers increase the number of dielectric layers, thus increasing the volume ratio between electrode material and ceramic, which

is not favourable in terms of sensitivity to mounting constraints.

NOTE 3 for item 2: it is therefore impossible to apply similarity rules between type 1 and type 2 ceramic chip capacitors as well as between different manufacturers. It is also good practice to select in priority the highest capacitance values in a class or type 1 or type 2 ceramic capacitors range to be submitted to assembly verification.

NOTE 4 for item 3: type refers only to type 1 or type 2 capacitor.

d. Verification by similarity for leaded devices, cylindrical or square end-capped devices with cylindrical body and device with inward formed L-shaped leads shall be valid in case the following conditions are met:

1. the devices are from the same family in conformance with the requirements from the clause 14.2.1,
2. devices are smaller than the verified Lmax and Wmax,
3. demonstration that small package is not damaged during the placement on PCB.

NOTE The dimension L is the distance between the outermost leads of the device and W is the device width.

e. Verification by similarity for leadless device with thermal plane termination shall be valid in case the following conditions are met:

1. smaller than the verified Lmax and Wmax,
2. the construction of the device is identical to that verified,
3. the materials are identical.

NOTE The outline dimensions of the device are length, L and width W.

f. Verification by similarity for area array devices shall be valid in case the following conditions are met:

1. lower number of columns,
2. the same pitch,
3. same column dimensions,
4. same columns distribution,
5. same column materials,
6. same column construction,
7. same column manufacturer,
8. same column assembly process,
9. lower mass,
10. same material and same package construction,

11. same shape.

14.3 Verification programme

a. The verification programme as shown in Figure 14-1 shall consist of:

1. Visual inspection in conformance with clause 13.
2. Vibration and shock testing in conformance with clause 14.5.
3. Temperature cycling in conformance with clause 14.6 except for area array devices .
4. Microsectioning in conformance with clause 14.7.
5. For area array devices, temperature cycling in conformance with requirements from clause 14.9.
6. Cleanliness in conformance with requirement 14.14b.

NOTE 1 Note to item 2: Mechanical testing according to this standard gives an indication of the reliability of the product in actual applications. It is unlikely that the test vehicle represents every flight configuration (size of the board, damping of the board, stiffening of board, number of board layers). The deflections, amplitudes, transmissibilities, radii of curvature experienced by SMDs under shock and vibration are totally dependent on the board to which they are mounted. Because each space project has its own unique shock and vibration requirements it is impossible to determine appropriate test levels without testing actual electronic boxes.

NOTE 2 Note to item 3: Temperature cycling is performed to ensure that the SMDs, substrates, solder alloys and associated stacking compounds and conformal coatings are suitable for the operational lifetime of the spacecraft.

b. The supplier shall present a verification programme for approval.

NOTE Owing to the different modes of failure resulting from vibration and temperature cycling, the supplier can use any sequence of environmental testing.

c. Removal and replacement shall be verified on the repair assembly method.

d. When mechanical bonding is underneath the device, microsectioning of one device may be performed after vibration and 50 thermal cycles to justify the integrity of the bonding.

NOTE The device can be one of the three assembled devices.

e. The devices used for the verification shall be in compliance with list of devices from the Table H-1.

NOTE It is under the responsibility of the company to ensure that the soldering method and temperature is compliant with the manufacturer datasheet and or technical notes.

f. The devices soldered by collective process shall not be reworked.

g. Reworking of collective assembled solder joint shall be decided during the MIP1 in compliance with Figure 14-1.

h. The environmental conditions of the mission including ground testing shall be reviewed to ensure the verification programme envelops the mission conditions.

i. Supplier shall ensure that the conditions associated with long term storage, extensive ground testing, mechanical stress after launch, high temperature application with or without thermal cycles are assessed.

j. The supplier shall organise a Verification review (VR) with the Approval Authority during which Verification programme is reviewed and approved.

NOTE The PCB design is reviewed to ensure compliance with requirements from clause 14.1.

k. Prior to start of verification assembly the supplier shall organise a Manufacturing readiness review (MRR) with the Approval Authority.

NOTE During the review, the Approval Authority can check that the verification programme is approved by all parties and that all open actions are closed.

l. The supplier shall organise a Mandatory inspection point (MIP1) with the Approval Authority prior to any conformal coating with five days notification.

NOTE The Approval Authority can delegate the MIP1 to the supplier.

m. Prior to any environmental testing the supplier shall organise with the Approval Authority an action review during which the MIP and outstanding actions are reviewed, with five days notification.

NOTE The Approval Authority can delegate the action review to the supplier.

n. The supplier shall organise with Approval Authority a Mandatory Inspection Point (MIP2) at the completion of the environmental test with five days notification.

NOTE The Approval Authority can delegate the MIP2 to the supplier.

o. The supplier shall organize with the Approval Authority a Test review board (TRB) during which the environmental tests results are reviewed.

NOTE The Approval Authority may delegate the TRB to the supplier.

p. The supplier shall organise with the Approval Authority a final verification review in conformance with requirements from clause 14.15.5.

NOTE The Assembly processes can be reviewed during the meeting in order to have the PID issued. Verification of closure of the actions identified during the audit of the manufacturing line.

q. Any nonconformance or major change with reference to the verification plan shall be notified to the Approval Authority within one week.

r. NRBs shall be organised by the supplier.

s. The schedule of the verification activities shall be provided and maintained.

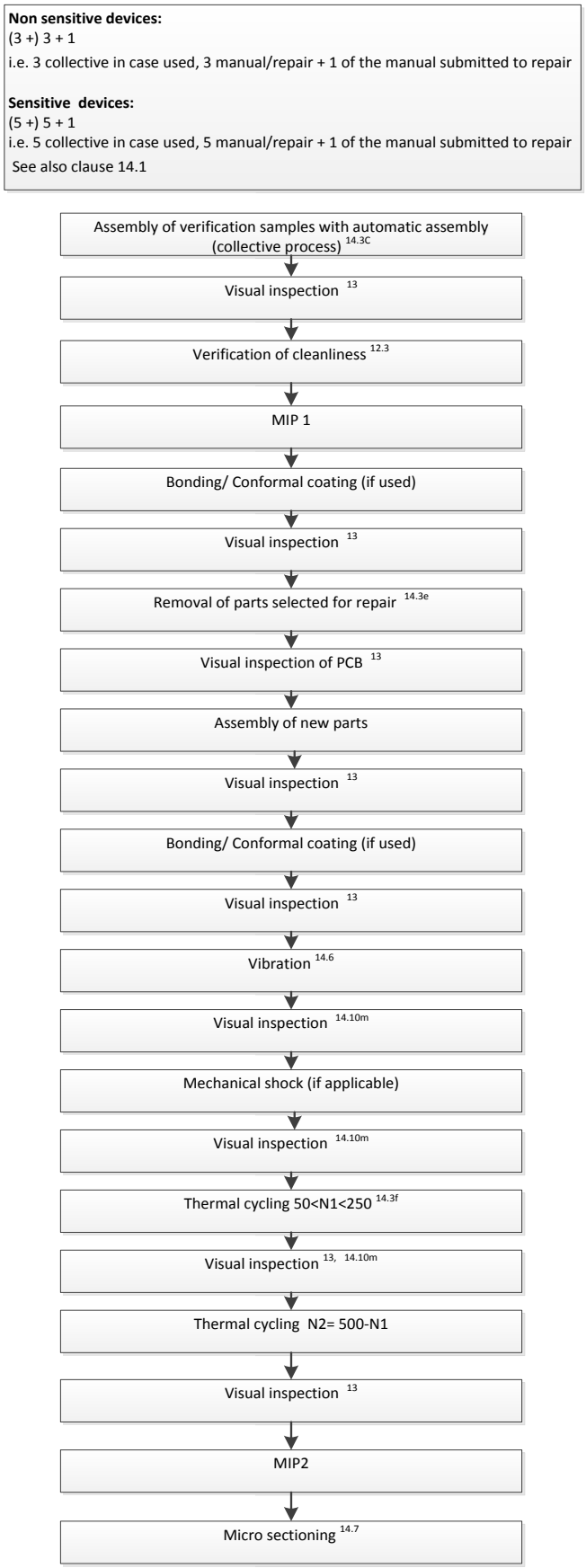


Figure 14-1: Verification programme flow chart (standard flow)

14.4 Electrical testing of devices

a. <<deleted>>

14.4.1 General

a. Except the cases specified in the requirements 14.4.1b and 14.4.1c, the supplier may propose electrical monitoring as an alternative method, for each assembly configuration, including the repair assembly method, to achieve verification providing the following conditions are met:

   1. one device for initial microsectioning except the case for sensitive and leadless devices,
   2. for sensitive devices, a minimum of five devices to be assembled,
   3. minimum number of 32 devices for electrical monitoring,
   4. all solder terminations are continuously electrically monitored throughout the temperature cycling,
   5. minimum of 1500 thermal cycles in accordance with requirements from the clause 14.6,
   6. the number of completed cycles for each failed device is recorded.

b. Electrical monitoring shall be performed for ceramic hermetic area array devices in conformance with requirements in clause 14.9.

c. Capacitors and "SMD – xx" devices shall be excluded from electrical monitoring.

   NOTE Capacitor and "SMD–xx" devices such SMD05, SMD1, SMD2 and SMD5C are excluded as the failure mechanism is crack in ceramic.

d. First failure in case number of cycles < 1500 shall be identified as the device assembly verification limitation.

e. Any failed device shall be subjected to failure analysis.

f. The electrical value of devices shall be selected to ensure detection of anomaly in the solder joint.

   1. for resistors zero ohm or the lowest value in the procurement specification,
   2. for other types, custom daisy chain.

g. During thermal cycling, a drift of less than 10 % of resistance shall be accepted when the electrical monitoring is performed and referenced to the first five cycles recorded values.

   NOTE Depending on application the acceptable drift of resistance can be adapted.

h. For each assembly method and type of devices at least 32 devices shall be assembled for electrical monitoring.

   NOTE 1 Machine reflow, hand soldering are the examples of assembly method.

NOTE 2 The assembly of the capability and the electrical verification samples can be made on the same board.

i. If capability and electrical monitoring samples are on the same board they shall be separated before the microsectioning of the capability samples and before the environmental tests for the electrical verification samples.

NOTE Illustration is given in the flow diagram of Figure 14-2.

j. Capability samples may be excluded from the programme if it can be demonstrated through previous verification heritage.

k. Microsectioning shall be performed in accordance with requirements from clause 14.7.

l. Vibration and shock testing shall be performed in conformance with requirements from clause 14.5.

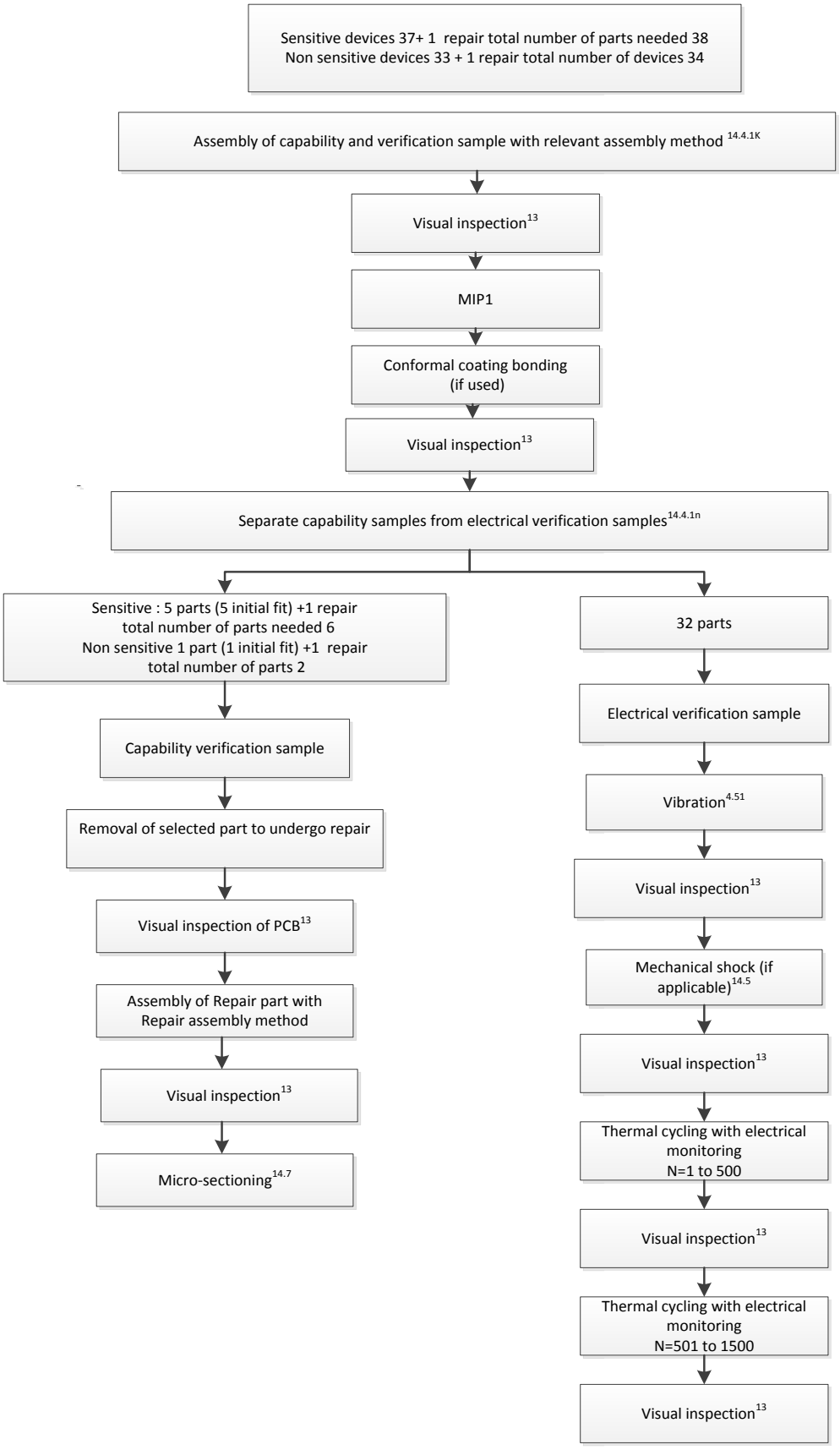


Figure 14-2: Verification programme flow chart (electrical testing)

14.5 Vibration and shock

a. Requirements from clause 13.2 from ECSS-Q-ST-70-08 shall apply for "Vibration".

b. For area array devices, the shock levels shall be set to meet the intended mission with margin, except the case specified in the requirement 14.5c.

c. For area array devices shock may be omitted when the mechanical design can demonstrate robust margin.

NOTE The use of dedicated mechanical stiffener is an example of such design.

d. For shock, sensitive devices shock testing shall be added to the verification programme flow.

NOTE Examples of shock sensitive devices can be found in ECSS-E-HB-32-25.

e. When shock testing is required as defined in 14.5d then the shock levels shall be set to meet the intended mission with margin.

f. The levels and duration of the vibration shall be provided.

NOTE It is the responsibility of the contractor to ensure that the levels applied are sufficient to cover the mission.

g. The levels and duration of the shock shall be provided by supplier.

h. The mounting configuration of the PCB for the vibration tests shall be identified.

i. The PCB shall be mounted such that the deflection and acceleration is representative of the FM.

j. The accelerometers shall be placed on the PCB as well as on the base plate in order to determine the acceleration of the PCB.

14.6 Temperature cycling test

a. Requirements from clause 13.3 of ECSS-Q-ST-70-08 “Temperature cycling test” shall apply for the thermal profile.

b. The total number of temperature cycles shall be 500, except for area array devices and devices verified by electrical monitoring when clause 14.9 and 14.4 is applicable.

c. The monitoring temperature sensor shall be attached to the surface of the printed circuit board.

d. <<deleted>>

e. Compliance from -55 °C to +85 °C for mission shall be stated.

14.7 Microsection

a. <<deleted, modified and moved to 14.7.2>>

b. <<deleted, modified and moved to 14.7.2>>

c. <<deleted>>

d. <<deleted, modified and moved to 14.7.2>>

e. <<deleted, modified and moved to 14.7.2>>

14.7.1 Microsection facilities

a. Approval Authority should make available the list of laboratories to perform microsection.

NOTE The list of available laboratories is on ESCIES website.

b. Microsections shall be performed by a laboratory specified in 14.7.1a except the case specified in the requirement 14.7.1c.

c. When in-house or other non-listed microsection facilities are used, the company shall demonstrate the following:

1. the laboratory capability on a representative sample without conformal coating is provided,
2. a report with associated microsections is sent to the Approval Authority for review and assessment of quality of microsectioning,
3. representative samples include chip devices, LCCs and FPs.

14.7.2 Microsectioning

a. Microsections shall be performed in compliance with the Table 14-2.

b. The microsection shall be inspected with a magnification of 50 to 200 times except the case specified in the requirement 14.7.2m.

c. At least one microsection shall be made per assembly configuration after environmental testing on each type of device, size and assembly processes and soldering processes.

NOTE Successive polishing planes can be performed.

d. Additional microsections may be requested in case of cracks or other features detected during the first microsection sample or by request from the Approval Authority.

e. The microsection shall be done on the device having the worst solder joint appearance as identified at MIP2.

f. In case the microsection shows a crack more than 75% of acceptable crack, a second device shall be microsectioned.

g. In case the second microsection shows a crack more than 75% of acceptable crack a third device shall be microsectioned.

h. In case the third microsection shows a more than 75% of acceptable crack device shall be classified as sensitive.

i. For sensitive devices five devices shall be microsectioned per assembly configuration.

j. Number of microsections as specified in requirement 14.7.2i may be reduced based on Approval Authority agreement.

k. The integrity of the assembly shall be assessed by microsectioning.

NOTE Integrity covers PCB, solder joints, adhesives, packages.

l. Adhesive for thermal or mechanical purpose underneath a device shall be microsectioned.

m. The microsection for devices with small stand-off should be inspected with magnification up to 500 times.

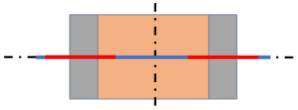
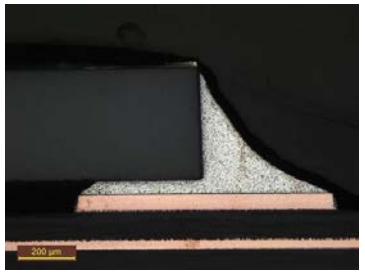
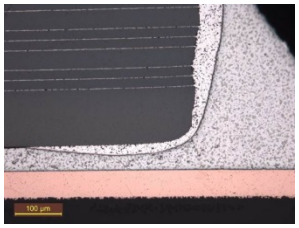
NOTE Examples of small stand-off devices are LCCs, chip resistors.

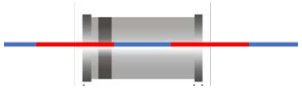
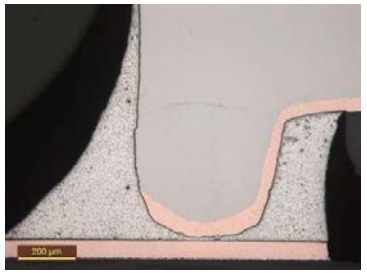
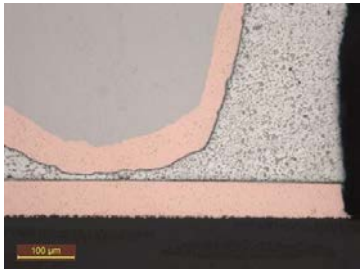
n. The Approval Authority shall have access to the moulded microsection and pictures.

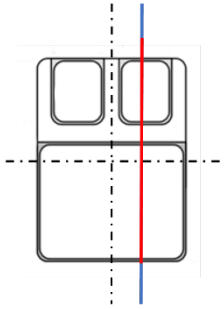
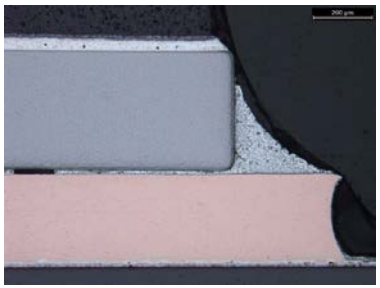
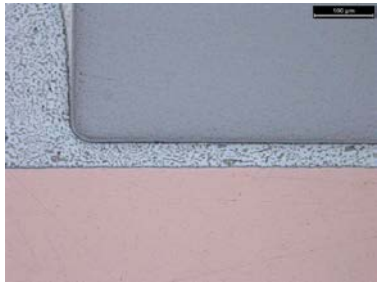
o. The microsections and other devices shall be stored for a period of at least 10 years.

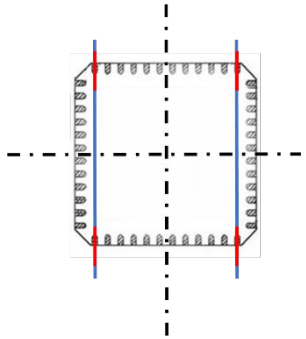
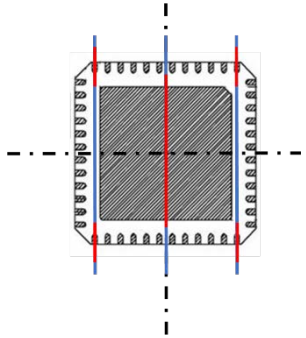
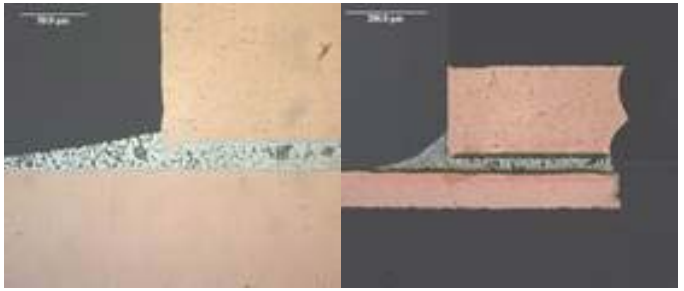
NOTE Stored samples can assist the analysis of in-service failures.

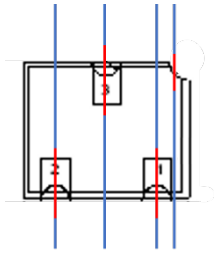
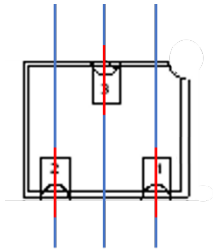
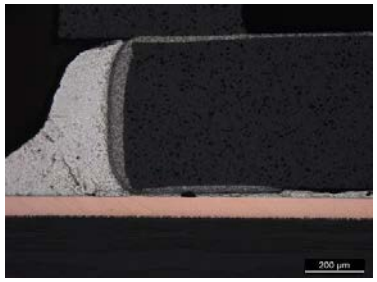
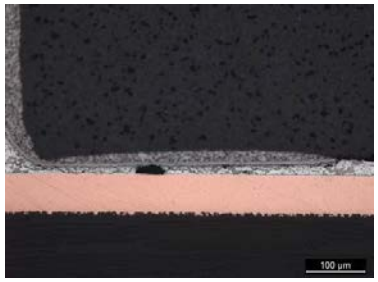
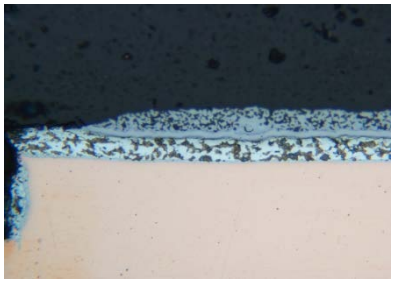
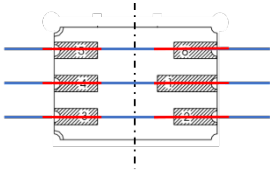
Table 14-2: Device microsection location

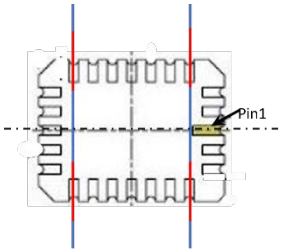
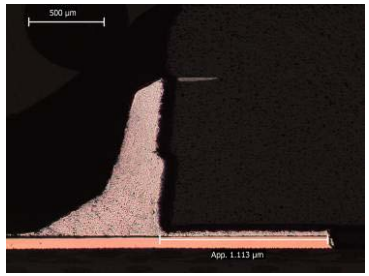
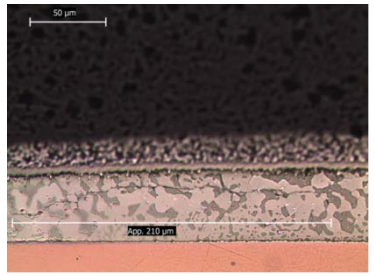
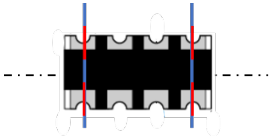
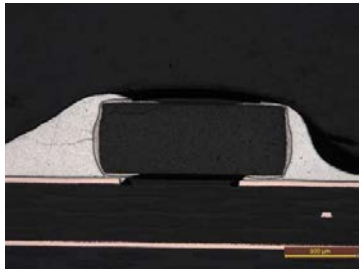
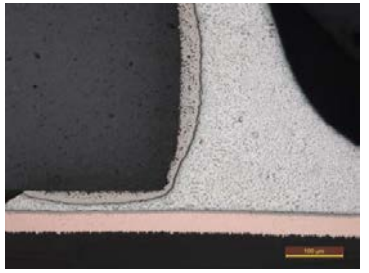
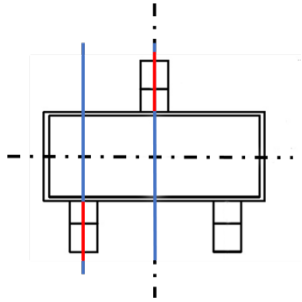
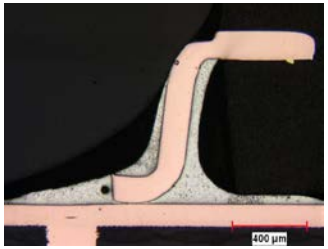
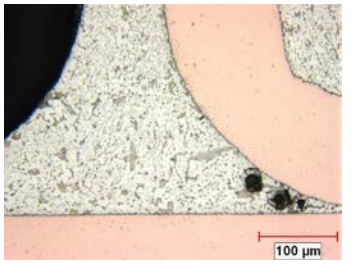
SMD type	Example device	Cross section planes	Example of views at min and max magnification
		Terminal to cross section Symmetry axis Cross section plane	
Rectangular and square end-capped or end-metallized device with rectangular body	chip resistors		 x50  x200
	chip capacitors		 x50  x200

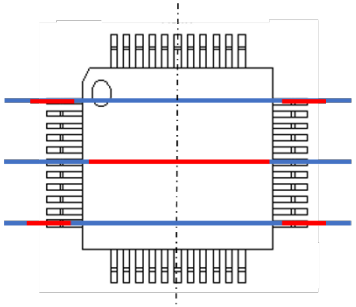
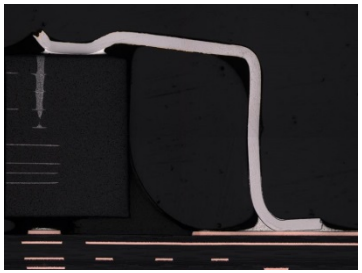
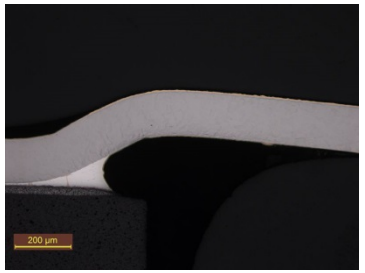
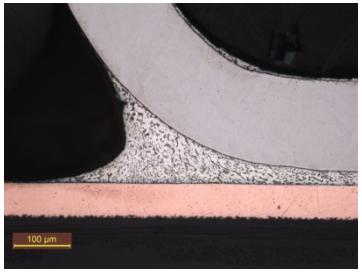
SMD type	Example device	Cross section planes	Example of views at min and max magnification
		Terminal to cross section Symmetry axis Cross section plane	
Cylindrical and square end-capped devices with cylindrical body	MELF		 x50  x100  x200

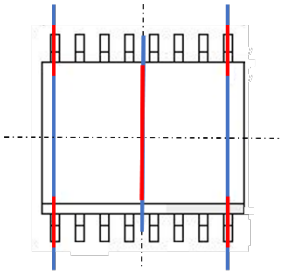
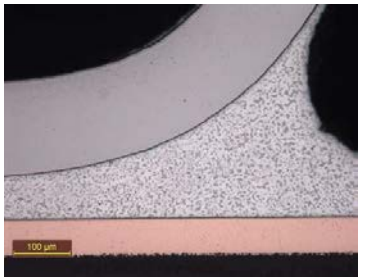
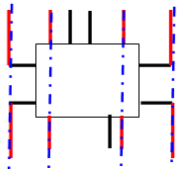
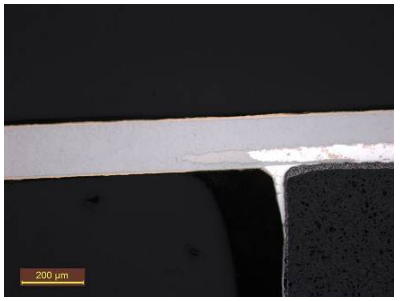
SMD type	Example device	Cross section planes	Example of views at min and max magnification
		Terminal to cross section Symmetry axis Cross section plane	
Bottom terminated chip device	SMD0.5, SMD1, SMD2, SMD0.2, SMD0.22	 + X Ray	  x25 x50   x100 x200 To check absence of cracks in the ceramic by visual inspection

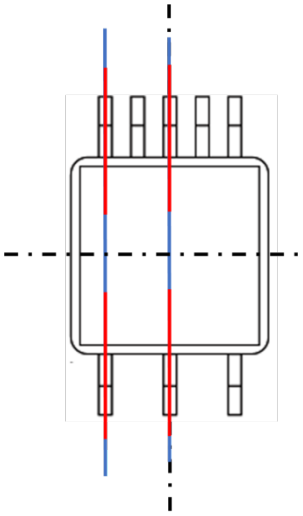
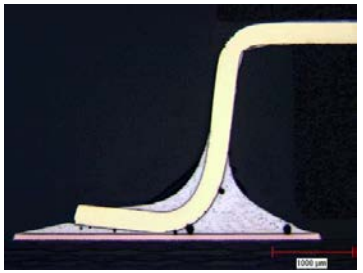
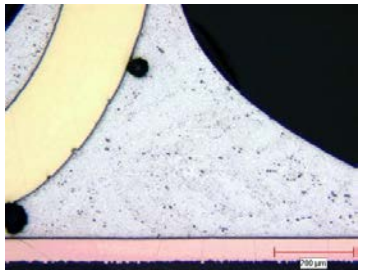
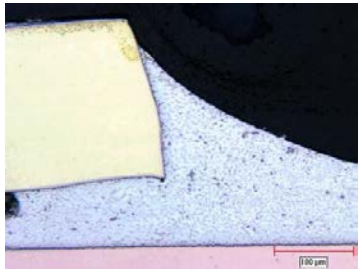
SMD type	Example device	Cross section planes	Example of views at min and max magnification
		Terminal to cross section Symmetry axis Cross section plane	
Bottom terminated chip device	Quad Flat Pack No lead (QFN)	 When thermal plane is present, the third microsection is in the middle axis: 	

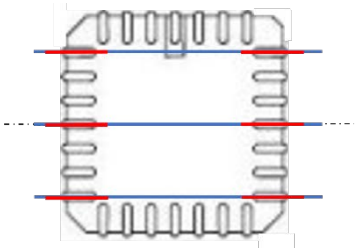
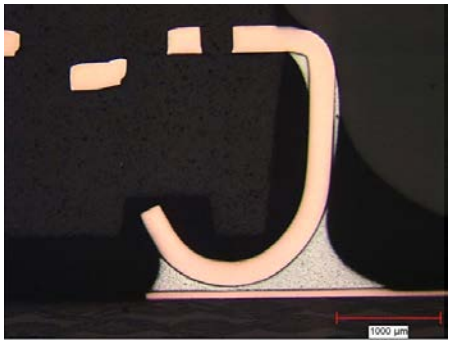
SMD type	Example device	Cross section planes	Example of views at min and max magnification
		Terminal to cross section Symmetry axis Cross section plane	
Castellated chip carrier device The main device of this type is leadless ceramic chip carrier (LCCC)	LCC3	 With ground connection (microsection to be done in the middle of castellation)  Without ground connection	 x100  x200  x400
	LCC6		

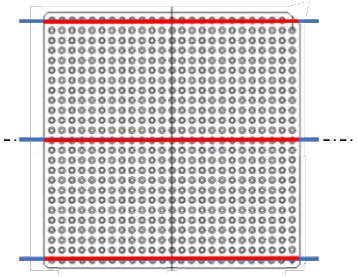
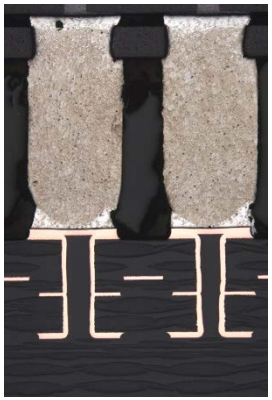
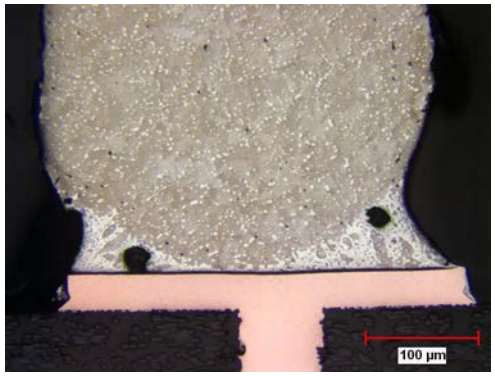
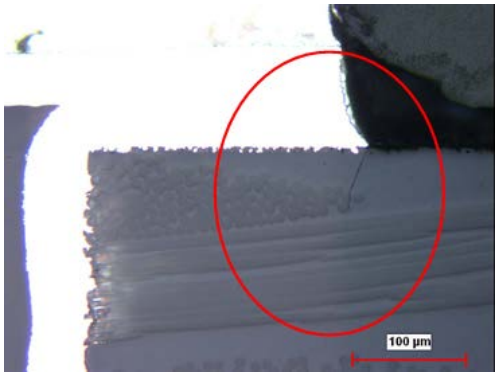
SMD type	Example device	Cross section planes	Example of views at min and max magnification
		Terminal to cross section Symmetry axis Cross section plane	
	LCC with termination on 4 faces		 x100  x500
	Resistor array		 x20  x100
Flat pack and Gull-wing leaded device with round, rectangular , ribbon leads	SOT23		 x50  x200

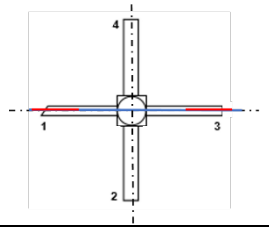
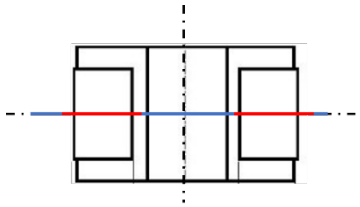
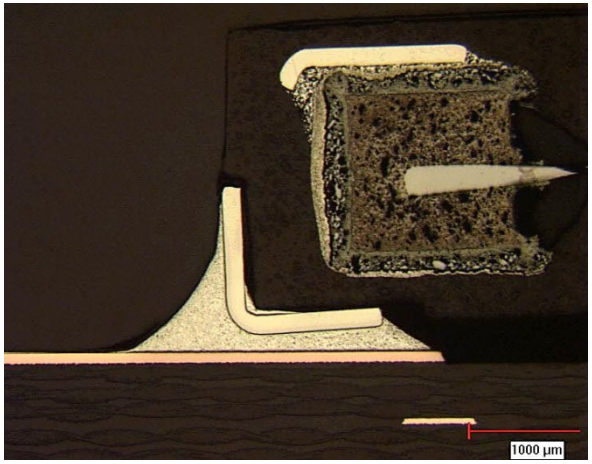
SMD type	Example device	Cross section planes	Example of views at min and max magnification
		Terminal to cross section Symmetry axis Cross section plane	
	CQFP + MQFP	 Centre micro-section to be done only when device is bonded.	  x50 x100  x200 Similar magnification to be applied for the assessment of the bonding lines.

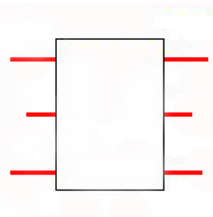
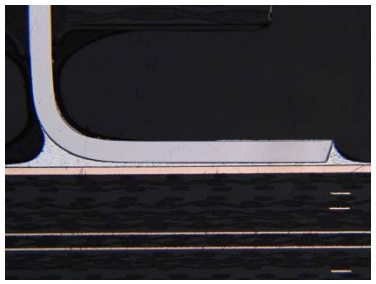
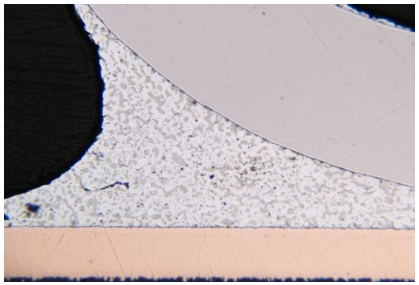
SMD type	Example device	Cross section planes	Example of views at min and max magnification
		Terminal to cross section Symmetry axis Cross section plane	
	FP, SO, SOIC	 Centre micro-section to be done only when device is bonded.	  x50 x200
	FP with spider leads		 x200

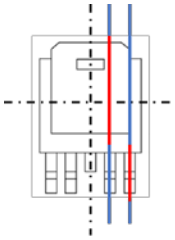
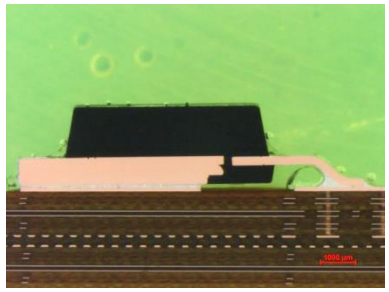
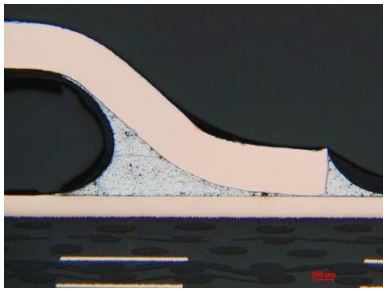
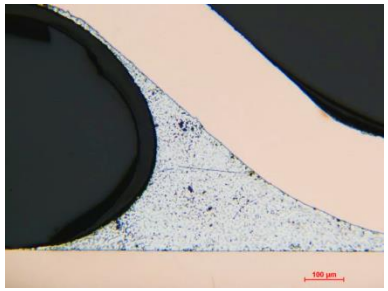
SMD type	Example device	Cross section planes	Example of views at min and max magnification
		Terminal to cross section Symmetry axis Cross section plane	
Moulded magnetics	1553 interface transformers or specific transformers	 Microsection plane in one edge. Additional microsection depending on lead configuration (different dimensions or shape)	 x25  x100  x200

SMD type	Example device	Cross section planes	Example of views at min and max magnification
		Terminal to cross section Symmetry axis Cross section plane	
"J" leaded device	ceramic leaded chip carriers (CLCC) and plastic leaded chip carriers (PLCC)		

SMD type	Example device	Cross section planes	Example of views at min and max magnification
		Terminal to cross section Symmetry axis Cross section plane	
Area Array devices (Capability Phase only)	CCGA		 x25  x100  x200 Presence of cracks in the laminate under investigation

SMD type	Example device	Cross section planes	Example of views at min and max magnification
		Terminal to cross section Symmetry axis Cross section plane	
Devices with ribbon terminals without stress relief (flat lug leads)			
Device with Inward formed L-shaped leads	Tantalum chip capacitor		

SMD type	Example device	Cross section planes	Example of views at min and max magnification
		Terminal to cross section Symmetry axis Cross section plane	
Stacked modules devices with leads protruding vertically from bottom		 Can be reduced when package is less than 50 leads	 x25  x200

SMD type	Example device	Cross section planes	Example of views at min and max magnification
		Terminal to cross section Symmetry axis Cross section plane	
Leaded device with plane termination	DPAK/TO252 D2 PAK SOT 223	 X Ray+ micro section (lead + plane) Microsection plane in one edge. Additional microsection depending on lead configuration (different dimensions or shape)	 x20  x100  x200

14.8 <<deleted>>

a. <<deleted>>

b. <<deleted>>

14.9 Special verification testing for hermetic ceramic area array packages

14.9.1 <<deleted>>

<<deleted>>

14.9.2 <<deleted>>

a. <<deleted>>

b. <<deleted>>

c. <<deleted>>

d. <<deleted>>

e. <<deleted>>

14.9.3 General

a. The assembly verification of hermetic ceramic AADs shall be divided in the following two parts, as shown in Figure 14-3.

1. electrical monitoring, and
2. demonstration of capability.

NOTE 1 The purpose of the capability samples is to show that the PCB integrity and the device are intact after the assembly and repair of AAD and environmental testing (vibration, mechanical shock and 500 temperature cycles). A crack in the columns or balls is not considered as reason for rejection.

NOTE 2 Once the capability samples show a satisfactory result the verification of AAD can commence.

NOTE 3 Capability samples can be excluded from the programme if the supplier can demonstrate through previous verification heritage.

b. When nominal and repair processes are identical then total number of parts during verification may be reduced to five with three assembled and two repairs among the three assembled.

c. The verification shall be performed with daisy chain devices to demonstrate a reliable electrical function of the PCB and the package interface throughout the environmental test campaign.

NOTE Environmental test campaign to include vibration, mechanical shock and 1500 temperature cycles.

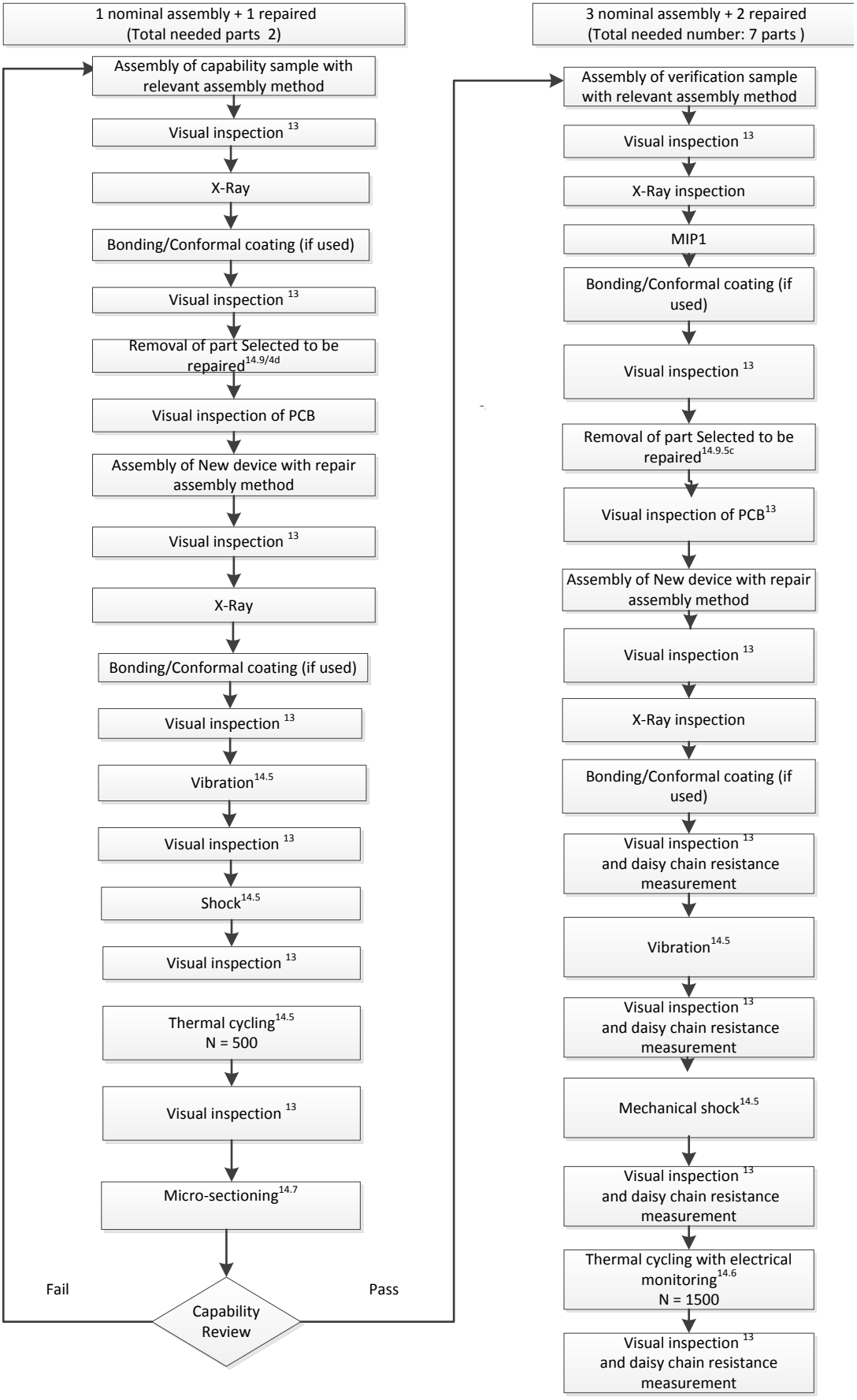


Figure 14-3: Verification programme flow chart (AAD)

14.9.4 Evaluation of capability samples

a. The supplier shall manufacture and demonstrate that the two capability samples are in conformance with the requirement 14.9.4i before the manufacture of the verification samples using daisy chain devices can be initiated.

b. The PCB material, PCB build-up, foot print and devices used as capability samples shall be representative for the FM of the hardware.

c. One device shall be assembled in the relevant reflow process.

NOTE The supplier can use daisy chain packages for the capability assessment with or without electrical monitoring.

d. The device shall be removed and replaced with a new device using the repair process.

e. The device shall be inspected in conformance with requirements from the clause 11.5.8.

f. The device shall be submitted to vibration testing in conformance with requirements from the clause 13.2 of ECSS-Q-ST-70-08.

g. The device shall be submitted to three mechanical shock axes in conformance with requirements 14.5b and 14.5c.

h. The device shall be submitted to 500 thermal cycles in conformance with requirements from the clause 13.3 of ECSS-Q-ST-70-08.

i. After environmental tests completion, microsectioning of the device shall be performed to demonstrate PCB integrity in the AAD area with respect to:

1. ECSS-Q-ST-70-10,
2. Damage to the device outside the procurement specification,
3. Footprint lifts,
4. Cracks in laminate,
5. Cracks in via,
6. Cracks in track,
7. Delamination’s in the PCB,
8. Measling in the PCB,
9. Cracks in bonding if used.

14.9.5 Verification

a. The PCB material, PCB build-up, foot print and daisy chain devices used for the verification shall be representative for the FM of the hardware.

b. For each assembly method and mounting configuration five devices shall be assembled.

c. Two of the assembled devices shall be removed and replaced with a new device using the repair process.

d. The devices shall be inspected in conformance with requirements from the clause 11.5.8.

e. The five devices shall be submitted to vibration testing in conformance with requirements from the clause 13.2 of ECSS-Q-ST-70-08.

f. The five devices shall be submitted to three mechanical shock pulses in each direction in conformance with requirements 14.5b and 14.5c.

g. The five devices shall be submitted to 1500 thermal cycles with temperature conditions in conformance with requirements from the clause 13.2 of ECSS-Q-ST-70-08.

h. Resistance measurement should be done, at ambient, before and after any mechanical testing.

i. Electrical monitoring of the daisy chain shall be performed during the 1500 thermal cycling.

j. The electrical monitoring shall be continuous throughout all 1500 cycles.

k. The sampling time of the electrical measurement shall be maximum 10 s throughout the 1500 cycles.

NOTE Different electrical monitoring methods can be agreed with Approval Authority.

l. The maximum increase of each individual daisy chain resistance, across the entire temperature cycling range during 1500 thermal cycles, shall not be more than 10 % of initial resistance recorded during the first five cycles.

m. No interrupts in the electrical monitoring shall be detected throughout the thermal cycling.

NOTE The supplier can provide their own criteria for an electrical failure to Approval Authority for approval.

14.10 Verification acceptance and rejection criteria

a. <<deleted>>

b. In the case of visual failures, an analysis shall be performed to identify the cause: component or soldering process.

c. Microsections shall be made in compliance with requirements from clause 14.7.2.

d. Surface and internal cracks of the solder fillet critical zone, as specified in Table 14-3, shall be considered acceptable.

e. Cracks present outside the critical zone shall be considered acceptable.

f. <<deleted>>

g. <<deleted>>

h. The devices shall be in conformance with the assembly requirements of clause 11.5.

i. The devices shall be in conformance with the requirements of clause 13.2.

j. Any visual defects in conformance with requirements from clause 13.3 shall be defined as a failure.

k. Any damage to the device shall be identified as a verification failure.

l. Thermal and mechanical bonding shall not be cracked at the completion of the verification testing.

NOTE Cracks in the thermal bonding perpendicular to PCB can be accepted.

m. Cracks in the bonding used for mechanical purpose shall not be accepted unless the following conditions are met:

1. absence of cracks after vibration and completion of a minimum of 50 thermal cycles,

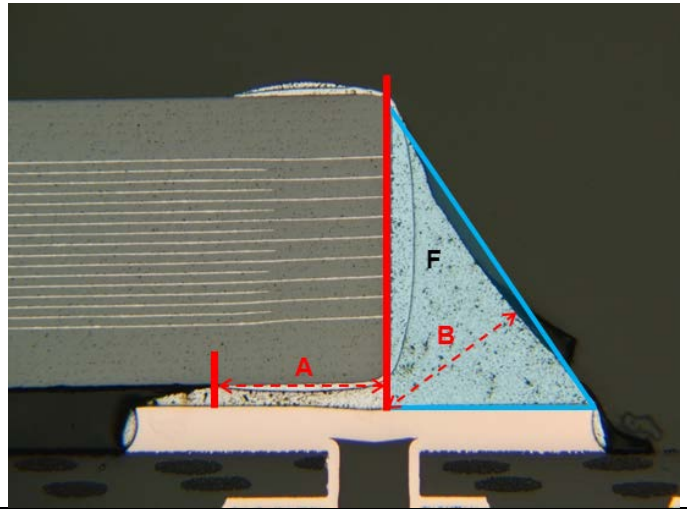
2. photos of microsections are provided in the verification report to demonstrate absence of cracks at 50 thermal cycles.

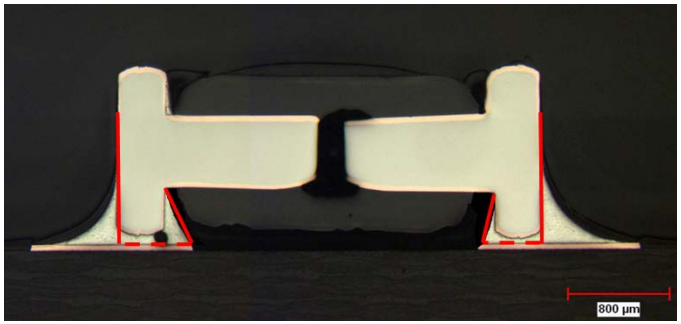
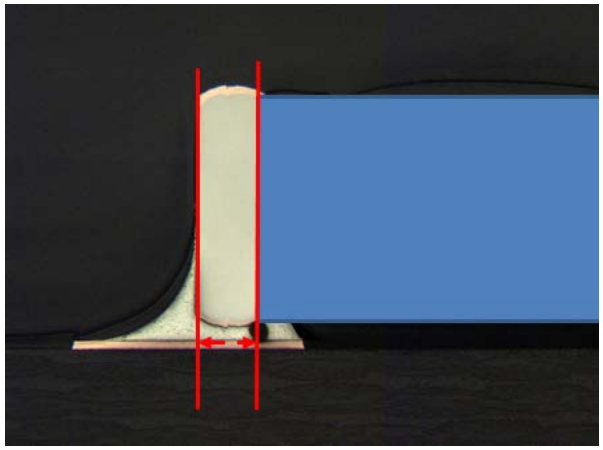
n. Acceptance and rejection criterion for PCBs shall be in compliance with clause 7.2 of ECSS-Q-ST-70-10.

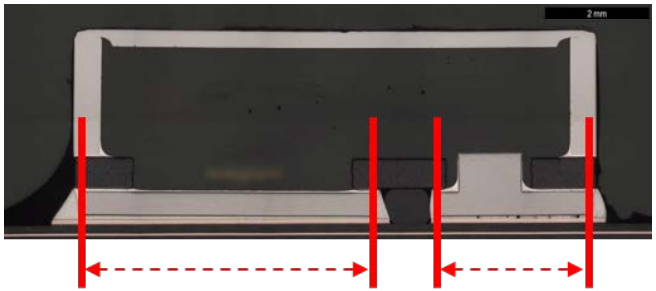
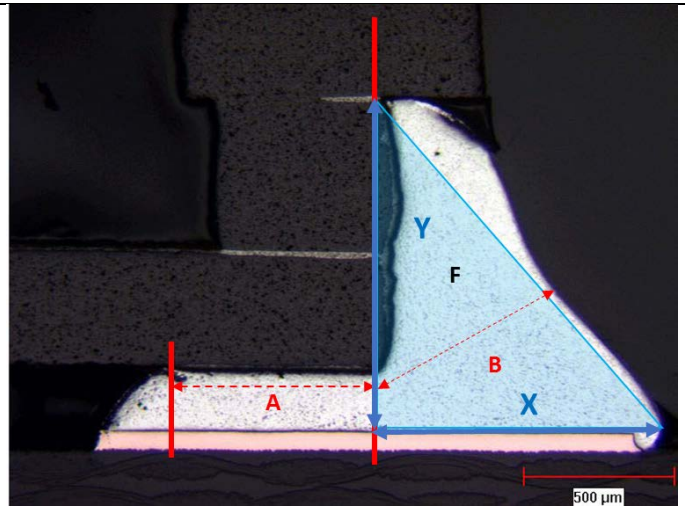
o. Defects, such as footprint lifting, cracks in laminate, cracks in via, cracks of tracks, PCB delamination shall be recorded as a nonconformance and analysed.

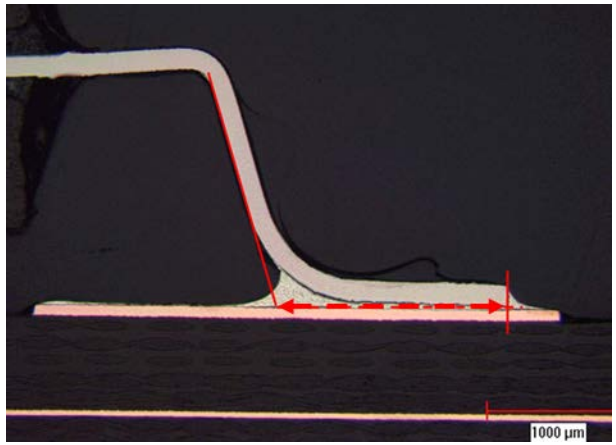
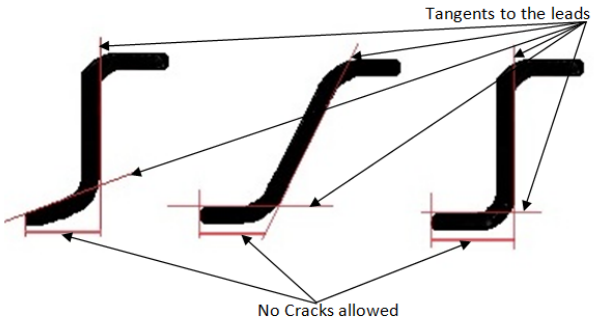
Figure 14-4: <<deleted>>

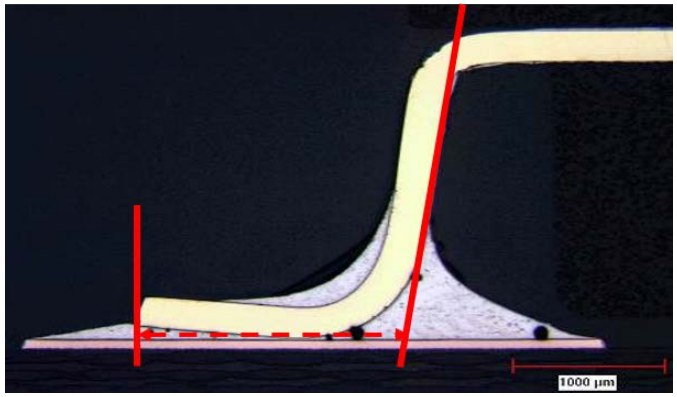
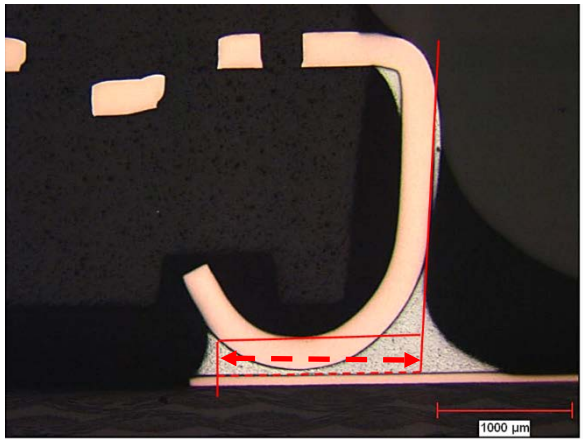
Table 14-3: Critical zone definition per device type and acceptance criteria

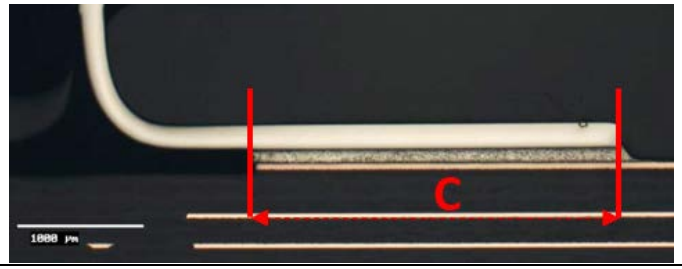
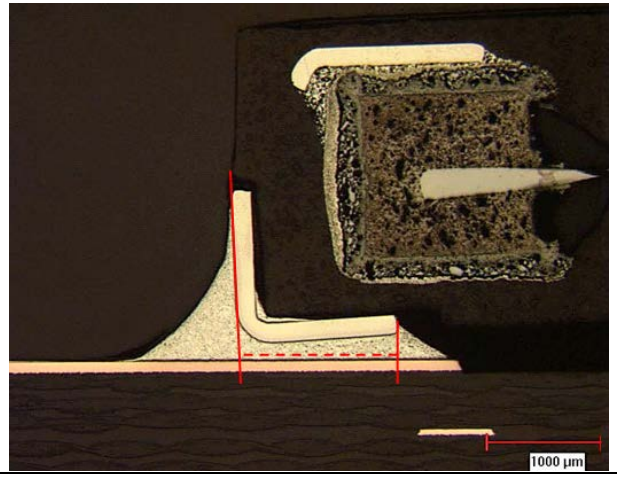
SMD type	Example device	Critical Zone definition	Acceptance criteria
Rectangular and square end-capped or end-metallized device with rectangular body	chip resistors chip capacitors		Crack length less than 60% of A+B, and no crack in fillet area F

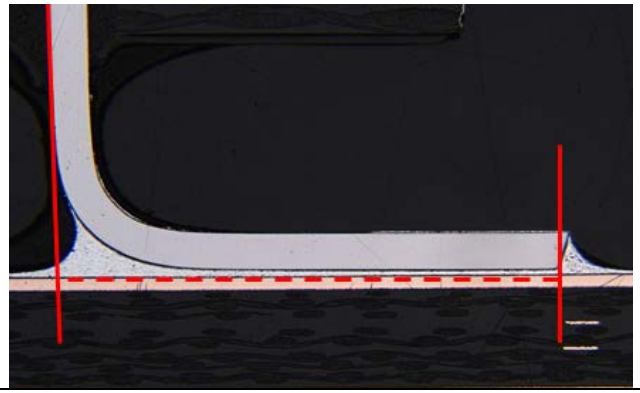
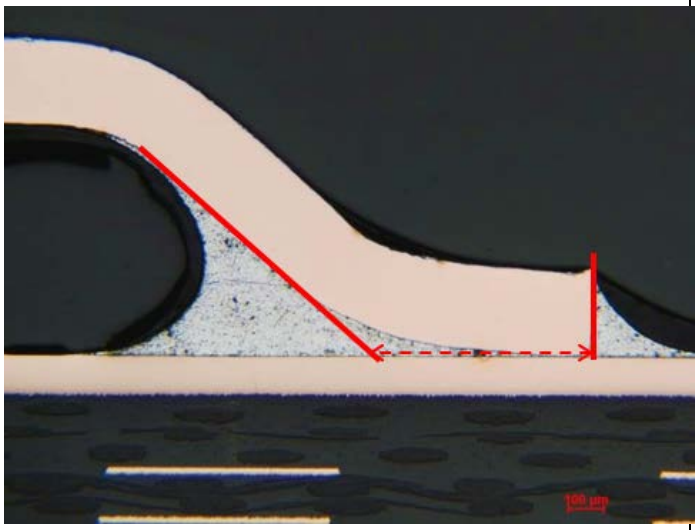
SMD type	Example device	Critical Zone definition	Acceptance criteria
Cylindrical and square end-capped devices with cylindrical body	MELF	  red line defines the critical zone ← - - →	Crack no longer than 33% of critical zone length

SMD type	Example device	Critical Zone definition	Acceptance criteria
Bottom terminated chip device	SMD0.5, SMD1, SMD2, SMD0.2, SMD0.22 Quad Flat Pack No lead (QFN)	 red line defines the critical zone	No crack longer than 25% of lap connection No cracks in the ceramic
Castellated chip carrier device The main device of this type is leadless ceramic chip carrier (LCCC)	LCCs		Crack length less than 70% of A+B and no crack in fillet area F (blue area) OR Crack less than A providing 100% coverage of castellation area with a convex solder joint, and solder wetting length on the solder footprint is more than castellation height + stand-off

SMD type	Example device	Critical Zone definition	Acceptance criteria
Flat pack and Gull-wing leaded device with round, rectangular , ribbon leads	SOT23 CQFP + MQFP FP, SO, SOIC FP with spider leads	 red line defines the critical zone ← - - →	Crack no longer than 33% of critical zone length
	Specific case: TSOP		For TSOP no crack allowed in the critical zone

SMD type	Example device	Critical Zone definition	Acceptance criteria
Moulded magnetics	1553 interface transformers or specific transformers	 red line defines the critical zone ← - - →	Crack no longer than 33% of critical zone length
"J" leaded device	ceramic leaded chip carriers (CLCC) and plastic leaded chip carriers (PLCC)	 red line defines the critical zone ← - - →	Crack no longer than 33% of critical zone length

SMD type	Example device	Critical Zone definition	Acceptance criteria
Devices with ribbon terminals without stress relief (flat lug leads)			Crack no longer than 33% of critical zone length C
Device with Inward formed L-shaped leads	Tantalum chip capacitor		Crack no longer than 33% of critical zone length

SMD type	Example device	Critical Zone definition	Acceptance criteria
Stacked modules devices with leads protruding vertically from bottom			Crack no longer than 33% of critical zone length OR For long leads (more 3 mm) crack no longer than 50% of critical area when 5 parts are microsectioned
Leaded device with plane termination	DPAK/TO252 D2 PAK SOT 223		Crack no longer than 33% of critical zone length Plane termination under X Ray inspection

14.11 Approval of verification

a. A letter confirming the completion of a successful verification programme shall be sent to the contact person of the supplier from the Approval Authority, with the SMT summary table specified in the DRD of Annex H attached to it.

NOTE 1 The letter and the SMT summary table provide evidence of the verification approval to a third party.

NOTE 2 The approval of verification applies to all space projects from the date of the approval until withdrawn.

NOTE 3 The SMT summary table is prepared by the supplier and sent to the Approval Authority for approval.

b. <<deleted>>

c. <<deleted>>

d. Reference to the SMT summary table number shall be made on each space project declared processes list .

NOTE See ECSS-Q-ST-70, Table C-2.

14.12 Withdrawal of approval status

a. The approval status of the supplier shall be withdrawn when any of the following status justify its withdrawal:

1. Repetitive supply problems and manufacturing defects.
2. Undeclared changes to the PID.
3. Continuous non-compliance with the PID.

14.13 Conditions for delta verification

a. The supplier shall undertake a verification for any new configuration not covered by similarity rules in accordance with requirements from clause 14.2.

b. The delta verification shall be performed when changes are undertaken as specified in Table 14-4.

c. For a process change verification programme based on assembly of already verified PCB materials, the choice of the PCB type or a sampling of several PCB types instead of all PCB materials may be selected, subject to agreement by Approval Authority.

NOTE 1 The selection criteria is based on worst cases depending on the change of process to be verified.

NOTE 2 Examples of worst cases are CTE mismatch, thermal dissipation, stiffness.

d. For delta-verification associated with process change the test vehicles shall be specified, in order to be representative of the process evolution.

e. The types and number of parts to be mounted on the test vehicles shall be specified as agreed by Approval Authority.

NOTE This allow to track any impact of the process evolution as defined in Table 14-4.

f. A delta-verification programme in accordance with the DRD from Annex G shall be submitted for approval to the Approval Authority.

g. Number of sensitive parts to be assembled and microsectioned shall be five.

h. Number of sensitive parts to be assembled and microsectioned may be reduced to three if the initial verification showed reproducible results.

NOTE Sensitive parts are from the ESCIES list and company PID.

i. Small size packages may be omitted from microsectioning providing that these package sizes are already in the company PID.

Table 14-4: Conditions invoking verification

Changes	Test vehicles without any test	Cleanliness tests (Ref 14.14)	Material compatibility with cleaning solvent	Test vehicles with tests according to Figure 14-1, Figure 14-2 or Figure 14-3
New device mounting configuration (example, already verified with conformal coating and now mounted without)				x
New SMD package size				X
New manufacturer of passive chips				X
New material of printed circuit board e.g. Epoxy, Polyimide, Aramid, mixed material build-up are different materials, PCB surface finish				X
New thermal and/or mechanical adhesive				X
New conformal coating				X
New solder paste with same alloy, same powder size distribution, same flux activation type	X +microsections[1]	X		
New solder paste with new alloy, flux activation type and/or different physical-chemical characteristics				X
New flux activation type for hand solder	X +microsections[1]	X		
New cleaning solvent and or new cleaning process		X	X	
New reflow profile, Peak temp +/-5°C, duration above liquidus [2]				X
New equipment to deposit soldering paste without change of process	X +microsections[1]			
New solder paste depositing process				X
New device placing equipment	X +microsections[1]			
New device placing equipment of same process method	Visual inspection only			
New type of reflow equipment with process change				X
New reflow equipment without process change	X +microsections[1]			
Move Manufacture location outside the clean room approved in the PID	X +microsections[1]			

[1] For microsection, one part per family type from the SMT summary table as per Annex H.

[2] The reflow profile is identical when the duration of the pre-heating, ramp of flux activation phase, peak temperature and time above solder liquidus, ramp of cooling phase can be repeated between different types of PCBs.

14.14 Verification of cleanliness

a. The verification of the PCB cleanliness shall be performed for the following cases:

   1. for the first verification programme performed by a company,

   2. when the conditions of Table 14-4 request it.

b. The cleanliness test of the board shall be conducted in accordance with requirements from the method 2.6.3.3 of IPC-TM-650 (2004).

14.15 Verification approval procedure

14.15.1 Request for verification

a. Verification approval procedure shall list the single point contact for all SMT matters.

b. RFA shall be issued.

c. The following items shall be submitted to the Approval Authority:

   1. A letter from the supplier signed by the contact person and the quality assurance organization of the supplier addressed to the Approval Authority, describing his experience in SMT and making the request for verification.

   2. One technology-sample of SMT taken from the assembly line, to be verified, not carrying conformal coating for the Approval Authority to inspect.

      NOTE Conformal coating to be omitted to enable detailed inspection to be undertaken by Approval Authority.

14.15.2 Technology sample

a. The technology sample shall be inspected by the Approval Authority in accordance with the requirements from clause 13.

b. The qualifying authority may waive the need for technology sample.

14.15.3 Audit of assembly processing

a. The Approval Authority shall inform the supplier on the result of inspection of a technology sample specified in the requirement 14.15.2a.

b. The Approval Authority shall inform the supplier on acceptance regarding the start of the next stages of the approval process.

c. The audit of the supplier's assembly line shall be performed prior to verification programme.

   NOTE Guidelines to audit report is given in Annex D.

d. The findings of the audit shall remain confidential between Approval Authority and the supplier.

14.15.4 Verification programme

a. A verification programme shall be submitted to the Approval Authority for acceptance prior to the start of assembly of the test SMT in accordance with DRD from Annex G.

14.15.5 Final verification review

a. The verification test report shall contain the following information:
   1. Applicable documents for verification
   2. Manufacturing traveller including devices traceability
   3. Vibration profile and responses
   4. Shock input if applicable
   5. Thermal cycle
   6. Visual inspection and MIP reports
   7. Microsection
   8. Nonconformances reports.

b. The verification test report shall be made available to the Approval Authority.

14.15.6 Certification approval of assembly line

a. Following the completion of the final verification review, the following documents shall be submitted to the Approval Authority for approval:
   1. PID
   2. SMT summary tables.

b. Assembly line audit shall be conducted every four years by the Approval Authority.

c. In case of changes in assembly line, impacting its approval an early audit shall be conducted to re-establish the approval as specified in the requirement 14.15.6b.

15 Quality assurance

15.1 General

a. Requirements from clause 5 from ECSS-Q-ST-20 shall apply for "Quality assurance".

15.2 Data

a. Requirements from clause 14.2 from ECSS-Q-ST-70-08 shall apply for "Data".

15.3 Nonconformance

a. The requirements from clauses 5 and 6 from ECSS-Q-ST-10-09 shall apply for "Nonconformance".

15.4 Calibration

a. Requirements from clause 14.4 from ECSS-Q-ST-70-08 shall apply for "Calibration".

15.5 Traceability

a. Requirements from clause 14.5 from ECSS-Q-ST-70-08 shall apply for "Traceability".

15.6 Workmanship standards

a. <<deleted>>

b. Visual standards consisting of work samples or visual aids that illustrate the quality characteristics of all soldered connections involved shall be prepared and be available to each operator and inspector.

NOTE The illustrations presented in Annex I of this Standard can be included as part of the examples.

15.7 Inspection

a. During all stages of the process, the inspection points defined in the manufacturing flow chart shall be carried out.

b. The inspection shall be performed in conformance with clause 13 of this Standard.

c. <<deleted>>

15.8 Operator and inspector training and certification

a. Requirements from clause 18.8 from ECSS-Q-ST-70-08 shall apply for "Operator and inspector training and certification".

b. A training programme for operators and inspectors performing all processes contained within the PID shall be developed, maintained and implemented by the supplier to provide excellence of workmanship and personal skill in SMTs.

NOTE Records of training, testing and certification status of the operators are maintained for at least 10 years.

c. Operators and inspectors shall be trained and certified at a school or in-house training authorised by the Approval Authority.

d. The operators performing X-ray inspection shall be trained and in-house certified to perform and assess X-ray results.

15.9 Quality records

<<deleted, requirement modified in 15.9d>>

a. <<deleted, requirement modified in 15.9d>>

b. <<deleted, requirement modified in 15.9d>>

c. <<deleted, requirement modified in 15.9d>>

d. The following documents, as a minimum, shall be made available:

1. PID,
2. Audit report established by the Approval Authority,
3. Verification report.

16
<<deleted and moved into clause 14.7.2 and Annex I>>

Annex A (informative)
<<deleted>>

Annex B (informative)
<<deleted, SMT summary table DRD created in Annex H>>

Annex C (informative)
<<deleted>>

Annex D (informative)
Example of an SMT audit report

ECSS-Q-ST-70-38: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 1	**COMPANY DETAILS**				
1. NAME					
2. ADDRESS					
3. TEL					
4. FAX					
5. MANAGING DIRECTOR					
6. QUALITY MANAGER					
7. PRODUCTION MANAGER					
8. SMT CONTACT PERSON					
9. SMT PRODUCT RANGE AND HISTORY (brief summary)					
10. Numbers of SMT operators		Design Engineers		QA	

ECSS-Q-ST-70-38: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 2	**QUALITY SYSTEM**					
1. QUALITY MANUAL* Reference:						
Issue:						
Date:					Viewed	Y ☐ N ☐
2. ORGANISATION OF THE QUALITY DEPARTMENT FOR SMT						
3. INTERNAL QUALITY AUDIT SYSTEM Reference:						
Date of last audit:						
Comments:					Viewed	Y ☐ N ☐
4. NON-CONFORMANCE SYSTEM Reference:						
	No. of NCRs in previous 12 months:		No. open at audit date:		Viewed	Y ☐ N ☐
5. CURRENT QUALITY APPROVALS Date of last assessment						
6. COMMENT ON COMMITMENT TO ECSS-Q-ST-70-38						
7. REFERENCE TO GENERAL ESA AUDIT & Date						

* Note: Request that a copy of the Contents List of the Quality Manual be appended to this report (See Attachment 1).

ECSS-Q-ST-70-38: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 3	**PROCESS CONTROL**
1. SMT APPROVED (if any) Make reference to an existing list of SMT configurations considered already tested. Identify how the SMT was tested.	

2. Make reference to the procedures that have the following functions and identify current issue and date:	
Process Identification Document	
1. Process instructions	Viewed: Y ☐ N ☐
2. Workmanship acceptance/rejection criteria	Viewed: Y ☐ N ☐
3. Calibration of SMT tooling	Viewed: Y ☐ N ☐
4. Control of limited Shelf life materials	Viewed: Y ☐ N ☐
5. Material procurement control with CofC or CofTest	Viewed: Y ☐ N ☐

3. TRAINING Make reference to the procedure for operator and inspector training. Identify the number of certificated operators and inspectors.	Viewed:	Y ☐ N ☐	Certificates viewed:	Y ☐ N ☐

ECSS-Q-ST-70-38: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 4	**FACILITIES**
CHECK LIST	
Devices storage and kitting area.	
Humidity and temperature control	
ESD protection and control	
Cleanliness in assembly areas	
Calibration	ESD (floor, mat, chair, wrist, solder iron….):
	Degolding, pretinning bath:
	Lead forming:
	Machine reflow:
	Solder tip:
	Repair station:
	Ovens:
Lighting in Lux	Degolding:
	Pretinning:
	Lead forming:

	HS Assembly:
	Stacking, bonding:
	Conformal coating:
PCB drying ovens and procedure	Unpopulated:
	Populated without conformal coating:
	Populated with conformal coating:
Oven	Baking of naked PCB:
	Baking of populated PCB:
	Curing of adhesive:
	Curing of conformal coating:
	Repair prior conformal coating
	Repair after conformal coating:
Bending tools	
Magnification aids	Device preparation (degolding, pretinning, lead forming):
	After solder paste application:
	After assembly by machine reflow:
	During assembly by hand:
	Final inspection:
Degolding bath (250°C-280°C)	

Pretinning (210-260°C)	
Solder fluxes (internal and external) used. Flux activity and trademark.	Degolding, pretinning:
	Solder paste:
	Hand soldering:
Cleaning Solvents	PCB cleaning:
	Degolding, pretinning:
	Soldering by machine reflow:
	Solder screen
	Soldering by hand:
	Prior to bonding, stacking:
	Prior to conformal coating:
Solder alloys (chemical composition, supplier, trademark and associated flux	-Dispensing:
	Screen printing:
	HS:
Solder paste application	Stencil:
	Dispensing:
	Repair station:
Pick and place machine	
Machine reflow	
Is the soldering equipment well	Machine reflow:

controlled (temperature-time profile, speed control…). How is the temperature profile controlled on the FM?	Solder Iron:
Hand Soldering iron (280°C to 340°C max)	
Fume exhaust facilities	
Repair station	
Cleaning Equipment	Machine reflow
	Hand soldering:
Cleanliness Testing (< 1,6 µg/cm^2)	
Stacking , bonding compounds	
Refrigerators: check expiration dates for adhesives, conformal coatings	Solder paste:
	Adhesive:
	Conformal coating:
Conformal Coating used	Curing conditions:
Cleanliness in conformal coating facilities	
Areas for Non-Conforming Items (Quarantine)	
Laboratories exist for: - Temperature cycling - Vibration	

- Electrical testing - Microsectioning	
SMT Assembly Traveller (operator activities, inspector stamps)	

END OF SECTION 4

ECSS-Q-ST-70-38: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 5 FINAL ASSESSMENT

AN ASSESSMENT OF THE SURFACE MOUNT TECHNOLOGY LINE AT THE FOLLOWING SUPPLIERS FACILITY HAS BEEN UNDERTAKEN AND THE FOLLOWING CONCLUSIONS MADE:

Supplier:
Address:

THE FACILITIES FOR THE ASSEMBLY OF SURFACE MOUNT TECHNOLOGY (ACCORDING TO ECCS-Q-ST-70-38C AT THE ABOVE SUPPLIER'S SITE ARE CONSIDERED:

SUITABLE CONDITIONALLY SUITABLE NOT SUITABLE

SUMMARY OF FINDINGS/CONDITIONS OF APPROVAL/SUMMARY OF CORRECTIVE ACTIONS NECESSARY:

Actions	Findings	Due date

NAME SIGN

PROCESS ASSESSMENT CARRIED OUT BY (Approval Authority):

IN PRESENCE OF (CONTRACTOR):

DATE:

Approval Authority: DATE:

END OF DOCUMENT

Annex E (informative) Additional information

E.1 <<deleted>>

<<deleted>>

E.2 Melting temperatures and choice

Table E-1: Guide for choice of solder type

Solder type	Melting range (		Uses
	Solidus	Liquidus	
63 tin solder (eutectic)	183	183	Soldering printed circuit boards where temperature limitations are critical and in applications with an extremely short melting range. Preferred solder for surface mount devices.
62 tin silver loaded	179	190	Soldering of terminations having silver and or silver palladium metallization. This solder composition decreases the scavenging of silver surfaces.
60 tin solder	183	188	Soldering electrical wire/cable harnesses or terminal connections and for coating or pretinning metals.
96 tin silver (eutectic)	221	221	Can be used for special applications, such as soldering terminal posts.
75 indium lead	145	162	Special solder used for low temperature soldering process when soldering gold and gold-plated finishes. Can be used for cryogenic applications.
70 indium lead	165	175	For use when soldering gold and gold-plated finishes when impractical to degold.
50 indium lead	184	210	This solder has low gold leaching characteristic.
10 tin lead	268	290	For use in step-soldering operations where the initial solder joint must not be reflowed on making the second joint (e.g. CGA columns, connections internal to devices)

Annex F (normative) Process Identification Document (PID) - DRD

F.1 DRD identification

F.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-38, requirement 5.1.2a.

F.1.2 Purpose and objective

The purpose of the PID is to consolidate the overall management, process and facilities utilised during the manufacturing and verification of the SMD.

F.2 Expected response

F.2.1 Scope and content

<1> SECTION 1: Document format

a. The PID shall contain the following information about the Document Format:

1. Cover page: document title, document reference, revision number and date, page numbering, signing of Production and Quality representatives,
2. Follow-up of PID updates: registration of PID updates indicating the nature of the update and the sections and pages updated,
3. Purpose and scope of the document,
4. Table of contents.

<2> SECTION 2: Manufacturing control

a. The PID shall contain the Manufacturing control flow chart of the verified SMT.

NOTE 1 This illustrates the various stages of procurement, manufacturing and inspection operations specific to this technology in a flow chart format.

NOTE 2 It can be used to identify, among others:

- the operation,
- the body responsible for its implementation,
- related documents: (only their reference),
- procurement specifications (for materials),
- acceptance inspection procedures (for materials and devices),
- manufacturing procedures,
- manufacturing and quality control procedures during and at the end of production.

<3> SECTION 3: Specifications

a. The PID shall contain the following information about Specifications:

1. List of procurement specifications, assembly procedures and inspection procedures concerning the technology dealt within the PID, including the precise title, the reference or number, the revision number and date of each document,
2. Printed circuit design rules in compliance with requirements from ECSS-Q-ST-70-12,
3. General Quality Assurance documents relating to the technology.

<4> SECTION 4: Organisation

a. The PID shall contain the following information about Organisation:

1. Represented as a flow chart: organization of the company, organization of production department and organization of the quality Department,
2. Focal point and PID responsible,
3. Operators and inspectors' certification methodology.

<5> SECTION 5: Manufacturing traveller or log file

a. The PID shall contain as a minimum the following information about the Manufacturing traveller or log file:

1. The sequencing of the various operations in their logical order of execution,
2. The references of the documents referred to and used during these operations,

3. The references of the Quality documents to ensure traceability of the various batches of material used (record reference), together with the work stations and tools employed,

4. The signatures of the various actors with the date on which the task was completed.

<6> Section 6: List of verified technology

a. The PID shall contain as a minimum the following information about the List of verified technology:

1. List of materials,

2. Temperature and time profiles for the machine reflow used in the verification,

3. List of verified devices per assembly configuration,

4. List of sensitive devices,

5. List of devices with limited project verification.

<7> SECTION 7: Description of production line

a. The PID shall contain as a minimum the following about the Description of production line:

1. Layout of premises with associated surface area, with indication of location of production machines and quality inspection,

2. Working environment; cleanliness class, ambient temperature limits, humidity and positive pressure limits for each type of activities.

<8> SECTION 8: List of equipment

a. The PID shall contain a list of all machines and tools utilised during the SMT activity.

<9> SECTION 9: List of laboratory services

a. The PID shall contain range and capability of supporting laboratory services.

<10> SECTION 10: Project SMT heritage

a. The PID shall contain a of board SMT assembly by year manufactured in accordance with the PID.

F.2.2 Special remarks

None.

Annex G (normative)
Verification programme report - DRD

G.1 DRD identification

G.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-38, requirement 14.1a.

G.1.2 Purpose and objective

The purpose of the Verification programme report DRD is to detail the requirements for the documentation of the verification programme.

G.2 Expected response

G.2.1 Scope and content

a. The verification programme documentation shall contain as a minimum the following:

1. Indication of method of the assembly:
   (a) The soldering method and repair methods
2. PCB information:
   (a) PCB material and manufacturer
   (b) PCB footprint surface finish
   (c) Number of layers
   (d) Thickness
   (e) Built up with identification of signal and full copper plane
   (f) Connection of the footprints to the internal layer representative of the FM
   (g) Location of the devices on the PCB
   (h) Location of the mechanical fixation or stiffeners if any
   (i) Number of PCB used for the verification programme.

3. Materials used
   (a) Solder paste and wire designation, commercial trade mark, and composition with associated flux class
   (b) Flux class used for pretinning and soldering
   (c) Conformal coating
   (d) Adhesive for mechanical, and for thermal
   (e) Solvent
   (f) Others.
4. List of devices
5. Environmental test conditions and facility
6. Verification method Microsection or Electrical monitoring
   (a) Microsection laboratory
7. PID and Manufacturing document process references
8. Verification workflow
9. Verification by similarity
10. NCRs
11. Certification status of the operators and inspectors
12. Compliance status of the operators and inspectors
13. Compliance of the manufacturing room
14. Additional information.

NOTE to item 1.(a): When machine reflow is used then the verified hand soldering or other method is used.

b. The content of documentation specified in G.2.1a.1 to 13 may be tailored for companies having already an ECSS SMT approval.

G.2.2 Special remarks

None.

Annex H (normative)
SMT summary table - DRD

H.1 DRD identification

H.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-38, requirement 14.11a.

H.1.2 Purpose and objective

The purpose of the SMT summary table is to consolidate the approval status of the boundary conditions for the verification activity.

H.2 Expected response

H.2.1 Scope and content

a. The SMT summary table shall include the following data

1. Assembly processes
2. PID reference with issue
3. Solder type: For machine reflow and for hand assembly
4. Conformal coating
5. Substrate type: Polyimide
6. Device data as shown in Table H-1.

NOTE Examples of assembly processes are vapour phase and hand soldering or convection reflow + hand soldering or hand soldering.

H.2.2 Special remarks

None.

Table H-1: Device type preparation and mounting configuration

Device family	Package	Manufacturer	Package dimensions	Bonding material (under device)	Stacking material (edge or corner)	Terminal material	Lead finish	Pitch (mm)	Nominal Terminal thickness (mm)/ Nominal width	In-House degolding / pretinning	In-house lead forming Yes/No/NA	Artificial stand-off Yes/No	Final report
Ceramic chip	C0603 Type 1		Length, width	NA	NA		Sn/Pb	NA	NA	No	N/A	No	
Ceramic	C0603 Type 11										N/A		
Ceramic resistor	R0805			NA	NA		Sn/Pb	NA	NA	No	N/A	No	
Diode	D5-B										N/A		
Tantalum capacitors													
IC	FP10 Bottom brazed			yes	One the side	Alloy42	Gold	1,27	0,25	yes	yes	NA	
CQFP	CQFP196 top brazed					Kovar					No		

Annex I (informative)
Visual and X-ray workmanship standards

I.1 Workmanship illustrations for standard SMDs

I.1.1 Chip components

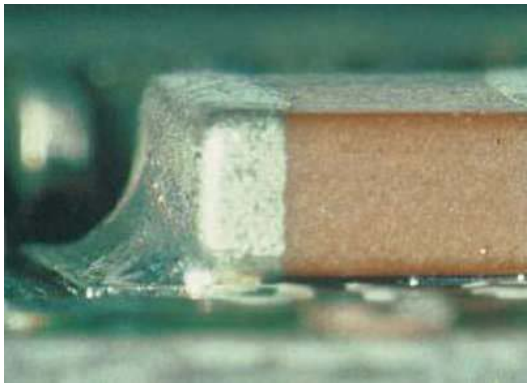


Figure I-1: Preferred solder (see also Table 11-1)

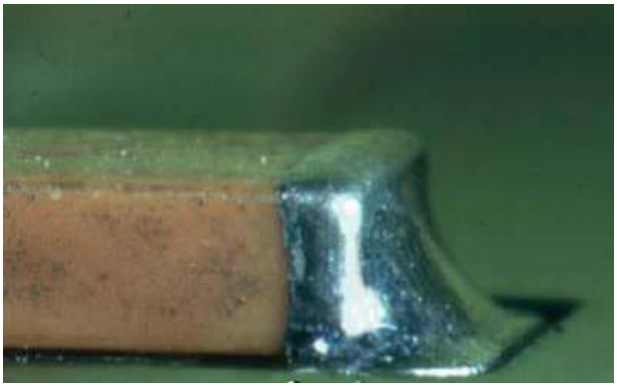


Figure I-2: Acceptable, maximum solder (see also Table 11-1)

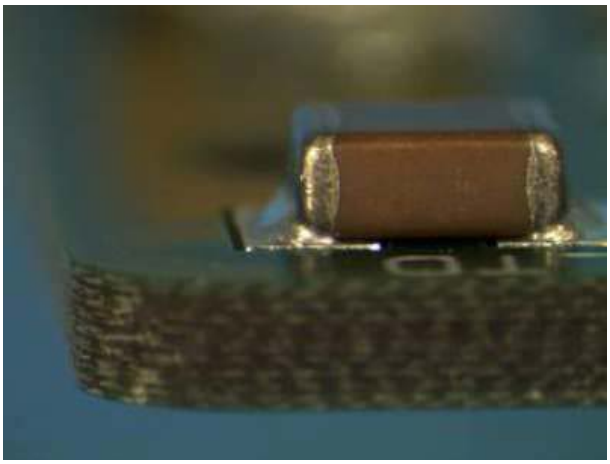


Figure I-3: Acceptable, minimum Solder (see also Table 11-1)

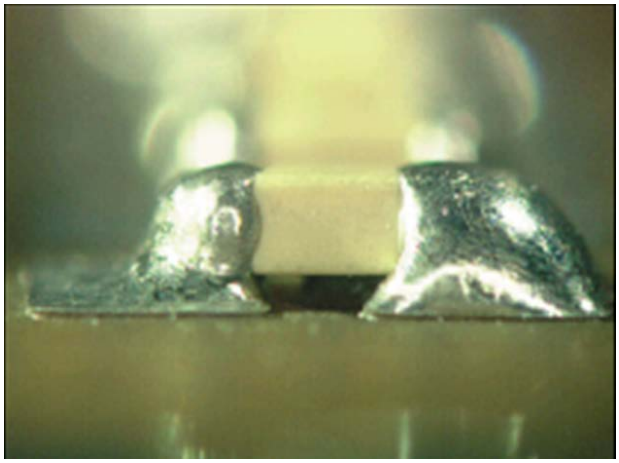


Figure I-4: Unacceptable, excessive solder (see also Table 11-1)

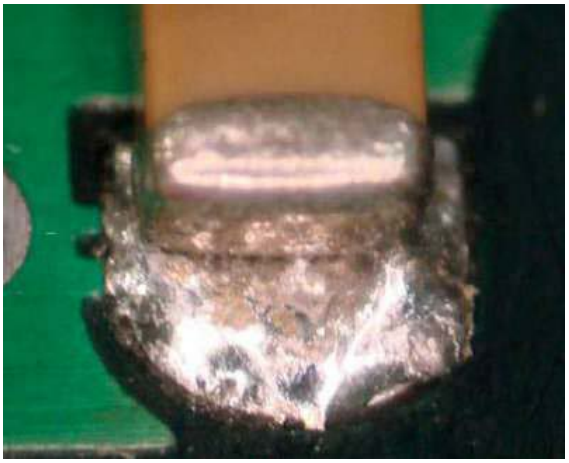


Figure I-5: Unacceptable, poor wetting (see also Table 11-1)

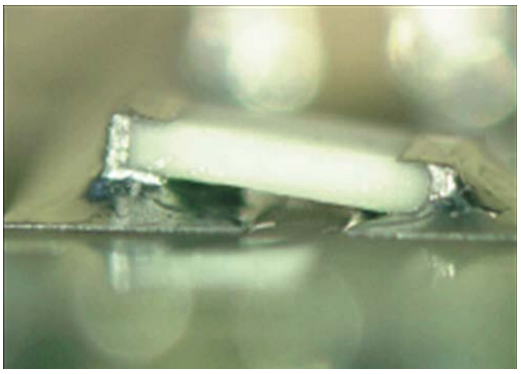


Figure I-6: Unacceptable, excessive tilt (see also Table 11-1)

Figure I-7: Unacceptable, tombstone effect

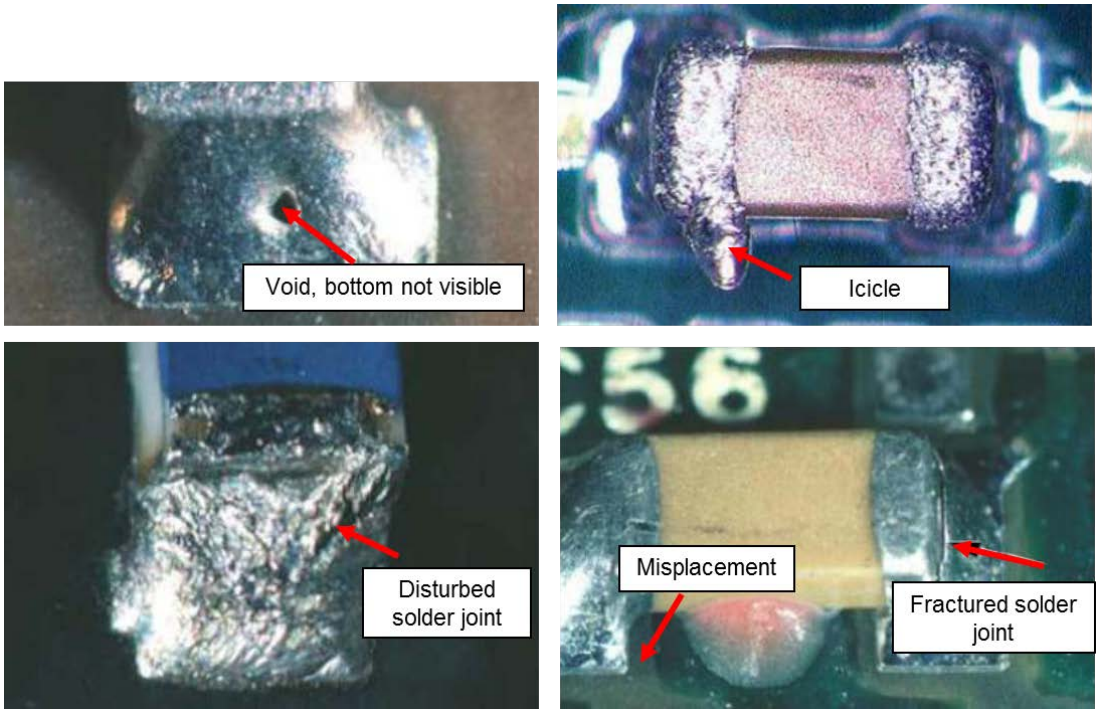


Figure I-8: Examples of Unacceptable solder joints - (see also Table 11-1)

I.1.2 MELF components

Figure I-9: Acceptable, terminal wetted along end, face and sides (see also Table 11-1)

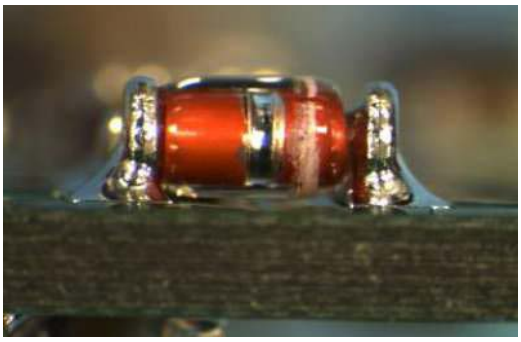


Figure I-10: Acceptable, maximum solder joint (see also Table 11-3)

Figure I-11: Not Acceptable, insufficient solder joint (see also Table 11-3)

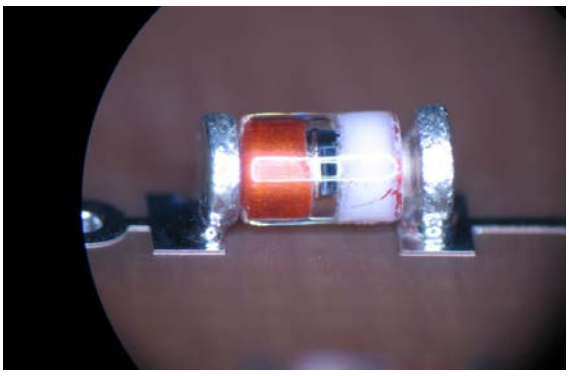


Figure I-12: Unacceptable overhang

I.1.3 Gull-wing leaded devices with round, rectangular, ribbon shape

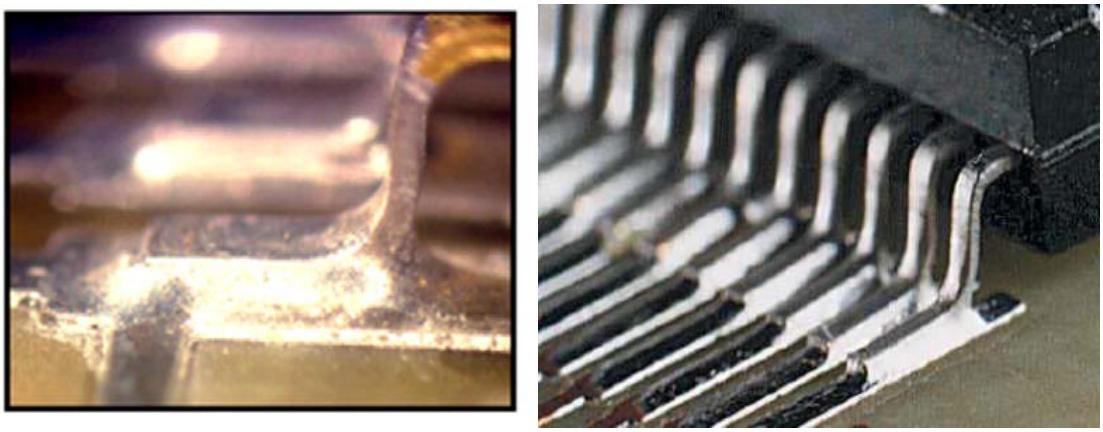


Figure I-13: Examples of Gullwing leads: Acceptable

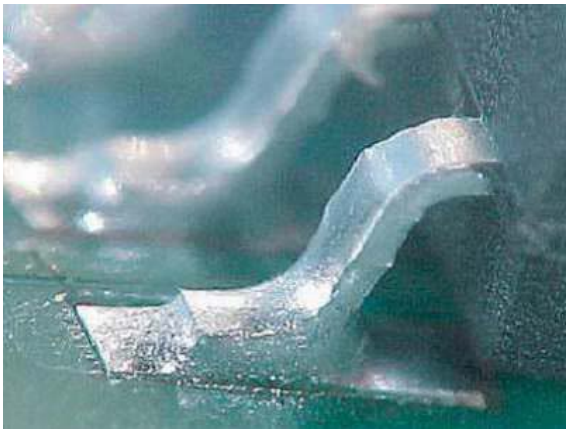


Figure I-14: Examples of gull-wing device with rectangular lead: Acceptable

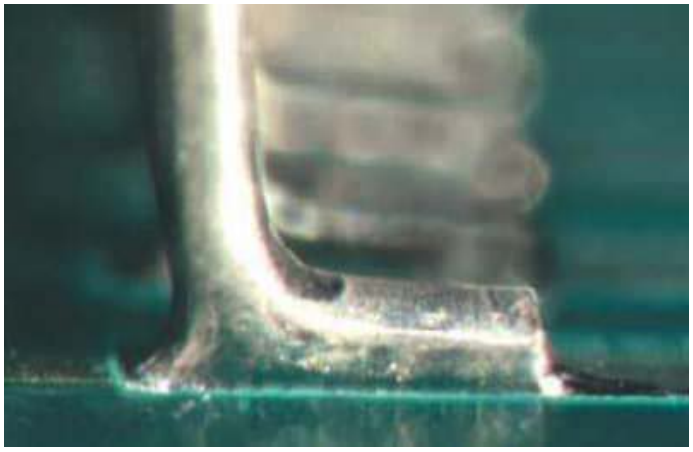


Figure I-15: Acceptable, minimum solder joint

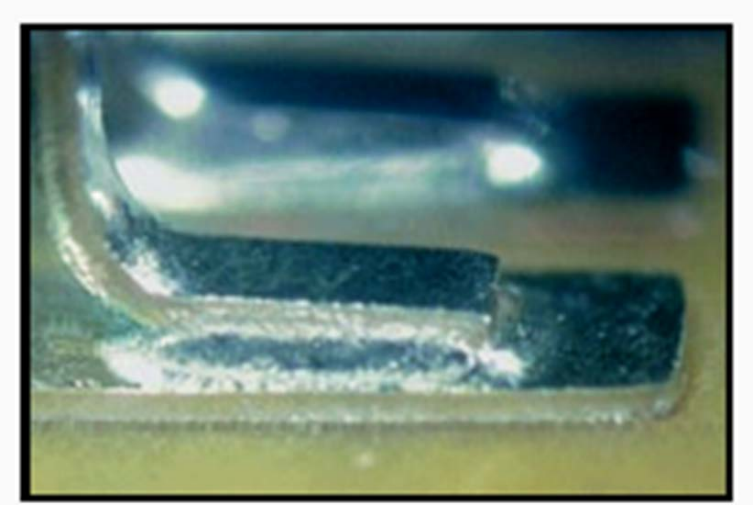


Figure I-16: Unacceptable, insufficient heel fillet

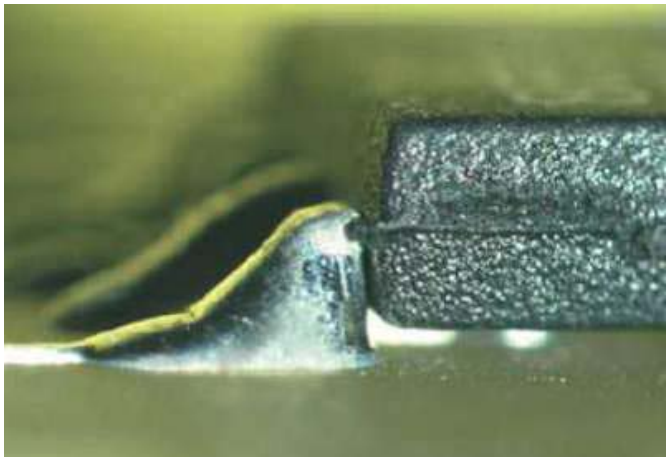


Figure I-17: Unacceptable, excessive solder

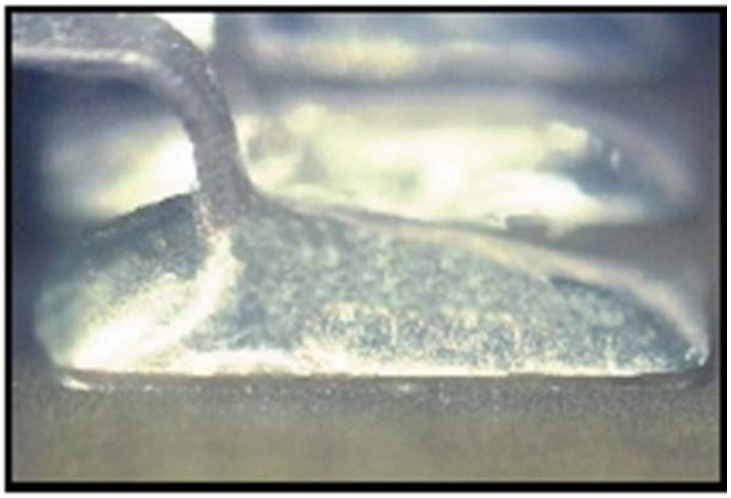


Figure I-18: Unacceptable, excessive solder

I.1.4 "J" leaded devices

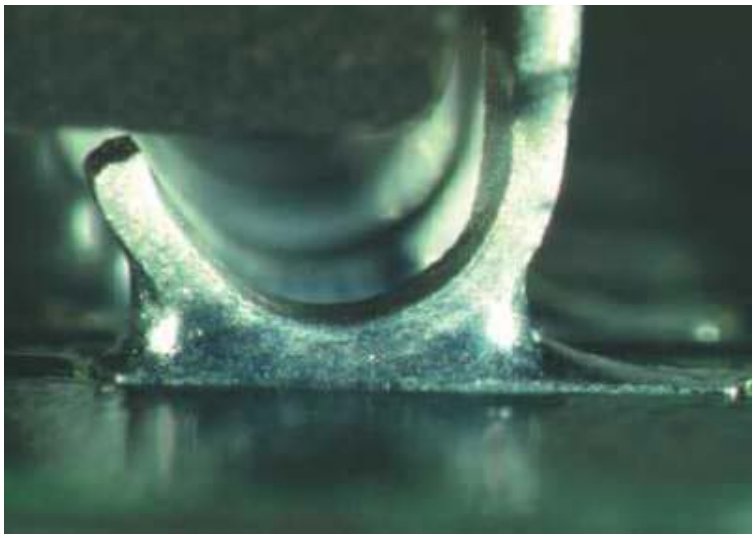


Figure I-19: Preferred solder joint

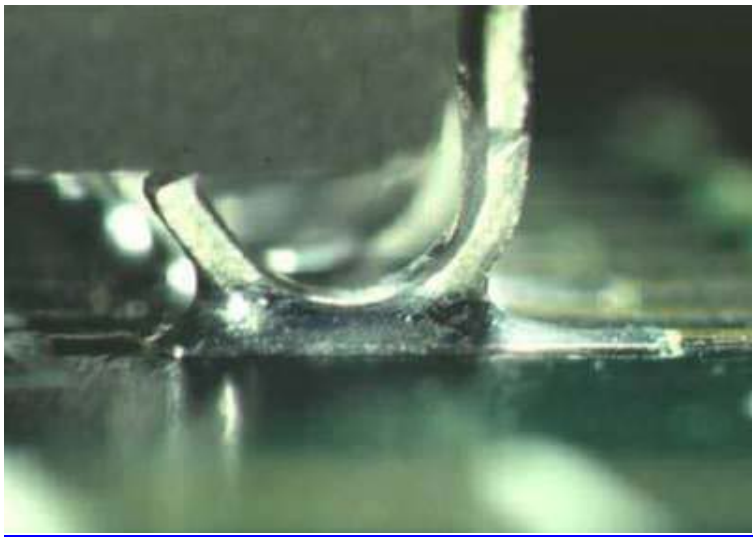


Figure I-20: Acceptable solder joint

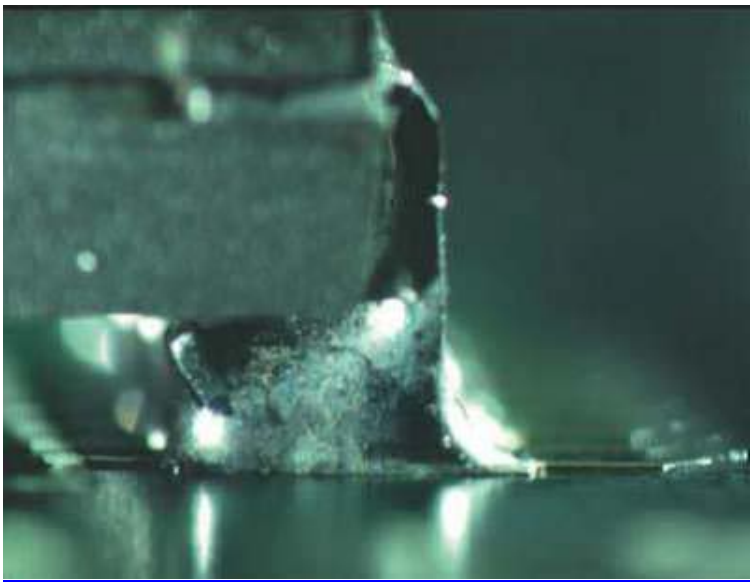


Figure I-21: Unacceptable, excessive solder joint

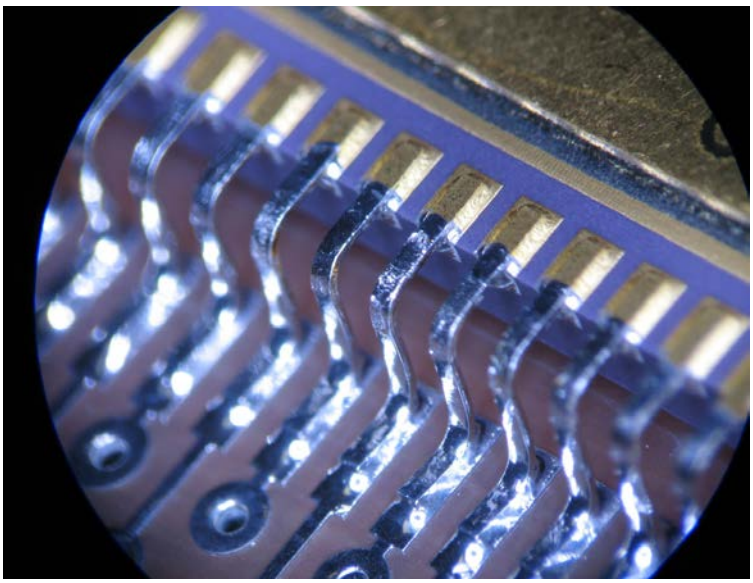


Figure I-22: Unacceptable, excessive degolding

I.1.5 L-shape Inward leaded component

Figure I-23: Acceptable, preferred solder joint

I.1.6 LCC devices

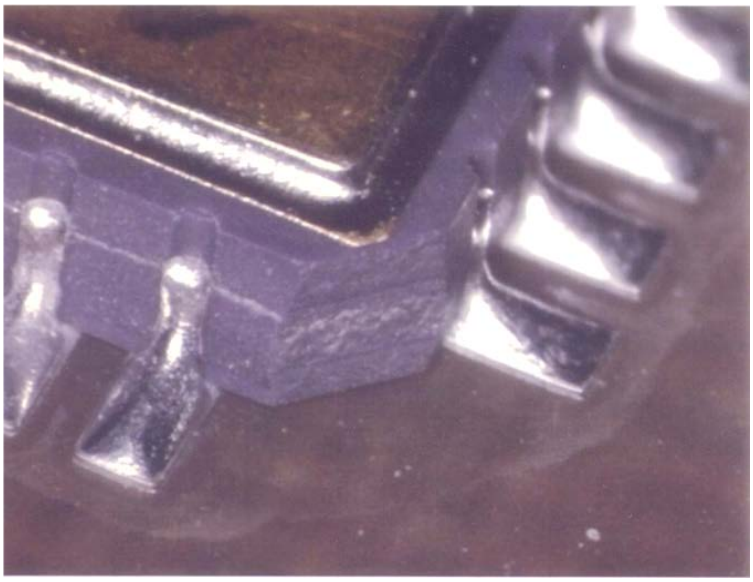


Figure I-24: LCC General view, acceptable solder joints

I.1.7 Miscellaneous soldering defects

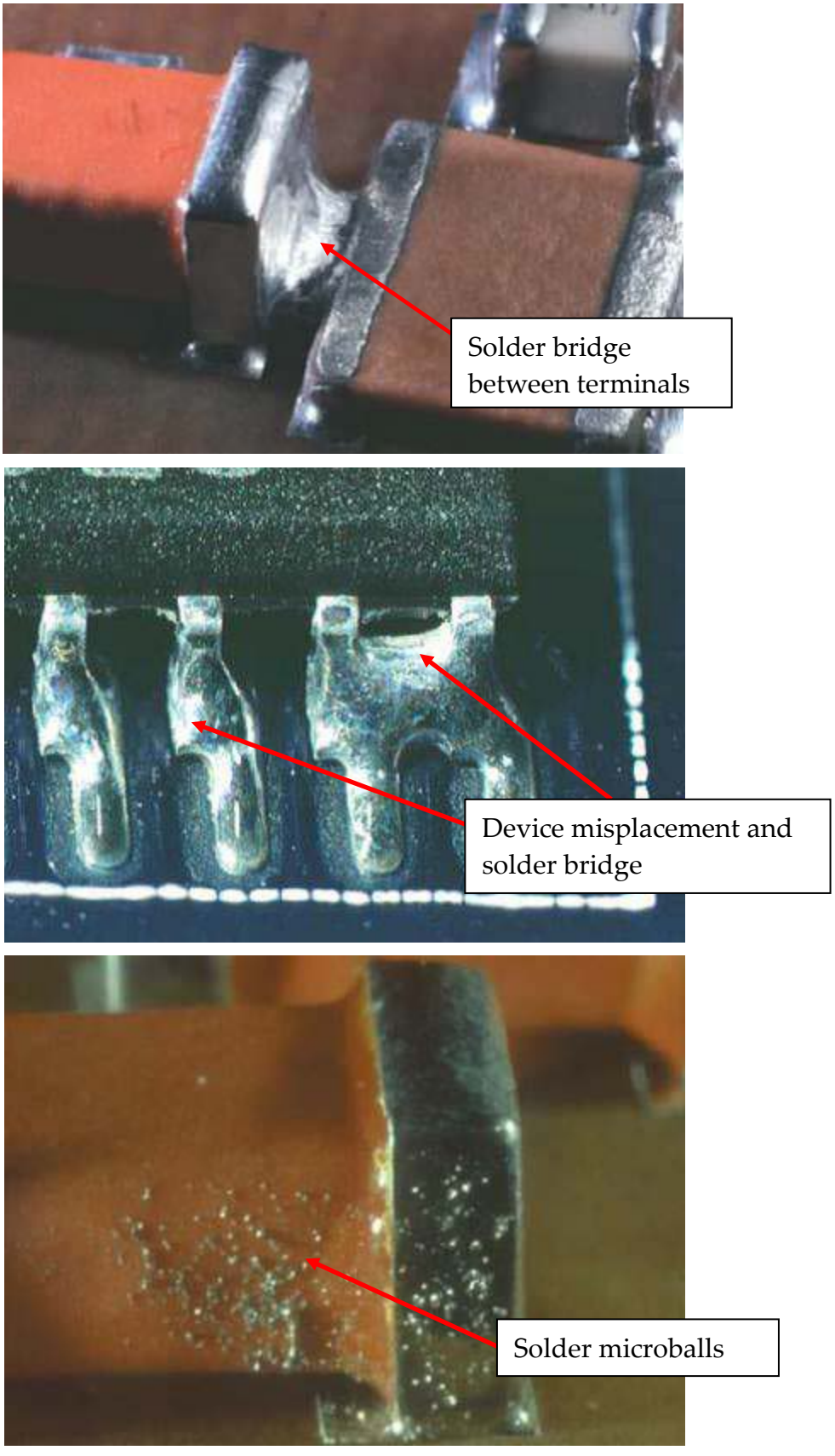


Figure I-25: Examples of unacceptable soldering

I.2 Workmanship illustrations for ball grid array devices

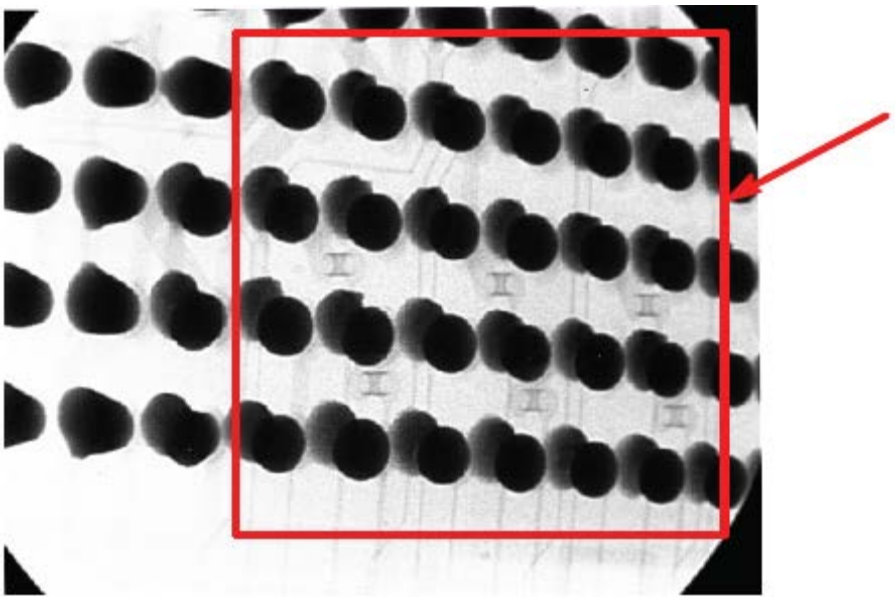
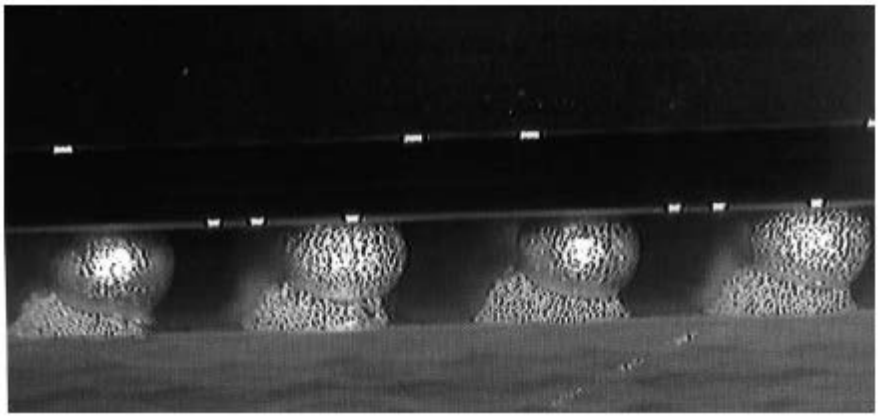
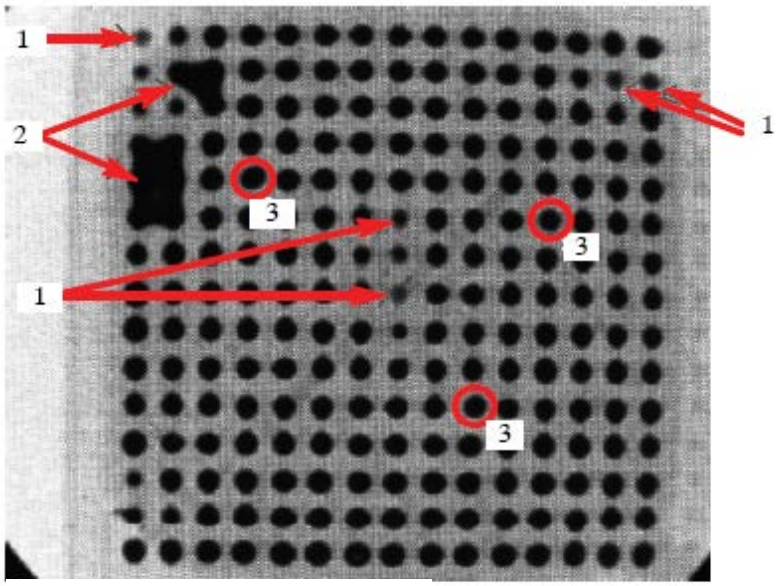


Figure I-26: Angled-transmission X-radiograph showing solder paste shadow due to partial reflow: Reject



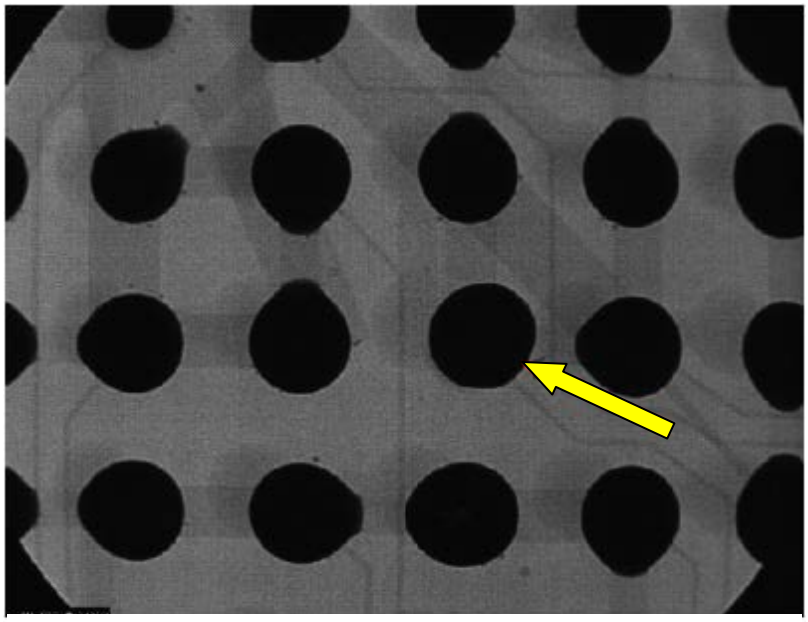
- non-reflow of solder paste: Reject
- maximum misplacement (15 % of pad ∅): Accept

Figure I-27: Micrograph showing



1. missing balls: Reject
2. bridges: Reject
3. non-wetted pads: Reject

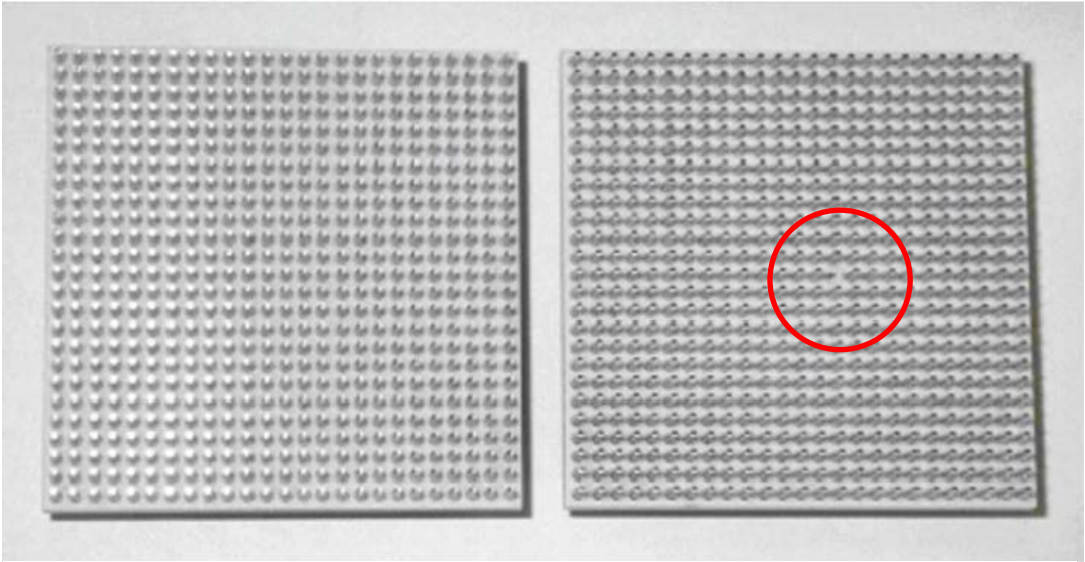
Figure I-28: Perpendicular transmission X-radiograph showing unacceptable defects



Solder has not flowed to extent of teardrop pad: Reject

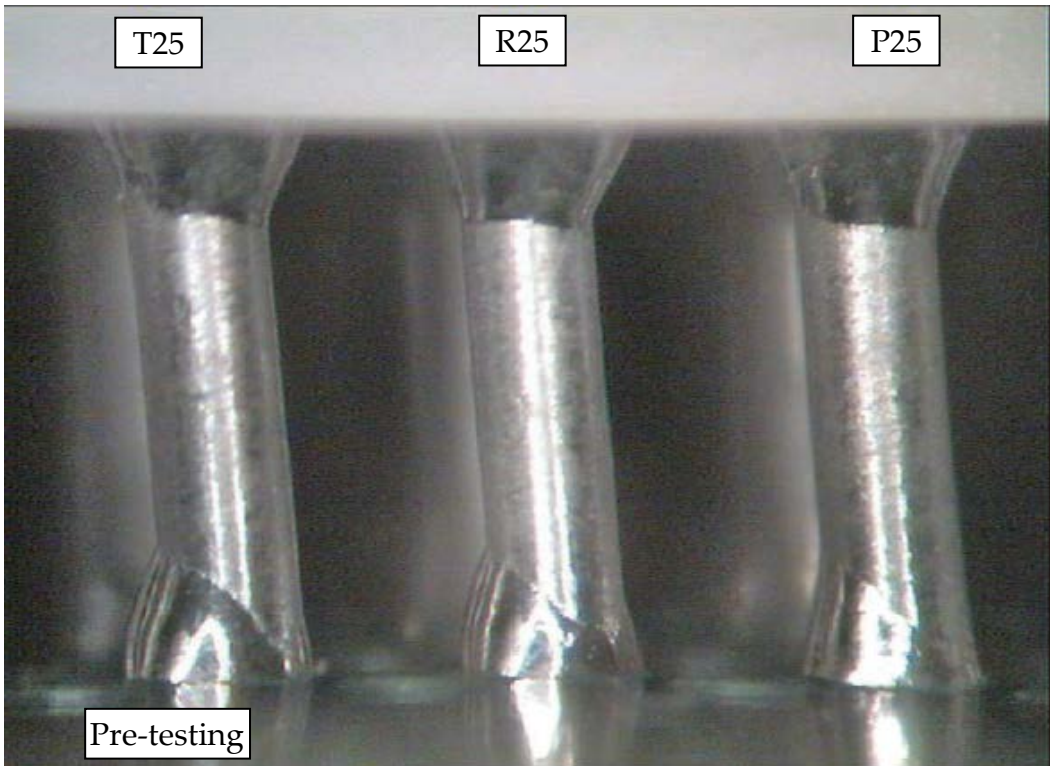
Figure I-29: Perpendicular transmission X-radiograph showing non-wetted footprint

I.3 Workmanship illustrations for column grid array devices



Good consistency of column alignment: Accept Missing column: Reject.

Figure I-30: Underside view showing missing column



NOTE: Asymmetry of solder fillets at PCB is consequence of teardrop footprints and is acceptable

Figure I-31: CGA mounted on PCB showing columns tilted < 10°: Accept

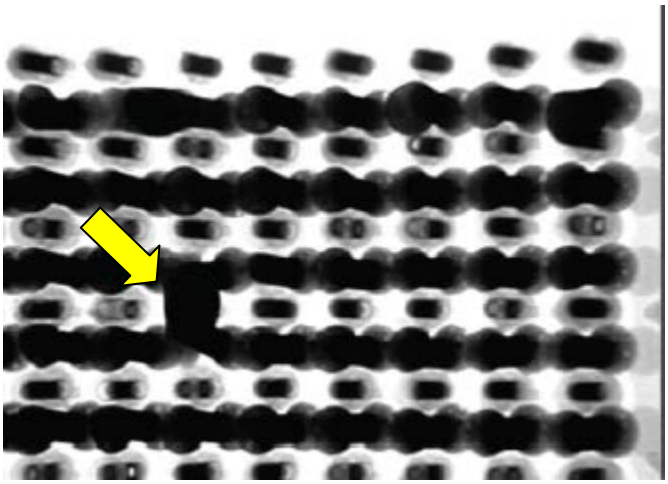


Figure I-32: X-radiograph of CGA mounted on PCB showing solder bridge: Reject

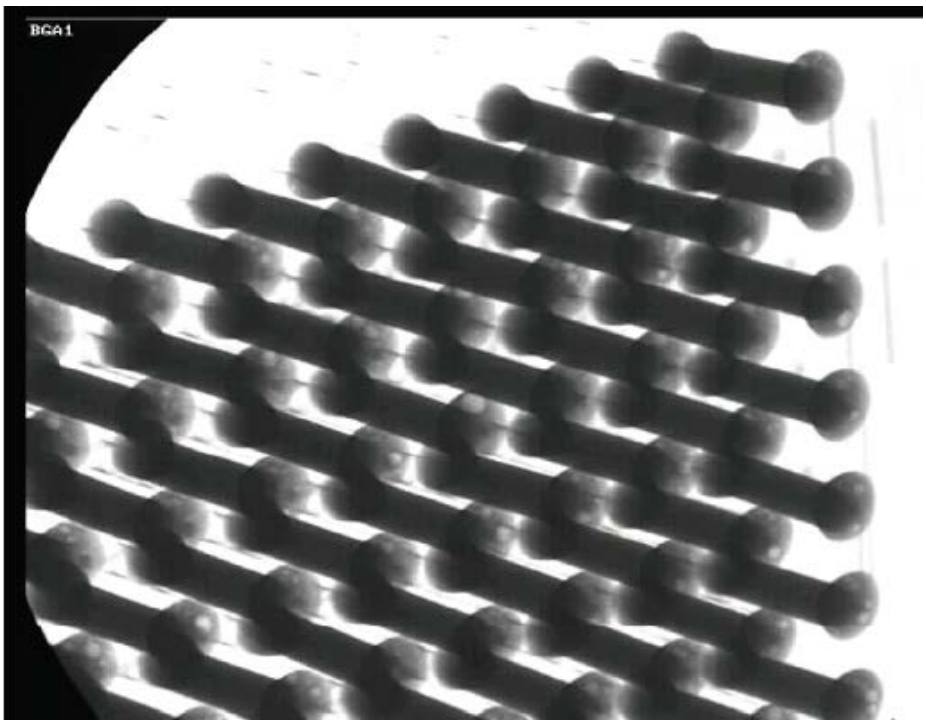
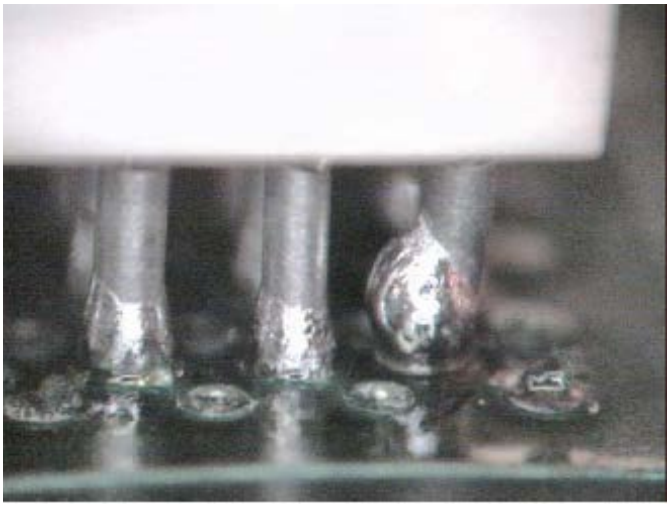


Figure I-33: X-radiograph of CGA showing solder fillets at base of columns: acceptable

Figure I-34: Micrograph of CGA mounted on PCB, bent column: reject



Unsoldered column: Reject.

Figure I-35: Micrograph of CGA mounted on PCB

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