ECSS-Q-ST-70-61C DIR1
26 March 2019

Space product assurance

High reliability assembly for surface mount and through hole connections

This Draft is distributed to the ECSS community for Public Review.
NOTE: During the Public Review the ECSS community is asked to provide representative photos for Annex F inside which placeholder were inserted to illustrate workmanship.
In case no photos are available the relevant table will be deleted when publishing the standard.

Start of Public Review: 27 March 2019
End of Public Review: 24 May 2019

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ECSS Secretariat
ESA-ESTEC
Requirements & Standards Division
Noordwijk, The Netherlands

Foreword

This Standard is one of the series of ECSS Standards intended to be applied together for the management, engineering, product assurance and sustainability in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards. Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

This Standard has been prepared by the ECSS-Q-ST-70-61C Working Group, reviewed by the ECSS Executive Secretariat and approved by the ECSS Technical Authority.

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Current step	
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Next steps	
	DRR implementation
	DRR Feedback
	TA Vote for publication and preparation of DOORS module
	Publication

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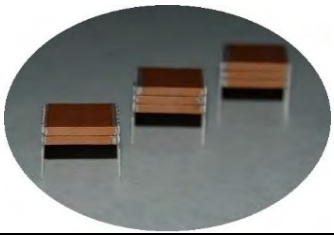
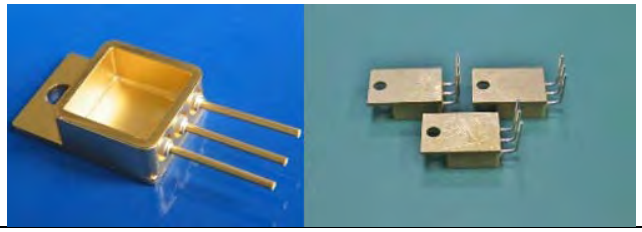
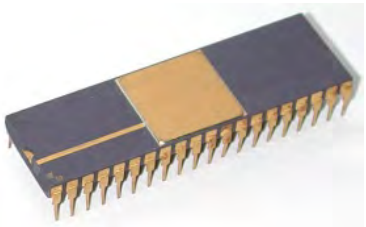
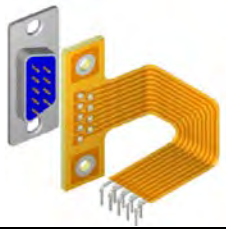
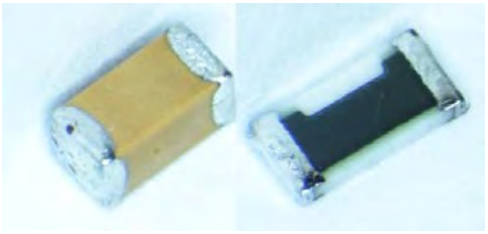
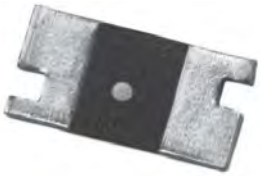
Introduction

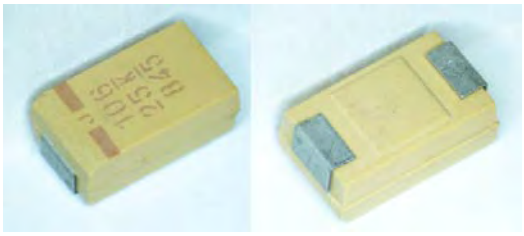
This document prescribes requirements for electrical connections of plated through hole components and for leadless and leaded surface mounted components (SMD) on spacecraft and associated equipment.

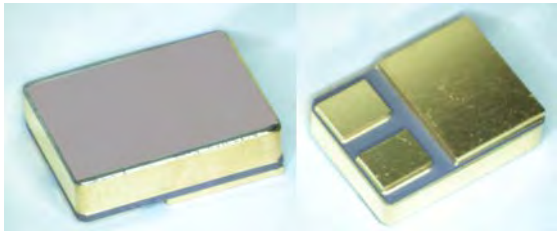
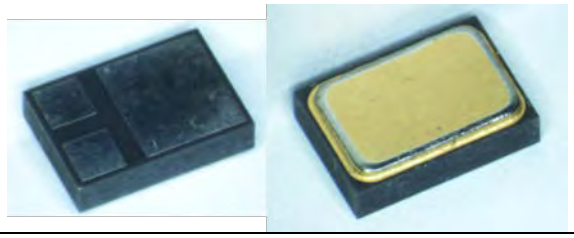
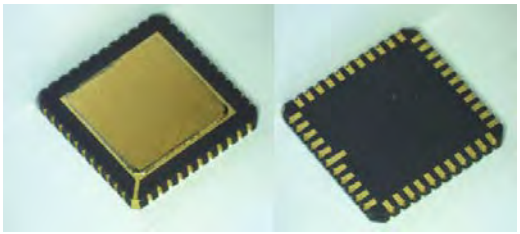
In the following table, principal types of through hole components and SMDs, including examples, can be gathered in the following families:

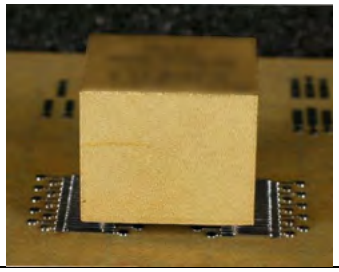
THROUGH HOLE COMPONENTS	
Radial component resistors fuses diodes	
Axial component capacitors	
Stacked capacitors CH capacitors CNC capacitors	
TO Metal Can package TO-39	

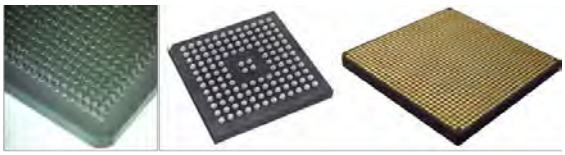
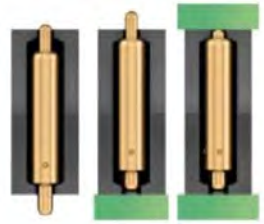
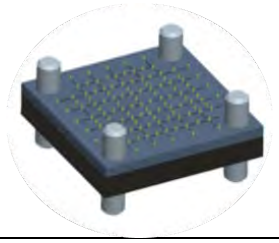
THROUGH HOLE COMPONENTS	
TO Metal tab package TO254	
Dual in Line Package (DIL or DIP) Side brazed DIP	
Connectors	
Leaded magnetics transformers with straight pins	
Sculptured flex	

SMT COMPONENTS	
Rectangular and square end-capped or end-metallized ceramic component with rectangular body, leadless chip (see 10.5.2.1) end capped chip resistors and end capped chip capacitors. resistors arrays	 
Rectangular and square end-capped or end-metallized metallic component with rectangular body, leadless chip (see 10.5.2.2) CSM 2512 Resistor with metallic terminations	 
Cylindrical and square end-capped components with cylindrical body, leadless chip (see 10.5.2.2) MELF for cylindrical end capped or	

SMT COMPONENTS	
D-5A for square end capped with barrel or rugby bodies	
Bottom terminated chip component (see 10.5.4) **This type of component has metallised terminations on the bottom side only)** Chip inductors **QFN** No lead (QFN)	 
Component with Inward formed L-shaped leads (see 10.5.5) moulded tantalum chip capacitors. SMD moulded shunt	 

SMT COMPONENTS	
Leadless component with plane termination (see 10.5.6) - With metal plane termination: SMD0.5, SMD1, SMD2, SMD0.2*(TO276 Jedec family denomination)	
- With non-metal plane termination: SMD0.2* ***package exists in two versions**	
Leaded component with plane termination (see 10.5.7) Diode PAcKage (DPAK or TO252)	  DPAK
Castellated chip carrier component (see 10.5.8) The main component of this type is leadless ceramic chip carrier (LCCC) LCC6	 

SMT COMPONENTS	
Flat pack and gull-wing leaded component with round, rectangular, ribbon leads (see 10.5.9) small-outline transistor (SOT), small—outline package (SO), flat pack and quad flat pack (QFP) and SMD connectors with stress-relief. This family also comprises components for through-hole mounting that have been reconfigured to surface mounting. transformers	 
"J" leaded component **(see 10.5.10)** ceramic leaded chip carriers (CLCC) and plastic **leaded chip carriers (PLCC).**	
Components with ribbon terminals without stress relief (flat lug leads) (see 10.5.11) This package has flat leads extending from the sides	
Stacked modules components with leads protruding vertically from bottom (see 10.5.12)	

SMT COMPONENTS	
Area array components (AAD) (see 10.5.13) Components connected via an array of solder columns (Column Grid Array – CGA), solder balls (Ball Grid Array – BGA) or directly to the board (Land Grid Array – LGA). The columns and balls consist of various types of solder with wide-ranging properties.	 CGA BGA LGA
Solderless connection (see 10.6) solderless connectors solderless interposers for LGA or connectors	 

1
Scope

This Standard defines the technical requirements and quality assurance provisions for the manufacture and verification of high-reliability electronic circuits of surface mount, through hole and solderless assemblies.

The Standard defines workmanship requirements, the acceptance and rejection criteria for high-reliability assemblies intended to withstand normal terrestrial conditions and the environment imposed by space flight.

The mounting and supporting of components, terminals and conductors specified in this standard applies only to assemblies designed to continuously operate over the mission within the temperature limits of -55 °C to +85 °C at solder joint level.

Requirements related to printed circuit boards are contained in ECSS-Q-ST-70-60 and ECSS-Q-ST-70-12.

This Standard does not cover the qualification and acceptance of the EQM and FM equipment with high-reliability electronic circuits of surface mount, through hole and solderless assemblies.

This Standard does not cover verification of thermal properties for component assembly.

This Standard does not cover pressfit connectors.

The qualification and acceptance tests of equipment manufactured in accordance with this Standard are covered by ECSS-E-ST-10-03.

This standard may be tailored for the specific characteristics and constraints of a space project, in accordance with ECSS-S-ST-00.

2
Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revision of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the more recent editions of the normative documents indicated below. For undated references, the latest edition of the publication referred to applies.

ECSS-S-ST-00-01	ECSS system — Glossary of terms
ECSS-M-ST-40	Space project management — Configuration and information management
ECSS-Q-ST-10-09	Space product assurance — Nonconformance control system
ECSS-Q-ST-20	Space product assurance — Quality assurance
ECSS-Q-ST-60	Space product assurance — Electrical, electronic and electromechanical (EEE) components
ECSS-Q-ST-60-05	Space product assurance — Generic requirements for hybrids
ECSS-Q-ST-60-13	Space product assurance - Commercial electrical, electronic and electromechanical (EEE) components
ECSS-Q-ST-70	Space product assurance — Materials, mechanical parts and processes
ECSS-Q-ST-70-01	Space product assurance — Cleanliness and contamination control
ECSS-Q-ST-70-02	Space product assurance — Thermal vacuum outgassing test for the screening of space materials
ECSS-Q-ST-70-12	Space product assurance — Design rules for printed circuit boards
ECSS-Q-ST-70-28	Space product assurance — Repair and modification of printed circuit board assemblies for space use.
ECSS-Q-ST-70-60	Space product assurance —Qualification and procurement of printed circuit boards
ECSS-Q-ST-70-71	Space product assurance —Materials processes and their data selection

ESA-STR-258 (November 2008)	ESA-Approved skills training schools
ESCC 23500 (September 2013)	Requirements for lead materials and finishes for components for space application
IPC J-STD-004A (January 2004)	Requirements for Soldering Fluxes
IPC J -STD-033D (January 2018)	Handling, Packing, Shipping and Use of Moisture, Reflow, and Process Sensitive Devices
IPC-TM-650 (latest edition)	Test methods manual. Surface Insulation Resistance, Fluxes
ISO 9454-1:2016	Soft soldering fluxes; classification and requirements
ISO 14644-1:2015	Cleanrooms and controlled environments
MIL-STD-883 K Method 2009 (April 2016)	Test Method Standard, Microcircuits

3
Terms, definitions and abbreviated terms

3.1 Terms from other standards

a. For the purpose of this Standard, the terms and definitions from ECSS-S-ST-00-01 apply.

b. For the purpose of this Standard, the terms and definitions from ECSS-Q-ST-60 apply, in particular for the following term(s):

   1. commercial component

c. For the purpose of this Standard, the terms and definitions from ECSS-Q-ST-70-28 apply, in particular for the following term(s):

   1. repair
   2. rework

3.2 Terms specific to the present standard

3.2.1 approval authority

entity that reviews and accepts the verification programme, evaluating the test results and grants the final approval

3.2.2 assembly sensitive component

component prone to have cracks in solder joint exceeding 75 % of acceptance criteria of solder cracks or showing nonconformance outside the component manufacturer limit

NOTE 1 ESA list of assembly sensitive components is published on ESCIES for information, see www.escies.org.

NOTE 2 Each company maintains its own list of assembly sensitive components in the PID.

3.2.3 bifurcated terminal

terminal containing a slot or split in which wires or leads are placed before soldering

NOTE The term "**split terminal**" is synonymous.

3.2.4 blister

delamination in a distinct local area or areas

3.2.5 bonding

application process of adhesive underneath a package for mechanical or thermal purpose

3.2.6 bridging

build-up of solder or conformal coating between parts, component leads or base substrate forming an elevated path

3.2.7 clinched-lead termination

conductor or component lead which passes through a printed circuit board and is then bent to make contact with the printed circuit board pad

NOTE The clinched portion is not forced to lie flat on the pad and some innate spring back is desirable before this form of termination is soldered.

3.2.8 cold flow

movement of insulation

NOTE For example, Teflon® (PTFE), caused by pressure.

3.2.9 cold solder joint

joint in which the solder has a blocky, wrinkled or piled-up appearance and shows signs of improper flow or wetting action

NOTE It can appear either shiny or dull, but not granular. The joint normally has abrupt lines of demarcation rather than a smooth, continuing fillet between the solder and the surfaces being joined. These lines are caused by either insufficient application of heat or the failure of an area of the surfaces being joined to reach soldering temperature.

3.2.10 conformal coating

thin protective coating which conforms to the configuration of the covered assembly

3.2.11 contact angle

angle enclosed between half-planes, tangent to a liquid surface and a solid-liquid interface at their intersection

NOTE In particular, the contact angle of liquid solder in contact with a solid metal surface. An approximate value for this can be determined by shadow projection or other means, by

measuring after the solder has solidified. The contact angle is always the angle inside the liquid.

3.2.12 co-planarity

maximum distance between lowest and highest termination when component rests on flat surface

3.2.13 collective assembled components

set of components that are soldered to PCB in one operation

3.2.14 critical zone

area in the solder joint in which the existence and magnitude of cracks is subject to acceptance or rejection

3.2.15 dewetting

condition in a soldered area in which the liquid solder has not adhered intimately, characterized by an abrupt boundary between solder and conductor, or solder and terminal/termination area

NOTE This is often seen as a dull surface with islands of thicker shiny solder.

3.2.16 disturbed solder joint

unsatisfactory connection resulting from relative motion between the conductor and termination during solidification of the solder

3.2.17 dynamic wave soldering machine

system that achieves wave soldering and which consists of stations for fluxing, preheating, and soldering by means of a conveyor

3.2.18 electrical clearance

spacing between non-common electrical conductors on external layers of a printed circuit board assembly

NOTE The distance between conductors depends on the design voltage and DC or AC peaks. Any violation of minimum electrical clearance as a result of a nonconformance is a defect condition.

3.2.19 fillet

smooth concave build-up of material between two surfaces

NOTE Example: A fillet of solder between a component lead and a solder pad or terminal, or a fillet of conformal coating material between a component and printed circuit board.

3.2.20 flux

material which, during soldering, removes the oxide film, protects the surface from oxidation, and permits the solder to wet the surfaces to be joined

3.2.21 glass meniscus

glass fillet of a lead seal which occurs where an external lead leaves the package body

NOTE These can be described as either functional, where an active track is terminated, or non-functional, where the pad is isolated.

3.2.22 modal survey

characterization of the dynamic properties of systems in the frequency domain

NOTE A typical example is testing structures under vibrational excitation

3.2.23 outsourcing

act of subcontracting work to another company in compliance with customer PID

3.2.24 pits

small holes or sharp depressions in the surface of solder

NOTE This can be caused by flux blow-out due to entrapment or overheating.

3.2.25 potting compound

compound, usually electrically non-conductive, used to encapsulate or as a filler between components, conductors or assemblies

3.2.26 pressfit connector

solderless termination technology where each contact is pressed into a plated hole of a printed circuit board creating a mechanical and electrical joint

3.2.27 reprocessing

preparatory operation done on a component prior to assembly

NOTE Degolding, pretinning, lead forming and cutting are examples of reprocessing.

3.2.28 shield

metallic sheath surrounding one or more wires, cables, cable assemblies, or a combination of wires and cables that is used to prevent or reduce the transmission of electromagnetic energy to or from the enclosed conductors

NOTE The shield also includes an insulating jacket that can cover the metallic sheath.

3.2.29 solder balls

numerous spheres of solder having not melted in with the joint form and being scattered around the joint area normally attached by flux residues

NOTE Can be caused by incorrect preheating or poor quality solder.

3.2.30 solder-cup terminal

hollow, cylindrical terminal closed at one end to accommodate one or more conductors

3.2.31 solder icicle

conical peak or sharp point of solder usually formed by the premature cooling and solidification of solder upon removal of the heat sources

3.2.32 solder pad

conductive surface on a printed circuit board to which terminations are soldered to form electrical connections

3.2.33 solder stand-off

thickness of solder between the underside of the component termination and the solder pad

3.2.34 split terminal

see "**bifurcated terminal**" 3.2.3

3.2.35 staking

application process of adhesive on the outside of a package for mechanical purpose

3.2.36 stress relief

method or means to minimize stresses to the soldered termination or component

NOTE Generally, in the form of a bend or service loop in a component lead, solid or stranded wire to provide relief from stress between terminations, as that caused, for instance by movement or thermal expansion.

3.2.37 stud termination

upright conductor termination through a printed circuit board

3.2.38 technology samples

samples of boards assembled with representative technology

3.2.39 thermal shunt

component with good heat-dissipation characteristics used to conduct heat away from an article being soldered

3.2.40 turret terminal

round post-type grooved stud around which conductors are fastened before soldering

3.2.41 underfill

material deposited between a component and substrate

3.2.42 verification board

substrate assembled with components subjected to a verification programme

3.2.43 wicking

flow of molten solder or cleaning solution by capillary action

NOTE Occurs when joining stranded wire; solder is drawn within the strands, but normally not visible on outer surface of strands. Wicking can also occur within the stress relief bend of a component lead.

3.3 Abbreviated terms

For the purpose of this Standard, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
AAD	area array component NOTE: also known as "area array device".
AOI	automatic optical inspection
AWG	American wire gauge
BGA	ball grid array
CBGA	ceramic ball grid array
CCGA	ceramic column grid array
CGA	column grid array
CLCC	ceramic leaded chip carrier
CTE	coefficient of thermal expansion
DCL	declared component list
DIL	dual in line
DIP	dual in line package
DPAK	diode package
DRD	document requirement definition
ETFE	ethylene tetrafluoroethylene
EPA	ESD protected area
ESD	electrostatic discharge

Abbreviation	Meaning
FEP	fluorinated ethylene propylene
FM	flight model or flight hardware
FP	flat pack package
JEDEC	Joint Electron Component Engineering Council
LCCC	leadless ceramic chip carrier
MELF	metal electrode face bonded NOTE: Also known as "minimelf" or "micromelf"
MIP	mandatory inspection point
MRR	manufacturing readiness review
PCB	printed circuit board
PLCC	plastic leaded chip carrier
PID	process identification document
PSD	power spectral density
PTFE	polytetrafluoroethylene
PTH	plated though hole component
QFN	quad flat pack no leads
QFP	quad flat pack
R_g	resistance to ground
R_s	surface resistance
r.m.s.	root-mean-square
SIR	surface insulation resistance
SMD	surface mounted component
SMT	surface-mount technology
SO	small outline
SOD	small outline diode
SOT	small outline transistor
SOP	small outline package
TO	transistor outline
TRB	test review board
TRR	test readiness review
TSOP	thin small outline package
RF	radio frequency

3.4 Nomenclature

The following nomenclature apply throughout this document:

a. The word “shall” is used in this document to express requirements. All the requirements are expressed with the word “shall”.

b. The word “should” is used in this document to express recommendations. All the recommendations are expressed with the word “should”.

NOTE It is expected that, during tailoring, all the recommendations in this standard are either converted into requirements or tailored out.

c. The words “may” and “need not” are used in this document to express positive and negative permissions respectively. All the positive permissions are expressed with the word “may”. All the negative permissions are expressed with the words “need not”.

d. The word “can” is used in this document to express capabilities or possibilities, and therefore, if not accompanied by one of the previous words, it implies descriptive text.

NOTE In ECSS “may” and “can” have a completely different meaning: “may” is normative (permission) and “can” is descriptive.

e. The present and past tense are used in this document to express statement of fact, and therefore they imply descriptive text.

4
Principles of reliable soldered connections

The following are the general principles to provide reliable soldered connections:

- Reliable soldered connections are the result of proper design, control of tools, materials, processes and work environments, and workmanship performed in accordance to verified and approved procedures, inspection control and precautions.
- The basic design concepts to provide reliable connections and to avoid solder joint failure are as follows:
  - Stress relief is an inherent part of the design, which reduces detrimental thermal and mechanical stresses on the solder connections.
  - Where adequate stress relief is not possible materials are so selected that the mismatch of thermal expansion coefficients is a minimum at the constraint points in the component mounting configuration.
- The assembled substrates are designed to allow easy inspection, rework and repair.
- Soldering to gold using tin-lead alloy can cause failure.

5
Preparatory conditions

5.1 Calibration

a. Calibration status of tools and inspection equipment shall be verified according to clause 17.4.

b. Records of the calibration and verification of the tools and inspection equipment shall be maintained.

5.2 Facility cleanliness

a. Personnel facilities shall be separated from the soldering areas.

NOTE Example: Washrooms, eating areas, smoking facilities.

b. Furniture shall be arranged to allow thorough cleaning of the floor.

c. Areas used for soldering shall be kept free from contaminants.

NOTE Loose material such as dirt, dust, solder particles, oil or clipped wires can contaminate soldered connections.

d. Working areas shall be kept free from any tools or equipment not used for the current task.

e. Working surfaces shall be covered with an easily-cleaned hard top or have a replaceable surface of clean, non-corrosive, silicone-free paper.

f. Tools used during soldering operations shall be free of visible contaminant.

g. Excess lubricants shall be removed from tools before soldering starts.

5.3 Environmental conditions

a. The clean room shall be compliant to the requirements of clause 5.3.1 of ECSS-Q-ST-70-01.

b. The soldering area shall have as minimum a cleanliness level of ISO Class 8.2 in accordance with ISO 14644-1 (2015).

c. Areas used for assembly or cleaning of parts and areas where toxic or volatile vapours are generated or released shall include a local air extraction system.

d. The room temperature of the facility shall be maintained at (22 ±3) °C.

e. The relative humidity at room temperature of the facility shall be maintained at (55 ±10) %.

f. The soldering area shall not be exposed to draughts.

g. Air shall be supplied to the room through a filtering system that provides a positive pressure difference with respect to adjacent rooms.

5.4 Lighting requirements

a. Lighting intensity shall be a minimum of 1080 lux on the work surface.

b. At least 90 % of the work area shall be without shadows or severe reflections.

5.5 Precautions against static discharges

5.5.1 Overview

Electronic components are particularly sensitive to electrostatic charging and discharging. To protect these components, it is necessary to define measures with regard to their handling, transport and storage.

The ESD control programme helps reducing to a minimum level the ESD-related damage to components. Main topics of the programme are:

- Training,
- Product qualification,
- Compliance verification,
- Grounding/bonding systems,
- Personnel grounding,
- EPA requirements,
- Packaging systems,
- Marking.

The controls referenced in this document have been selected to prevent from damages the ESD sensitive devices (ESDS) which are susceptible to discharges of greater than or equal to 100 V (Human Body Model) or 200 V (Charged Device Model).

5.5.2 General

a. An ESD Control Programme in accordance with EN 61340-5-1 (2016) shall be developed and implemented by the supplier.

NOTE EN 61340-5-2 guideline can be used for editing the ESD Control Programme.

b. The process for the selection of new parts shall take in account the ESD sensitivity of the parts.

c. ESD sensitive devices shall require additional measures.

d. Electrostatic sensitive components shall be handled prepared, mounted, soldered and cleaned in an ESD protected area.

e. Electrostatic sensitive components shall be kept as shipped until assembly preparation.

NOTE For example, kept in the anti-static tubes or foam.

f. Containers for ESD sensitive components shall be labelled as such.

5.5.3 ESD Protected Area

a. ESD sensitive devices shall be assembled in an EPA.

b. As a minimum, a dissipative mat, a wrist strap and common grounding facility for both shall be in place in the EPA.

c. EPA areas shall be visibly marked as such.

d. ESD rules and regulations shall apply as specified in EN 61340-5-1 (2016).

e. If the measured electrostatic field or surface potential exceeds the stated limits, ionization or other charge mitigating techniques shall be used.

f. Relative Humidity shall be controlled in the EPA in accordance with requirement 5.3e.

5.5.4 Precautions against ESD during manufacturing

a. Delimited EPA and corresponding ESD control items shall be in compliance with Table 5-1.

b. Ionized air in presence of high voltage or RF shall not be used.

NOTE Static charges on isolated parts or tooling can be dissipated using ionised air.

c. A wrist strap shall be worn by the operator.

d. Powered equipment at the work station shall be grounded.

e. The normal value of the resistance between the tip of the soldering system and the ground of the ESD protected area shall not exceed 5 Ω.

NOTE The measurement is generally performed at soldering temperature.

f. A ground-fault circuit interrupter shall be installed.

g. Protective clothing shall be made from static dissipative material.

h. Gloves and finger cots shall be made from static dissipative material.

i. Tools, such as mounting aids, consumables, masking tape, shall be conductive or static dissipative.

j. Paperwork accompanying ESD sensitive components shall be contained in static dissipative bags or envelopes.

NOTE Example of accompanying paperwork are traveller logs, drawings and instructions.

k. Paperwork shall not come into contact with ESD sensitive components.

Table 5-1: EPA requirements summary

ESD Control item		**Limits values *** (unit: Ω)
Working surfaces, storage, racks and trolleys	Dissipative top surface	$R_s < 1 \times 10^9$
	ESD protected to ground	$R_g < 1 \times 10^9$
Flooring	ESD protected to ground	$R_g < 1 \times 10^9$
Ionization		Decay (1000 V to 100 V) in less than 20 s Offset voltage ± 35V
Seatings	ESD protected to ground	$R_g < 1 \times 10^9$
Wrist strap	ESD protected to ground	$R_g < 5 \times 10^6$
* Values are taken from Table 3 of EN 61340-5-1:2016.		

5.5.5 Protective packaging and ESD protection

a. All ESD-sensitive items shall be contained within ESD-protective containers for movement between and within ESD-protected areas.

b. ESD protective packaging shall display ESD warning signs.

c. If the packaging is not ESD safe, it shall be labelled accordingly.

NOTE The objective of ESD protection is to prevent ESD to the item contained within, to allow for dissipation of charge, and to prevent charging of the ESD item by an external electrostatic field.

d. A container providing mechanical and ESD protection shall be used, whenever the ESD-sensitive electronic assembly is transported within a manufacturing plant or during shipment to external destinations.

NOTE This can be achieved by a container with:
- an outer shell that provides adequate mechanical protection for the contents;
- foam or bubble wrap shock absorbing liners that have static shielding covers;
- shielding package for the ESD sensitive contents.

e. All static-shielding bags shall be metallized.

f. Bags, film, bubble wrap or foam of Pink-Polyethylene shall not be used near any ESD-sensitive item or within an ESD protected area.

NOTE Pink-polyethylene (pink-poly) provides little protection against ESD events and voltage fields and is a contaminants source.

g. Shipping popcorn, foam liners and polystyrene foam shall not be used near ESD-sensitive items unless shielding overwrap protects them.

5.6 Equipment and tools

5.6.1 General

a. Any equipment and tools shall be inspected in order to meet requirements from clause 17.4.

b. Equipment shall not generate, induce or transmit electrostatic charges to components being placed.

c. Any machine or part of machine, in particular the conveyor, shall be grounded in order to avoid electrostatic discharge.

d. Machines and equipment used to solder surface mount components shall either be a type incorporating dynamic single or dual solder wave or be of the solder reflow type.

e. The supplier shall verify that the soldering conditions of assembly equipment comply with the values given by the individual component data sheets.

NOTE Examples of soldering conditions include maximum temperature to avoid internal melting, thermal shocks, thermal damages, removal of marking ink, degradation of encapsulating plastic.

f. Temperature and time profiles for assembly shall be identified by the supplier and approved by the Approval Authority.

g. The supplier shall identify changes and implement a verification programme in compliance with the requirements from clause 13.

h. The supplier shall demonstrate the reproducibility of their processes.

5.6.2 Brushes

a. Medium-stiff natural- or synthetic bristle, ESD-safe, brushes shall be used for cleaning provided that they do not damage any surface to be cleaned or adjacent materials.

b. Brushes shall be cleaned in a solvent in accordance with clause 6.4.

c. Brushes shall not be damaged by the solvents used for PCB cleaning.

d. Wire brushes shall not be used.

5.6.3 Cutters and pliers

a. Cutting edge profiles and cutter usage shall be in accordance with Figure 5-1.

b. The cutter used for trimming conductor wire and component leads shall shear sharply, producing a clean, flat, smooth-cut surface along the entire cutting edge.

NOTE 1 These measures minimize the transmission of mechanical and shock loads to delicate parts.

NOTE 2 Smooth, long-nose pliers or tweezers can be used for attaching or removing conductor wires and component leads.

c. No twisting action shall occur during the cutting operation.

d. Cutting edges shall be checked for damage and maintained in a sharp condition.

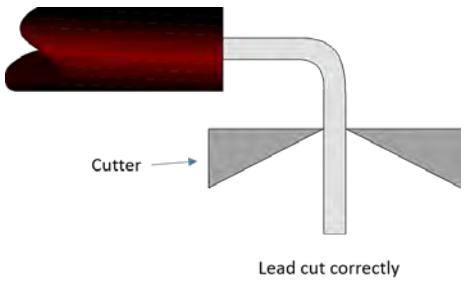


Figure 5-1: Profile of correct cutters for trimming leads

5.6.4 Bending tools

a. Bare component leads shall be bent or shaped using tools, including automatic bending tools, which do not nick or damage the leads or insulation.

b. Components shall not be damaged by the bending process (see also clause 8.2.9.

NOTE It is good practice to use bending tools with polished finish. The preferred surface finish for shaping tools is hard chromium plating.

c. Bending tools shall have no sharp edges in contact with the component leads.

5.6.5 Clinching tools

a. Clinching tools shall not damage the surfaces of printed-circuit conductors, components or component leads.

5.6.6 Insulation strippers

5.6.6.1 Thermal strippers

a. The temperature of the stripper shall not burn, blister or cause excessive melting of the insulation.

NOTE 1 Thermal insulation strippers can be used for wire insulation types susceptible to damage by mechanical strippers.

NOTE 2 It is good practice to apply thermal strippers for use with AWG 22 and smaller wire sizes where there is a possibility of the wire stretching if a mechanical stripper is used.

NOTE 3 Local air extraction units can be used during thermal stripping.

5.6.6.2 Precision mechanical cutting-type strippers

a. Mechanical strippers shall be of the following types:

1. Automatic power-driven strippers with precision, factory-set, cutting and stripping dies and wire guards, or
2. Precision-type hand strippers with accurately machined and factory-pre-set cutting heads.

NOTE Figure 5-2 shows an example of acceptable mechanical strippers.

b. Stripping tools or machines shall fit the size of the wire conductor.

NOTE It is good practice to mask off the die openings for wire sizes not in use.

c. The conductor shall not be twisted, ringed, nicked, cut or scored by the process.

Figure 5-2: Example of approved mechanical strippers

5.6.6.3 Enamel stripping

a. The enamel shall be removed by chemical or thermal means.

b. The enamel may be removed by mechanical means provided that visual inspection using a minimum magnification of x40 is carried out to undamaged the conductor.

c. When stripping the ends of enamel wires the complete removal of the enamel shall be verified by visual inspection.

d. Chemical stripping materials shall be completely neutralised and be cleaned such that there are no residues from the stripping, neutralizing, or cleaning steps.

e. The enamel shall not be visually contaminated by the stripping process.

5.6.6.4 Verification of stripping tools

a. Thermal and mechanical stripping tools shall be verified by sampling at the start of each production batch.

5.6.7 Hot air blower

a. Hot air blower may be used for shrinking of sleeves and removal of some adhesives

b. Hot air blower shall be temperature monitored

c. Hot air blower shall meet requirement 5.6.1c against ESD

5.6.8 Soldering tools

5.6.8.1 General

a. The leads shall not be damaged during preparation and assembly.

5.6.8.2 Holding tools

a. Holding tools used as soldering aids shall not be wetted by the solder during the assembly.

5.6.8.3 Thermal shunts

a. Thermal shunts shall be used for the degolding, pretinning and soldering of temperature-sensitive components.

NOTE An effective clamp-type thermal shunt can be constructed by sweating small copper bars into the jaws of an alligator clip.

b. The heat sink shall be used when the non-thermal sensitivity of the device cannot be demonstrated.

c. The thermal shunt shall not disturb the solder joint by mechanical interference.

d. Shunts shall be applied and removed without mechanically damaging the component or the assembly.

NOTE Shunts can be held in place by friction, spring tension or any other means that does not damage the finish or insulation.

5.6.8.4 Anti-wicking tools

a. The conductor gauge sizes of the anti-wicking tools shall be marked on the tool.

NOTE Anti-wicking tools can be used for pretinning the stranded wires.

5.6.8.5 Soldering irons

a. The size and shape of the soldering iron and tip shall not damage adjacent areas or connections during soldering operations.

b. Temperature-controlled soldering irons shall be used.

c. Temperature of the solder tip shall be verified once a week and after each solder tip change.

d. Selected temperature of the solder tip shall remain within +/-10°C.

e. Files shall not be used for dressing plated copper soldering-iron tips.

f. A selection of tip sizes and shapes appropriate to each soldering operation envisaged shall be available.

g. Thermal shunts, as specified in 10.2.2a, shall be used to protect thermally-sensitive components.

h. A soldering iron holder shall be used.

NOTE It is good practice to use a cage-type holder that leaves the soldering-iron tip unsupported when a temperature-controlled soldering iron is used.

i. For soldering of electronic components, the soldering-tip temperature shall be between 280 °C and 340 °C.

NOTE Based on the component manufacturer's recommendations, solder iron can be

substituted by applying, for instance, hot air in order to avoid thermal shock.

j. A soldering tip temperature lower than 280 °C may be used for thermal sensitive components.

k. A soldering tip temperature up to 380 °C may be used for polyimide PCBs with heat sinks, wide tracks or ground planes.

l. In order to improve solder flow, by order of preference, the following actions shall be taken into account:

1. Select proper solder tip and solder equipment power,
2. Introduce preheating of assembly,
3. Increase preheating temperature,
4. Increase solder temperature.

5.6.9 Baking and curing ovens

a. An oven shall be used to bake out PCBs in compliance with requirements from clause 7.7.

b. An oven used for silicone shall not be used to bake out PCBs.

c. An oven used for silicone shall not be used to cure adhesives other than silicone.

d. The oven shall be equipped with an independent automatic shutdown system to protect from overheating.

5.6.10 Solder deposition equipment

a. Equipment used to deposit solder pastes shall be of a screening, stencilling, dispensing, roller coating, dotting or jet printing type.

b. Equipment shall apply pastes of a viscosity and quantity such that the positioned component is retained on the board before and during soldering operations, ensuring self-centring and solder fillet formation.

c. Equipment used to apply solder preforms shall align the preform with the land or component lead and termination.

5.6.11 Automatic component placement equipment

a. Automatic or computer-controlled equipment used for component placement shall be of the coordinate-driven pick-and-place type or of the robotic type.

b. The placement equipment used shall be of a type that:

1. prevents component or board damages,
2. indexes components with respect to the circuit and
3. aligns the component leads or castellation with the board terminal areas

5.6.12 Dynamic wave-solder machines

a. Dynamic soldering machines shall be of automatic type and of a design offering the following:

   1. Controlling the flux application.
   2. Controlling preheating to drive off volatile solvents and to avoid thermal shock damage to the PCB and component packages.
   3. Maintaining the solder temperature at the printed circuit board assembly to within ±5 °C of the established bath temperature throughout the duration of any continuous soldering run when measured 3,0 mm below the surface of the wave.
   4. Having a wave system that limits shadowing and allows solder fillet formation.
   5. Having carriers made from a material that cannot contaminate, degrade or damage the printed circuit board or substrate nor transmit vibration or shock stress from the conveyors to a degree permitting physical, functional or electrostatic damage to components, board or substrate during transport through preheating, soldering and cooling stages.
   6. Showing an extraction system, either integral or separate, conforming to the requirements of clause 5.3a.

      NOTE to item 4: It is good practice to use nitrogen atmosphere.

b. The following wave soldering machine parameters shall be controlled:

   1. the amount of flux and its coverage,
   2. the preheat temperature to avoid damage to the PCB and to the component packages,
   3. the solder temperature so that the solder in the wave making contact with the board is 235 °C to 275 °C.

c. The supplier shall provide evidence that:

   1. the assembled board does not become contaminated before being loaded on the carrier,
   2. the conveyor speed does not vary by more than ±5 %, and
   3. the height of the solder wave to a constant pre-selected value across the width of the wave.

5.6.13 Selective wave solder equipment

a. Selective wave soldering machines shall be of automatic type and of a design offering the following:

   1. A holding mechanism for the board to be soldered, which can fixate the board during the process, without degrading or damaging the PCB or the mounted components.

2. Nozzle, through which a local solder wave applies solder selectively per component or termination, from the solder side of the PCB to the component leads to be soldered.
3. Automatic relative movement between nozzle and PCB both in-plane and out-of-plane direction.
4. Controllable flux application.
5. Maintain the preheating temperature to within ±5 °C during soldering to avoid thermal shock damage to the PCB and to component packages.
6. Maintaining the wave solder temperature to within ±5 °C of the established soldering temperature throughout the process.
7. Showing an extraction system, either integral or separate, conforming to the requirements of clause 5.3.

NOTE to item 2: It is good practice to use local flow of nitrogen around the solder nozzle.

b. The following selective wave soldering machine parameters shall be controlled:
   1. the amount of flux and its coverage,
   2. the preheat temperature,
   3. the solder temperature so that the solder in the selective wave making contact with the board is maximum 300 °C,
   4. the nozzle speed so that the soldering time per lead does not exceed 10 s.

5.6.14 Condensation (vapour phase) reflow machines

a. Condensation reflow machines shall:
   1. not transmit a movement or vibration into the assemblies being soldered that result in misalignment of components or disturbed solder joints,
   2. be capable of preheating an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering,
   3. use a reflow fluid whose boiling point is a minimum of 12 °C above the melting point of the solder being used,
   4. maintain the preselected temperature to within ±5 °C in the reflow zone during soldering,
   5. include an extraction system that conforms to clause 5.3.

5.6.15 Local hot gas reflow machines

a. Local hot gas reflow machines shall:

1. not transmit movement or vibration to the assemblies being soldered which result in misalignment of components or disturbed solder joints,
2. preheat an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering,
3. heat the area of the assembly to be soldered using focused or unfocussed energy, to a preselected temperature that is a minimum of 12 °C above the melting point of the solder being used as measured at laminate or substrate surface,
4. prevent the reflow of adjacent components,
5. maintain the preselected reflow temperature within ±5 °C as measured at the substrate surface.

5.6.16 Forced convection and infrared reflow systems

a. Forced convection and infrared reflow machines shall be of design such that the system:

1. provides a controlled temperature profile and does not transmit movement or vibration into the assembly being soldered,
2. preheats an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering,
3. heats the area of the assembly to be soldered using focused or unfocussed energy, to a preselected temperature that is a minimum of 12 °C above the melting point of the solder being used as measured at laminate or substrate surface,
4. maintains the preselected temperature to within ±5 °C in the reflow zone during soldering.

5.6.17 Other equipment for reflow soldering

a. Other solder reflow systems may be approved for use by the Approval Authority under the condition that they meet the requirements of either clause 5.6.14, 5.6.15 or 5.6.16.

5.6.18 Cleanliness testing equipment

a. Cleanliness testing equipment shall be able to:

1. test the cleanliness of bare and assembled printed circuit boards,
2. have the capability to measure requirement from clause 11.1.3.3a,
3. meet the requirements of IPC-TM-650 Method 2.3.25.

5.6.19 Automatic Optical Inspection (AOI) equipment

a. AOI shall not replace final visual inspection.

NOTE AOI is an aid for inspection.

b. AOI equipment should be capable of detecting the following defects:

1. Missing component
2. Wrong type of component
3. Wrong polarization
4. Component upside down
5. Misplacement
6. Tombstoning or component placed on its edge
7. Lack of solder.

5.6.20 X-ray inspection equipment

a. The maximum dose during X-ray inspection shall be less than 5 % of the eligible dose of the most sensitive component according to its specification.

b. X-ray equipment shall be calibrated in order to evaluate the total dose received by the components during the inspection.

NOTE In order to minimize the dose given to the component, it is good practice to:

- Record the total dose received.
- Use off-line image analysis as much as possible.
- Use filters, optimizing the direction of the X-ray beam and masking sensitive areas.

c. The resolution of the X-ray equipment shall be able to detect solder balls having a diameter of 0,03 mm.

d. The sensitivity shall be demonstrated by means of actual 0,03 mm diameter solder balls, stuck to adhesive tape, attached to the multilayer board assembly being inspected.

6
Material selection

6.1 General

a. Material selection shall be performed in accordance with ECSS-Q-ST-70-71 and ECSS-Q-ST-70.

b. Components, subassemblies, assemblies and hardware for space flight applications shall not have tin finishes containing more than 97 % tin.

c. Electrical and electronic components identified as having plated or metallized external surfaces with a tin finish containing more than 97 % tin shall be pretinned with a tin-lead solder in accordance with clause 7.3.4.1.

NOTE Tin whisker mitigation (barrier methods such as coating or sleeving) is addressed in the framework of an NRB or to the Approval Authority.

d. Pretinning shall not degrade or damage the component.

e. Operations carried out during degolding or pretinning shall not contravene the individual detailed specification for the component, PCB and terminations.

6.2 Solder

6.2.1 Form

a. For soldering, solder paste, ribbon, wire and preforms shall be used provided that the alloy and flux meet the requirements of this standard.

b. Alloy for use in solder baths, for degolding, pretinning and wave, shall be supplied without flux and be compliant with the requirements of Table 6-1.

NOTE Bars and ingots are example of procured alloys.

6.2.2 Composition

a. The solder alloy shall have a composition specified in Table 6-1.

NOTE 1 Complementary information can be found in EN-IEC 61190-1-3 for solder and EN-IEC 61190-1-2 for solder paste.

NOTE 2 The solder alloy used depends upon the application. See Annex G for guidelines for the choice of solder type.

b. In case Indium Lead, Sn96 and Sn10 solders are used for plated through holes soldering, a verification shall be performed in compliance with clause 13.

6.2.3 Solder paste

a. The metal purity shall be as specified in Table 6-1.

Table 6-1: Chemical composition of spacecraft solders

ESA designation		Sn min % - max %	Pb max %	In min % – max %	Sb max %	Ag min % – max %	Bi max %	Cu max %	Fe max %	Zn max %	Al max %	As max %	Cd max %	Other max %
PTH and SMD assembly applications														
63 Tin solder Sn63		62,5-63,5	remainder	-	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
62 Tin Silver loaded Sn62		61,5-62,5	remainder	-	0,05	1,8-2,2	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
60 Tin solder Sn60		59,5-61,5	remainder	-	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
Only for SMD assembly applications														
96 Tin solder Sn96		remain	0,10	-	0,05	3,5-4,0	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
75 Indium Lead In75		max 0,25	remainder	74,0-76,0	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
70 Indium Lead In70		0,00-0,10	remainder	69,3-70,7	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
50 Indium Lead In50		0,00-0,10	remainder	49,5-50,5	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08

6.2.4 Maintenance of paste purity

a. When purchased premixed or mixed in house, the purity of solder paste shall be maintained.

b. Manufacturers' instructions shall be applied for the handling and storage of containers of solder paste purchased premixed.

c. Refrigerated solder paste shall reach room temperature before opening the container.

d. Neither paste purchased premixed nor paste mixed in-house shall be used if the use-by date or shelf life recommended by the manufacturer of the paste or paste constituents has expired.

e. When the solder paste's shelf life has expired it shall not be used unless:

1. Relifing is performed,
2. tests that include visual inspection and viscosity measurements, according to the manufacturer's recommendations, are passed successfully.

f. When relifing is performed, and the material passes the specified tests, the new shelf life shall be half the initial shelf life.

g. Tools used for removing solder paste from the container shall not contaminate the paste dispensed or that remaining within.

6.3 Flux

6.3.1 Rosin based fluxes

a. Fluxes shall be selected in accordance with Table 6-2.

NOTE 1 Complementary information can be found EN-IEC 61190-1-1 for flux.

NOTE 2 Fluxes manufacturers are mainly in compliance with IPC J-STD-004A (2004).

b. For the pretinning of component leads, metallised terminations and terminal posts low activated, rosin-based fluxes shall be used.

NOTE ROL0 or ROL1 are types of flux compliant to the requirement.

c. When pretinning with low activated rosin-based flux does not give acceptable wetting, moderate or high activated rosin-based fluxes may be used.

NOTE ROH1 flux is extremely aggressive and can cause corrosion and damage to electronic materials.

d. For assembly the following fluxes shall be selected:

1. For normal assembly, use ROL0 pure rosin flux.
2. When low activated rosin flux is used, monitor the effectiveness of subsequent cleaning operations in accordance with clause 11.1.3.

NOTE Example: low activated rosin flux ROL1.

e. High activated rosin-based fluxes shall be stored separately from pure rosin fluxes and low activated rosin fluxes.

NOTE Example: High activated rosin flux ROH1.

Table 6-2: Fluxes

	IPC J-STD-004A designation	**Equivalent designation from ISO 9454-1:2016**	**Nature**	**Max composition*** (Weight %)
Pretinning				
Normal wetting	ROL0	1111	Rosin	< 0,05 % halide
	ROL1	1122	Rosin	< 0,5 % halide
Difficult wetting	ROM1	1123	Rosin	0,5 % – 2 % halides
Difficult wetting	ROH1	1124	Rosin	≥ 2,0 % halides
Assembly				
Preferred	ROL0	1111	Rosin	< 0,05 % halide
Requiring cleanliness testing	ROL1	1122	Rosin	< 0,5 % halide
* Maximum values of halide contents are from IPC that are above max values of ISO.				

6.3.2 Application of flux

a. The quantity of flux used shall be such that the solder joint is in accordance with clause 12.

b. When flux-cored solder is used, it shall be positioned such that the flux flows and covers the components to be joined as the solder melts.

c. When an external liquid flux is used in conjunction with flux-cored solders, the fluxes shall be compatible.

d. When external flux is used, liquid flux shall be applied to the surfaces to be joined prior to the application of heat.

6.3.3 Flux controls for wave-soldering equipment

a. A controlled method shall be established and implemented for wave-soldering machines such that the flux is not contaminated with remaining residues from previous non-space works.

b. All fluxes properties shall be controlled and results recorded prior to soldering.

NOTE 1 e.g. specific gravity.

NOTE 2 This is to avoid variations from the optimum.

c. All fluxes, machine oils and ionisable contaminants on the assembly shall be removed within one hour of the wave soldering operation.

d. Dross (oxides) from the solder bath shall be removed so that dross does not mix with the liquid solder.

NOTE Automatic or manual processes are acceptable, provided that the dross does not come in contact with the PCB assembly during any portion of the soldering process.

e. Dross removal material that melt, dissolve or alloy with the liquid solder and flux shall not be used.

6.4 Solvents

a. Solvents for the removal of grease, oil, dirt, flux and flux residues shall be electrically non-conductive and non-corrosive.

b. Solvents shall not dissolve or degrade the quality of parts or materials.

c. Solvents shall not remove component identification markings.

d. Containers of solvents shall be labelled.

e. Solvents shall be maintained in an uncontaminated condition.

f. Solvents showing visual evidence of contaminants or decomposition shall not be used.

g. Solvents shall not be used such that dissolved flux residue contaminates electrical contact surfaces.

NOTE Examples of electrical contact surfaces are those in switches, potentiometers or connectors.

h. The following solvents shall be used for cleaning in soldering operations:

1. ethyl alcohol, 99,5 % pure or 95 % pure by volume,
2. isopropyl alcohol, 99 % pure,
3. deionized water at a maximum temperature of 40 °C is used for removing certain fluxes provided that the assembly is thoroughly dried directly after cleaning,
4. any mixture of 6.4h.1, 6.4h.2 and 6.4h.3.

i. Other solvents that pass a compatibility test programme agreed by the Approval Authority may be used.

j. Water-based solvents containing saponifiers shall not be used.

k. Solvents shall be selected such that they dry completely.

6.5 Flexible insulation materials

a. Materials shall have low outgassing properties in accordance with clause 5.5 of ECSS-Q-ST-70-02.

b. The following flexible insulation materials may be used in a space environment:

1. ETFE, FEP and PTFE.
2. Polyolefin and PVDF (Kynar®) sleeving for heat-shrinkable wire terminations.

3. Irradiated polyethylene, fluorinated resin and polyimide.

c. PTFE materials shall not be heated above 250 °C.

NOTE Poisonous gases can be liberated above this temperature.

6.6 Terminals

6.6.1 Materials

a. Terminals shall be made from one of the following materials:

1. Bronze (copper-tin) alloys.
2. Brass (copper-zinc) alloys.

NOTE It is good practice to use bronze terminals.

b. When a brass terminal is used it shall be plated with a barrier layer of copper or nickel of 3 µm to 10 µm.

NOTE 1 A barrier layer is necessary on brass items to prevent the diffusion, and subsequent surface oxidation, of zinc.

NOTE 2 It is good practice to use a copper barrier layer on brass terminals because nickel is magnetic and can have a poor solderability.

c. Terminals shall be tin-lead plated with an alloy containing a maximum of 97 % tin.

NOTE Example: Hot-dipped or reflowed electro-deposited platings.

d. Terminals with platings on the mounting surface shall be rejected if the platings loosen in subsequent soldering operations.

6.6.2 Tin, silver and gold-plated terminals

a. Terminals with pure tin, silver or gold-plated finish shall not be soldered to PCB.

b. Pure tin or gold-plated finishes shall be replaced using one of the methods described in clause 7.3.

c. The maximum gold thickness of the terminal shall be specified in the procurement specification.

d. Silver finish shall be pretinned according to clause 7.3.4.

6.7 Wires

a. Wire shall be made from high-purity copper or copper alloy.

b. The wire shall have one of the following finishes:

1. Silver-plating of a minimum 2 µm thickness,
2. Wire-drawn, fused pure tin,
3. Enamelled.

c. Wires shall be stripped of their insulation in accordance with clause 7.2.1.

d. Wires shall be pretinned

6.8 Sculptured flex

a. Sculptured flex shall be designed in conformance with the requirements of clause 8.7 of ECSS-Q-ST-70-12.

b. Sculptured flex shall be manufactured and procured according to the requirements of ECSS-Q-ST-70-60.

6.9 Printed circuits substrates

6.9.1 Substrates selection

a. PCBs shall be designed in conformance with the requirements of clause 14 of ECSS-Q-ST-70-12.

b. PCBs shall be manufactured and procured according to the requirements of ECSS-Q-ST-70-60.

c. Ceramic substrates shall meet the requirements of ECSS-Q-ST-60-05.

d. Verification from clause 13 shall be valid for material type groups in Table 6-1 from ECSS-Q-ST-70-12.

6.9.2 Gold finish on PCBs footprint

a. Degolding of pads shall be performed in accordance with clause 7.3.

NOTE RF circuits with gold finishes (see Table 10-13 of ECSS-Q-ST-70-60) can have their pads selectively plated with a tin-lead finish.

b. Soldering to gold finish with tin lead may be performed only when the gold finish is thinner than 0,1 μm and is approved by the Approval Authority.

6.10 Components

6.10.1 General

a. Components lead materials and their finishes shall be selected in compliance with requirements from clause 3 of ESCC23500.

NOTE ESCC 23500 is only applicable for procured components and the pre-assembly operations as degolding and pretinning are out of its scope.

b. In case of not golden termination finish, the lead finish shall be checked as per ESCC 25500 in accordance with requirement 4.3.7b.1(f) from ECSS-Q-ST-60.

c. Components shall be capable of withstanding cleaning processes currently used in space projects.

d. Components with Silver Palladium finish shall not be used.

e. Reprocessing shall not damage the component.

f. Gold plated terminations of component shall be degolded and pretinned in compliance with clause 7.3.

g. Degolding for gold finishes of thickness less than 0,1 µm may be omitted subject to agreement by the Approval Authority.

h. Pretinning of ceramic chip capacitors shall not be performed.

i. Type II chip ceramic capacitors shall not be reworked.

j. If components initially designed for insertion-mount application are used for surface mounting, they shall be of a type that can be surface-mount adapted.

k. The adaptation specified in the requirement 6.10.1j shall not functionally or physically degrade the component or the substrate to which the adapted component is attached.

l. Connectors shall be of a configuration incorporating either male or female quick-disconnect contacts and stress relief provision for the soldered connection of each individual contact when such connections are completed.

6.10.2 Moisture sensitive components

a. Moisture sensitive components shall be stored and handled in conformance with the component manufacturer's recommendations.

NOTE Many types of plastic encapsulated components, particularly some plastic BGAs, are moisture sensitive.

b. When moisture sensitive components are used, bake out shall be performed in accordance with clause 7.8.

6.11 Adhesives, potting, underfill and conformal coatings

a. Adhesives shall be dispensable, non-stringing, and have a reproducible dot profile after application.

b. Adhesives, pottings, underfill and conformal coatings shall conform to the outgassing requirements of ECSS-Q-ST-70-02.

c. Materials covered by this clause shall be individually assessed in accordance with clause 5.2.7 of ECSS-Q-ST-70-71, when flammability requirements are applicable.

d. No materials that emit acetic acid, ammonia, amines, hydrochloric acid and other acids shall be used.

NOTE Such compounds can cause stress-corrosion cracking of part leads

e. Limited shelf life items shall be stored and controlled in accordance with the material manufacturer's recommendations or in accordance with the

manufacturer's documented procedures for controlling shelf life and shelf life extensions where permitted.

7
Preparations prior to mounting and soldering

7.1 General

7.1.1 Tools

a. Operators shall use tools that are fit for the purpose and undamaged prior to use.

7.1.2 Components

a. The supplier shall verify that degolding, pretinning and soldering conditions do not exceed the values given by the individual component data sheets.

7.2 Preparation of components, wires, terminals and solder cups

7.2.1 Insulation removal

7.2.1.1 Stripping tools

a. Stripping tools or machines shall be in accordance with clause 5.6.6.

7.2.1.2 Damage to insulation

a. The remaining conductor insulation shall not be damaged by the insulation removal process.

b. Conductors with damaged insulation shall not be used.

NOTE 1 Example: Insulation damage includes nicks, cuts, crushing and charring.

NOTE 2 The operation of mechanical stripping tools can leave slight pressure markings in the remaining conductor insulation. This effect is considered to be normal.

c. The insulation material shall not be charred by thermal stripping.

NOTE Discoloration of the insulation material after thermal stripping is normal.

7.2.1.3 Damage to conductors

a. The conductor shall not be damaged by the insulation removal process.

NOTE Example: Conductor damage includes twisting, ringing, nicks, cuts or scores.

b. Part leads and other conductors that are reduced in cross-sectional area by the insulation removal process shall not be used.

c. Coated wires where the base material is exposed shall not be used.

7.2.1.4 Insulation clearance

a. The maximum insulation clearance, measured from the solder joint, shall be as stated in Table 7-1.

b. In the case of the assembly of coil winding wires, maximum insulation clearances may be exceeded provided that electrical clearances are maintained.

c. For PTFE-insulated wire, the minimum distance between the insulation and the solder fillet shall be 1 mm.

NOTE The minimum clearance distance for PTFE insulation accommodates cold flow.

d. The wire insulation shall not be in contact with the solder joint.

Table 7-1: Clearances for insulation

Wire diameter (American Wire Gauge)	**Conductor diameter** d (mm)	**Insulation clearance** (maximum)
32 to 24	0,200 to 0,510	$4 \times d$
22 to 12	0,636 to 2,030	$3 \times d$
≥ 10	≥ 2,565	$2 \times d$

7.2.2 Surfaces to be soldered

7.2.2.1 Cleaning

a. Before assembly, components, wire, terminal and connector contacts shall be visually examined for cleanliness, absence of oil films and freedom from tarnish or corrosion.

b. Conducting surfaces to be soldered shall be cleaned using solvents specified in clause 6.4.

c. Abrasives shall not be used for surface preparation.

NOTE Abrasives can include pumice, pumice-impregnated erasers and emery paper.

7.2.2.2 Wire lay

a. Disturbed lay in stranded-wire conductors shall be restored before soldering.

b. Restoration of the lay shall be done without contaminating the conductor.

7.2.2.3 Terminals and solder cups

a. Terminals and solder cup sizes shall be selected to match the size of conductors in accordance with the manufacturer's data sheet.

b. The size of terminals or solder cups shall not be modified.

7.3 Degolding and pretinning

7.3.1 General

a. Solder alloy used for degolding and pretinning shall be Sn60, Sn62 or Sn63 solder.

b. Applied temperature to component termination shall not exceed the manufacturer recommendations.

c. For temperature sensitive components, thermal shunts, in accordance with clause 5.6.8.3 may be used.

d. Pretinning temperature shall not exceed the temperature used for degolding one

e. The lead forming of components with glass-to-metal lead seals shall be performed before degolding and pretinning.

f. The lead forming for glass-to-metal leads may be performed after degolding and pretinning provided demonstration of absence of cracks in the leads after lead forming.

g. The distance of the degolding and pretinning to the component body shall be compliant with the manufacturer's recommendations or more than 0,75 mm in case not specified by the manufacturer.

7.3.2 Solder baths method for degolding and pretinning

a. Solder baths used for degolding and pretinning shall be in accordance with Table 7-2.

b. A controlled method shall be established and implemented for the replacement of solder baths, based on either:

   1. **Contaminants**: Replace the solder bath alloy when the contaminants limits given in Table 7-2 are exceeded, or
   2. **Time**: Establish a schedule of solder-bath replacement with justification of the replacement frequency.

c. Degolding and pretinning shall be performed according to the following sequence:

   1. ROL0 or ROL1 flux is applied to area to be degolded.
   2. Surface impurities is removed from the bath surface before use.
   3. Gold-plated component leads and terminals are dipped into solder bath-1 for a time between 2 (two) seconds and 4 (four) seconds.
   4. ROL0 or ROL1 flux is applied to degolded area.
   5. The fluxed area is dipped into solder bath 2 (two) for a time between 2 (two) seconds and 4 (four) seconds.
   6. The component leads are cooled before cleaning.

NOTE Rapid cooling by contact with cleaning solvents can crack packages or glass-to-metal seals

d. The cross-sectional area of terminations shall not be reduced by dissolution into the solder bath below the minimum values of specification.

Table 7-2: Solder baths parameters for degolding and pretinning

	Solder bath 1	Solder bath 2
Use	Gold dissolution	Pretinning
Temperature range (°C)	245 to 280	210 to 280
Time	2 to 4 seconds	2 to 4 seconds
Contaminants limits (weight %)	Au < 1	Cu < 0,25; Au < 0,2; (Cu + Au) < 0,3; Zn, Al and Fe: traces.

7.3.3 Solder iron method for degolding and pretinning

7.3.3.1 PCB

a. For degolding, solder shall be melted onto the conductor using a soldering iron tip with temperature lower than 330 °C.

b. Solder shall be wicked-out using copper braid.

c. For pretinning, solder shall be applied on the PCB conductor using a solder iron tip with temperature lower than 330 °C.

7.3.3.2 Components terminations

a. For degolding and pretinning, solder shall be melted onto the component termination using a soldering iron tip with temperature lower than the maximum recommended by the component manufacturer.

b. Solder shall be wicked-out using copper braid.

7.3.3.3 Solder cup

a. For degolding, solder shall be melted inside the solder cup using a soldering iron tip with temperature lower than 330 °C.

b. Solder shall be wicked-out using stranded wire or copper braid.

c. For pretinning, solder shall be applied inside the solder cup using a solder iron tip with temperature lower than 330 °C.

d. Excess of solder shall be removed with stranded wires or copper braid.

7.3.4 Pretinning processes

7.3.4.1 Alloying of pure tin finish component leads

a. Pure tin component terminations shall be pretinned with full tin lead solder coverage.

b. Pure tin component terminations shall be in compliance with requirements from clauses 7.3.2, 7.3.4 and requirement 8.1a from ECSS-Q-ST-60-13.

NOTE Pure tin terminations can be dipped into liquid solder as described in clause 7.3.2 in order to replace the tin with tin-lead alloy.

c. Reprocessing process shall be verified by microsectioning and SEM/EDX with respect to alloying and full coverage.

7.3.4.2 Solder bath method for pretinning of stranded wires

a. The insulation materials shall be removed in accordance with clause 7.2.1.

b. ROL0 flux shall be applied to wires.

c. The fluxed area shall be dipped into solder bath 2 (two) for a time between 3 (three) seconds and 4 (four) seconds.

NOTE Pretinning promotes solderability and prevents untwisting or separation stranded wires.

d. The cross-sectional area of terminations shall not be reduced by dissolution into the solder bath below the minimum values of specification.

e. Antiwicking tools shall be used to prevent solder flow under the insulation.

7.3.4.3 Solder iron method for pretinning of stranded wires

a. Stranded wires may also be pretinned by applying solder to the wire using a heated soldering-iron tip.

b. Solder shall be melted onto the conductor using a heated soldering iron.

c. Solder shall be wicked-out using stranded wire.

7.3.5 Constraints on pretinning methods

a. Solder shall penetrate to the inner strands of stranded wire.

b. Solder shall not be in contact with the insulation.

c. Pretinning shall not degrade the characteristics of the wire.

NOTE Flow of solder (wicking) beyond the insulation can reduce the flexibility of the wire.

d. The insulation shall not be damaged by the pretinning.

e. Flux shall be removed by means of a cleaning solvent, in compliance with clause 6.4.

f. Cleaning solvent shall not flow under the wire insulation.

NOTE Application using a lint-free cloth can limit the flow of solvent.

7.4 Preparation of the soldering tip

7.4.1 Fit

a. The soldering tip shall be fitted in accordance with the equipment manufacturer's specification.

7.4.2 Maintenance

a. Oxidation products shall be removed from the tip.

NOTE Build-up of oxidation products can reduce the ability of the tip to transfer heat.

b. Plated tips shall be examined for cracking.

NOTE Cracked platings allow the liquid solder to alloy with and erode the underlying copper, forming intermetallics which reduce heat transfer and lead to unacceptable joints.

c. Prior to examination, solder obscuring the surface shall be removed when the iron is hot by wiping the tip with moist, lint-free, sponge material.

d. Tips with cracked platings shall be removed from the soldering area.

7.4.3 Plated tips

a. Deposits shall be removed using a moist sponge.

b. Adherent deposits may be removed using abrasive paper of grain size 600 or finer.

NOTE The use of a file to remove the deposits is forbidden.

7.4.4 Tip in operation

a. The working surface of the soldering tip shall be pretinned in accordance with clause 7.3.2.

NOTE Pretinning prevents oxidation of the tip.

7.5 General handling

a. ESD-sensitive components shall be handled in accordance with clause 5.5.

b. Metal surfaces to be soldered that show visible evidence of contaminants shall be cleaned with a solvent specified in clause 6.4.

c. During assembly, component leads, terminals, wire ends and PCB termination areas shall not be touched with bare hands.

d. After final cleaning, personnel working with PCBs shall wear lint-free gloves or finger cots.

7.6 Storage

7.6.1 Components

a. Storage facilities shall protect components from contaminants and damage.

b. Storage boxes and bags shall be made of materials which do not degrade the solderability of the components.

c. Storage materials shall not contain amines, amides, silicones, sulphur or polysulphides.

d. Packaging and containers for ESD-sensitive components shall be in accordance with clause 5.5.

7.6.2 PCBs

a. Bare PCBs shall be stored in accordance with clause 6.11 of ECSS-Q-ST-70-60.

7.6.3 Materials requiring segregation

a. Solders not in accordance with clause 6.2 shall be removed from the work area.

b. Activated fluxes shall be stored in accordance with clause 6.3.1e.

NOTE Example: ROH1 flux.

c. Solvents that do not conform to clause 6.4 shall be removed from the work area.

NOTE Example: Solvents contaminated with impurities such as inorganic acids.

7.7 Baking conditions of PCBs

a. Baking of bare PCBs should be made as a minimum of 8 hours at 120 °C.

b. Baking of populated PCBs shall be performed when the PCB has been kept under clean room conditions for more than 72 hours.

NOTE Storage of PCBs in dry cabinet interrupts the accumulated baking time.

c. Baking of populated PCB shall be made at a temperature which does not degrade the components or assembly.

NOTE To limit the bake out operation, which can induce later failure, the PCB can be stored in dry environment after the baking.

7.8 Baking and storage of moisture sensitive components

a. Baking of moisture sensitive components shall be implemented in conformance with IPC J-STD-033D (2018) before any reprocessing or assembly process.

NOTE This is to counteract the "popcorn" effect in soldering using oven or vapour phase reflow techniques.

b. Baking times and temperatures, for moisture sensitive components, shall be in compliance with manufacturer recommendations and baking times as specified in IPC J-STD-033D (2018) and documented.

NOTE 1 Typical baking conditions are from 6 h to 24 h at 125 °C depending on the classification, except for components delivered in reels for which a lower temperature and longer time are used.

NOTE 2 It is good practice to store components under nitrogen, dry air (20 % RH maximum) or partial vacuum.

8
Components mounting requirements prior to soldering

8.1 General requirements

a. When staking, bonding or underfill are performed before soldering, it shall be performed in accordance to clause 11.2.

NOTE Staking, bonding or underfill can be applied before or after soldering depending on configuration.

8.2 Mounting of plated through hole components

8.2.1 General

a. Distance between the bottom of the component body and the mounting surface shall be less than 3,5 mm.

b. For components with stress relief, the distance between the bottom of the component body and the mounting surface may be up to 5 mm.

8.2.2 Heavy components

a. Components weighing more than 5 g shall be supported by either one of the following methods:

1. adhesive compounds in accordance with clause 6.11, or
2. mechanical methods.

NOTE For example: lacing.

b. The support method shall not impose stresses that result in functional degradation or damage to the part or assembly.

c. The support method shall not impair stress relief designs.

8.2.3 Metal-case components

a. Metal-case components shall be electrically insulated using space-approved materials in accordance with ECSS-Q-ST-70-71 Annex C when they meet one of the following conditions:

1. mounted over printed conductors,
2. in contact with another metal-case component,
3. in contact with a conductive material.

b. Metal-cased components shall not be mounted over soldered connections.

c. Component identification marks shall not be obscured by the insulation.

NOTE For example, the serial numbers.

8.2.4 Glass-encased components

a. Glass-encased parts shall be enclosed with sleeving when epoxy material is used for staking, conformal coating or encapsulating.

NOTE Epoxy material cannot be applied directly to the glass.

b. Glass-encased components may be enclosed in resilient transparent sleeving or in heat-shrinkable sleeving.

NOTE Heating and shrinkage of sleeving can damage glass-encased components.

8.2.5 Stress relief of components with bendable leads

a. Stress relief shall be incorporated into soldered leads and conductors as well as interfacial connections.

NOTE 1 Stress relief provides freedom of movement for component leads or conductors between points of constraint.

NOTE 2 Stresses can arise between points of constraint due to mechanical loading or temperature variations.

NOTE 3 Examples of stress relief methods are shown in Figure 8-6, Figure 8-10 and Figure 8-11.

b. The assembly of TO-39, TO-59 and CKR-06 packages shall be performed in accordance with Figure 8-1 when assembled without stress relief.

c. Underfill staking of PTH packages as presented in Figure 8-2 may be used if verified according to clause 13.

d. Stress relief designs shall not damage the assembly.

NOTE Long lead lengths or large loops between constraint points can vibrate and damage the assembly.

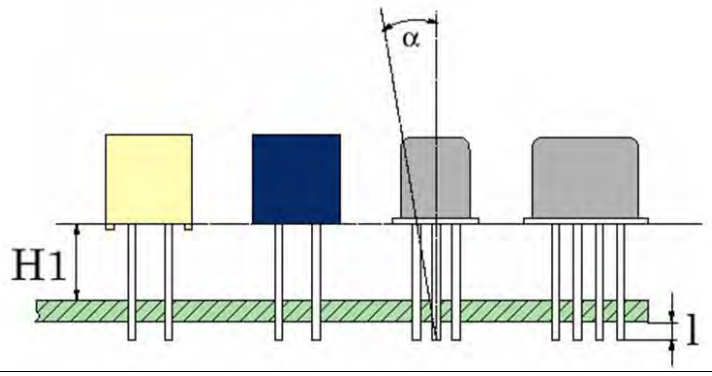
e. Leads shall not be temporarily constrained against spring-back force during soldering.

NOTE Residual stresses are produced in the lead material or solder joint.

f. Solder fillets shall not impair stress relief bends.

g. CKR06 and similar packages shall be adhesively staked in accordance with Figure 8-1.

NOTE The use of a filler (silica powder) can prevent excessive flow of adhesive.



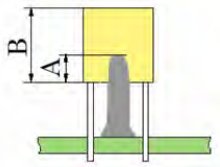
Mounting without spacer: 2,4 mm ≤ H1 ≤ 3 mm

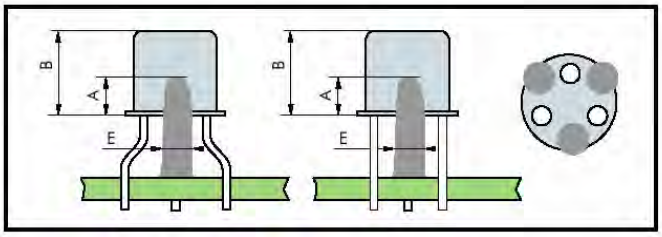
Mounting with spacer: 2 mm ≤ H1 ≤ 3,5 mm

l: see Figure 8-9

$\alpha \leq 10°$

Dimensional limits





Preferred A > = 1/3 B

a) Adhesively staked transistor

b) Adhesively staked CKR06

Figure 8-1: Assembly of TO-39, TO-56 and CKR06

Figure 8-2: Staking of TO package with underfill

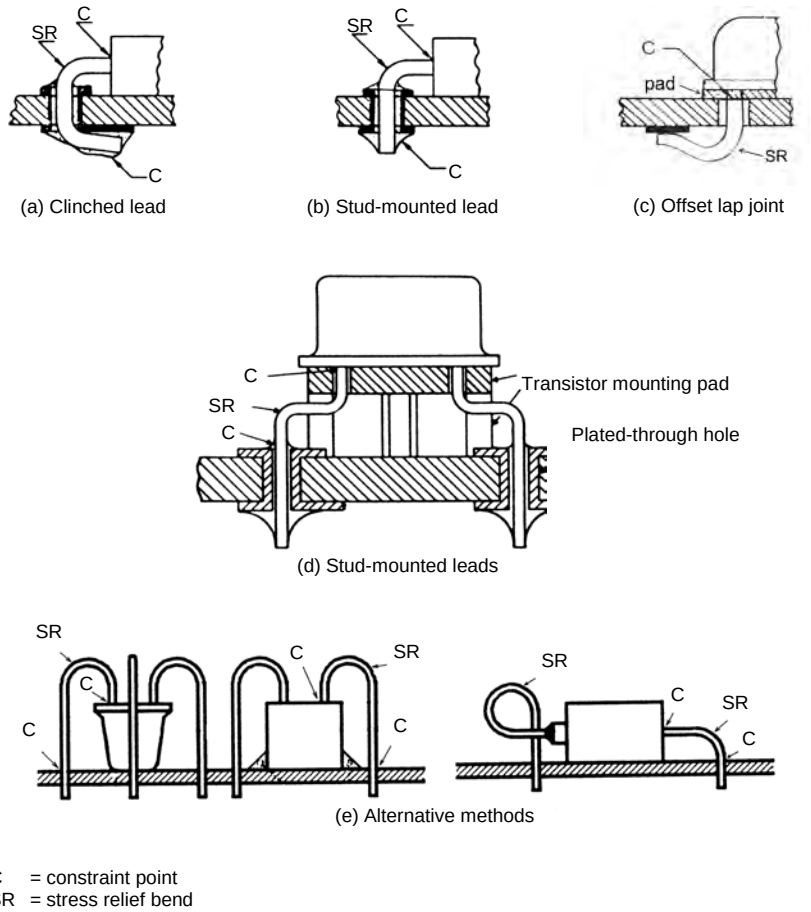


Figure 8-3: Methods for incorporating stress relief with components having bendable leads

8.2.6 Stress relief of components with non-bendable leads

a. Stress relief for components with non-bendable leads mounted in contact with the PCB or adhesively bonded to the PCB shall use wire extensions according to Figure 8-4.

NOTE Bending can damage components when lead diameters are large or components have delicate seals or where lead-material composition makes bending impracticable.

b. DIP components with brazed leads up to DIP 24 may be assembled without additional stress relief, provided that the tapered portions of the leads are clear of solder. In order to achieve acceptable stand-off, a shim can be used.

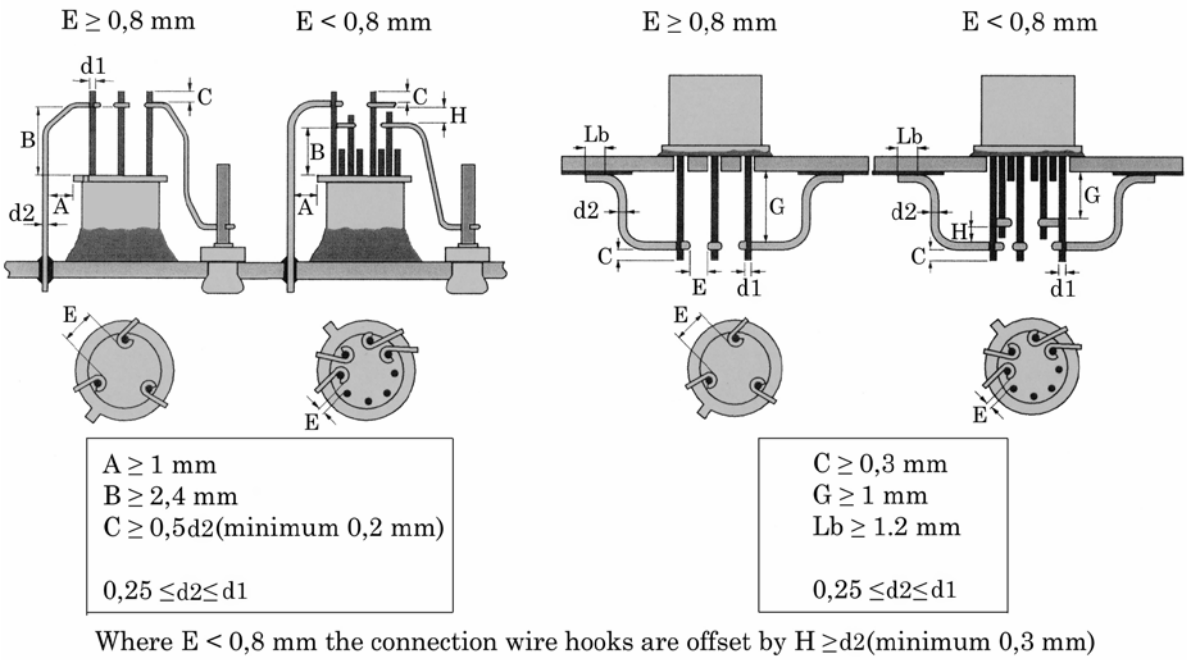


Figure 8-4: Methods for attaching wire extensions to non-bendable leads

8.2.7 Lead and conductor cutting

a. Solder terminations shall not be cut after the soldering operation.

NOTE Component leads and wires are cut and shaped before soldering.

8.2.8 Location

a. Component bodies shall not be located in contact with soldered or welded terminations.

8.2.9 PTH lead bending requirements

8.2.9.1 General

a. During bending, component leads shall be supported to avoid axial stress and damage to seals or internal bonds.

b. The inside radius of a bend shall not be less than the lead diameter or ribbon thickness.

c. The distances between the bends and the end seals at either end of an axial component shall be similar.

d. The minimum distance from the bend to the end seal shall be two times the lead diameter for round leads and 0,50 mm for ribbon leads in accordance with Figure 8-5(a).

e. Where the component lead is welded the minimum distance to the bend shall be measured from the weld in accordance with Figure 8-5(b).

NOTE Example: Tantalum capacitors.

f. Bending tools shall not impinge on the weld.

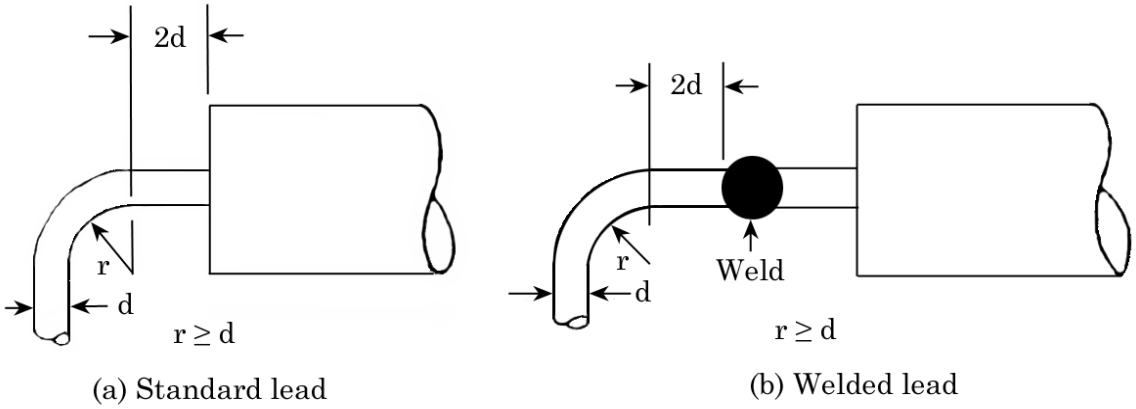


Figure 8-5: Minimum lead bend

8.2.9.2 Conductors terminating on both sides of a non-plated-through hole

a. Stress relief shall be provided in the component lead on both sides of the PCB in accordance with Figure 8-6 (a).

b. When a solid hook-up wire is used to interconnect solder terminations on opposite sides of a PCB, stress relief shall be provided in the wire between the two terminations in accordance with Figure 8-6 (b).

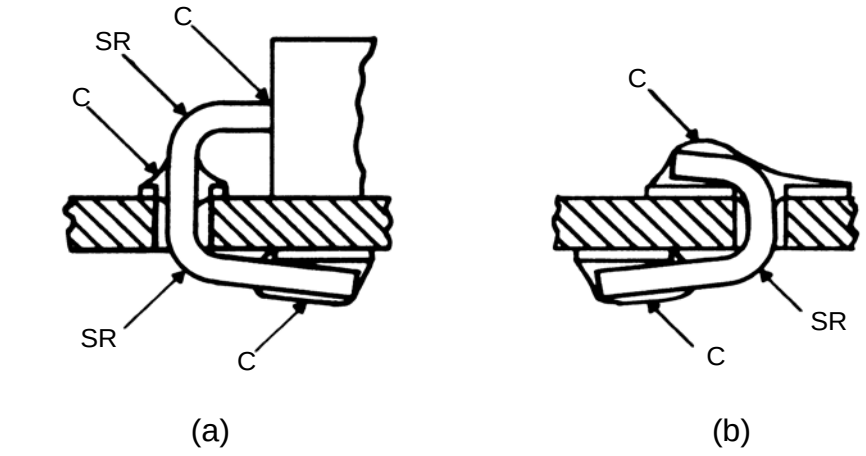


Figure 8-6: Leads with solder termination on both sides

8.2.10 Mounting of swage terminals to PCBs

a. Swage-type terminals, designed to have the terminal shoulder soldered to printed conductors, shall be secured to single-sided PCBs by a roll swage in accordance with Figure 8-7(a).

b. Swage-type terminals that are mounted in a plated-through hole shall be secured to the PCB by an elliptical funnel swage in accordance with Figure 8-7(b).

NOTE An elliptical funnel swage enables complete filling of the plated-through hole with solder.

c. The PCB shall not be damaged by the swaging process.

d. After swaging, the terminal shall be inspected for circumferential splits or cracks.

e. After swaging, the terminal shall be free from circumferential splits or cracks.

f. After swaging, the terminal may have a maximum of three radial splits or cracks, provided that the splits or cracks do not extend beyond the swaged area of the terminal and are a minimum of 90° apart.

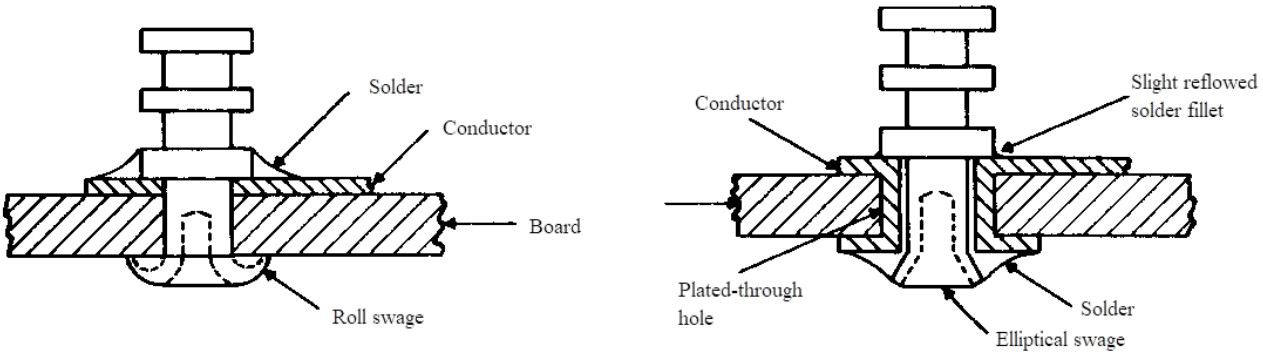


Figure 8-7: Types of terminal swaging

8.2.11 Lead attachment to PCBs

8.2.11.1 General

a. Solder terminations shall be visible for inspection after soldering.

b. Component leads shall be terminated to PCBs by clinch, stud or lapped terminations.

8.2.11.2 Clinched leads

a. Non-bendable leads shall not be clinched, see also clause 8.2.5

b. Clinched leads terminating at a PCB pad shall be bent to make contact with the printed circuit conductors.

c. The clinched lead shall not extend beyond the edge of the conductor pattern, see Figure 8-8.

d. The lead shall not be forced to lie flat at the bend radius, see Figure 8-8

e. Component leads can spring-back when clinched.

f. The soldered length shall comply with clauses 8.2.11.4 and 8.2.11.5.

g. Rounded termination areas shall be such that:

1. the lead extends through and overlap the solder pad,

2. the lead is bent in the direction of the longest dimension of the solder pad, and
3. the area of the solder-pad permits a solder fillet to be formed.

h. The solder joints to clinched termina shall meet the solder fillet requirements of Figure E-1.

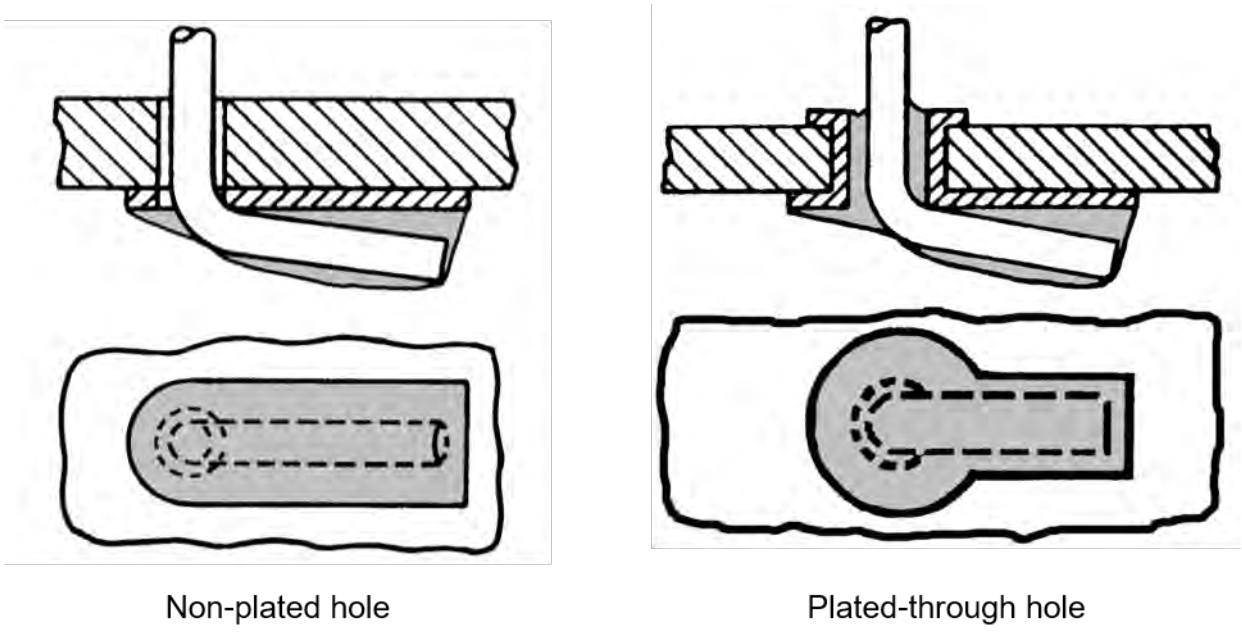


Figure 8-8: Clinched-lead terminations

8.2.11.3 Stud leads

a. For unsupported holes, the cut stud leads shall protrude beyond the PCB surface by 1,5 mm ± 0,8 mm, as illustrated in Figure 8-9(a).

b. For plated-through hole less than 2,2 mm in length, the cut stud leads shall protrude beyond the PCB surface by 1,5 mm ± 0,8 mm, as illustrated in Figure 8-9(b).

c. For components with short leads and plated-through holes, greater than or equal to 2,2 mm in length, the protrusion may be zero, provided that the outline of the lead is visible, there is wetting between the lead and pad around the entire circumference and there is complete penetration of solder to the component side according to Figure 8-9(c).

d. For components with procured short leads soldered in plated through-holes of thick PCBs negative protrusion may be accepted, provided that all the following conditions are met:
   1. The leads are pretinned before soldering, for optimal wetting.
   2. Additional heating from the component side, by means of an extra soldering iron, is applied.
   3. After soldering, the terminal pad on the component side shows solder flow-through with wetting according to 10.3.1.3b.
   4. X-ray inspection is carried out after soldering.
   5. The maximum amount of voids is in compliant with requirement 12.4a.

6. X-ray inspection shows solder flow of 90% within the plated through hole.

e. The solder joints to stud terminals shall meet the solder fillet requirements of Figure E-2.

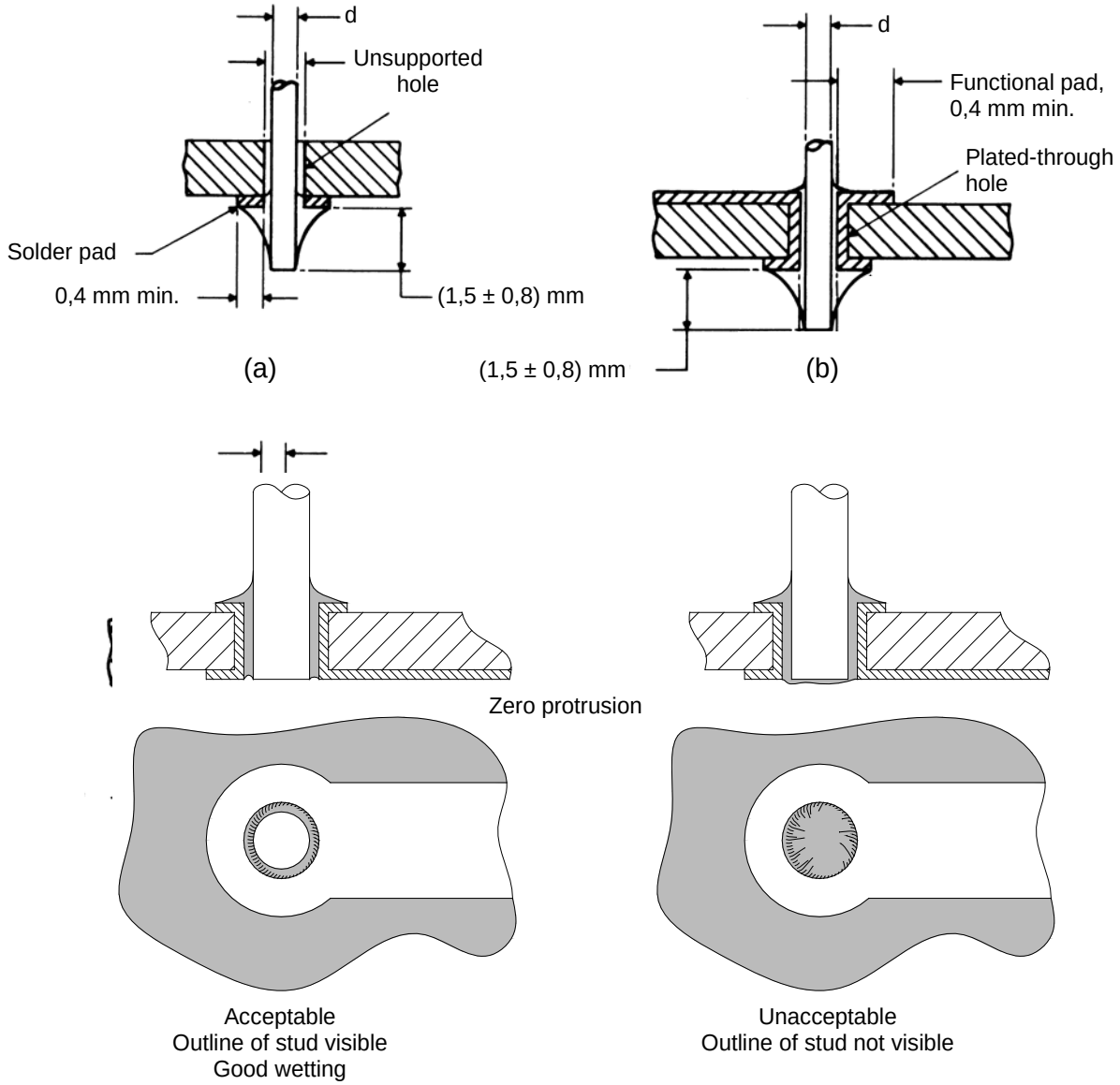


Figure 8-9: Stud terminations

8.2.11.4 Lapped round leads

a. Round leads shall overlap the solder pad in compliance with Figure 8-10(a).

b. No portion of the soldered lead termination shall project beyond the edges of the pad.

8.2.11.5 Lapped ribbon leads

a. Ribbon leads shall overlap the solder pad, in compliance with Figure 8-10(b).

b. No portion of the soldered lead termination shall project beyond the edges of the pad.

c. One side of the lead may be flush with the edge of the solder pad.

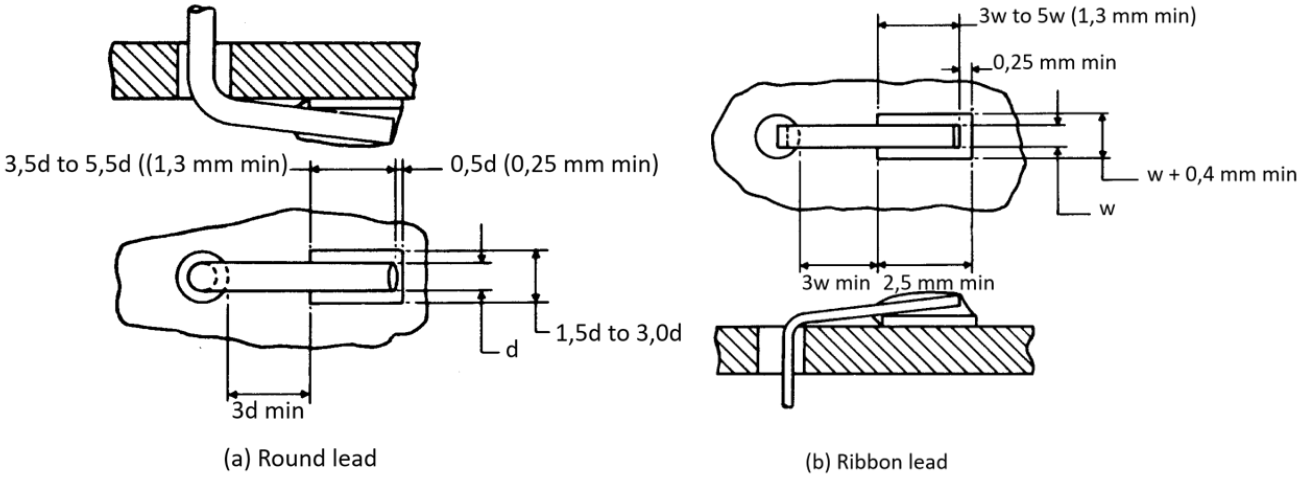


Figure 8-10: Methods of through-hole lapped termination

8.2.12 Mounting of components to terminals

a. Degree of wrap, routing and connection to terminals shall be in accordance with clause 9 and 10.

b. The lead length between the component and the terminals shall be similar at both ends, except where component package shapes dictate staggering.

NOTE Example: Top hat diodes with flanges.

c. Stress relief shall be provided in accordance with Figure 8-11.

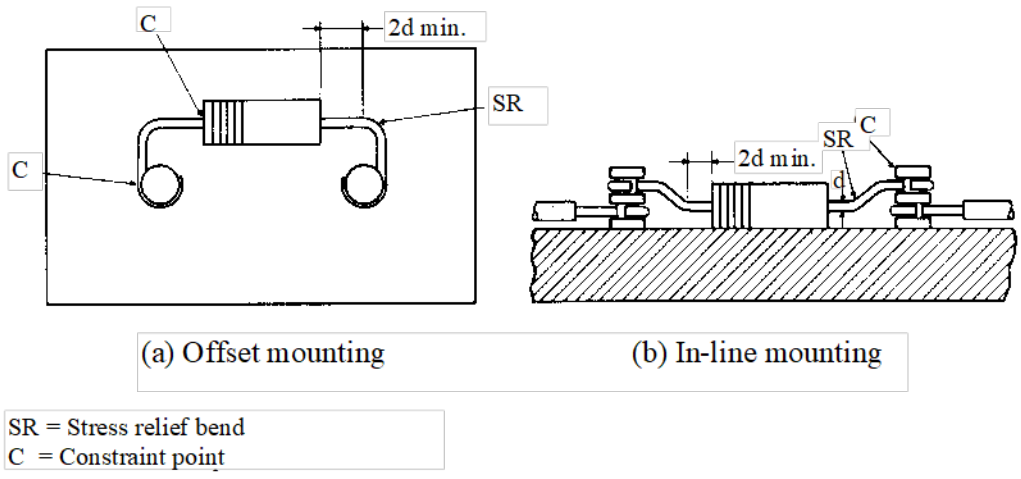


Figure 8-11: Method of stress relieving parts attached to terminals

8.2.13 Mounting of through hole connectors to PCBs

a. PCB connectors shall be supplied with either:
   1. pre-formed leads supporting stress relief bends, or
   2. straight, resin bonded leads.

b. Degolding and pretinning of leads, in accordance with clause 7.3, shall be performed before mechanical fixing of connectors to the PCB.

c. Before soldering, the operator shall verify that there is no contact between the solder fillet to be formed and the gold plating.

d. Connector leads shall protrude through the board in accordance with clause 8.2.11.3.

8.3 Mounting of surface mount components

8.3.1 General

a. When CTE mismatch exists between components and substrate, the supplier shall take it into account with the mounting technology.

NOTE 1 Pure eutectic tin-lead solder or indium-lead solder provide better stress relief (due to their ductility) than those with additional elements, e.g. antimony, gold.

NOTE 2 Leadless components with e.g. end-cap terminations, metallization, can have some stress relief (such as additional foil or wire leads, possibly attached by welding or high melting point solder).

NOTE 3 A solder stand-off can assist stress relief. In this situation, the CTE mismatch strain is taken up by the ductile solder.

b. Surface mounting of leaded components shall be parallel to the board surface.

c. Components to be mounted shall be designed for and be capable of withstanding the soldering temperatures of the particular process being used for fabrication of the assembly.

NOTE Surface mounted components can be mounted on either one side or both sides of a printed circuit assembly.

d. Components unable to withstand machine soldering temperatures shall be hand soldered in a subsequent operation.

NOTE To mount component by hand soldering at very low temperature can degrade reliability of component and PCB by increasing the duration of soldering necessary to obtain an acceptable solder joint.

e. The supplier shall not exceed the component manufacturer's mandated processing conditions for degolding, pretinning, reprocessing and soldering.

f. The supplier may exceed the component manufacturer's mandated processing conditions, as stated in 8.3.1e, only after:

1. proof of successful verification tests as described in clause 13,
2. dedicated tests at component levels showing there is no degradation of these components, and
3. customer approval.

g. The solder fillet shall not be in contact with any remaining gold-plated area.

h. The spacing between conductive elements shall not be reduced below the minimum electrical spacing specified in clause 7.3 of ECSS-Q-ST-70-12.

NOTE Some surface mounted components that are not bonded to the PCB can self-align during the soldering process. It is the registration after soldering that is important.

8.3.2 Lead forming

a. The leads of leaded surface mount components shall be formed to their final configuration prior to mounting.

b. Forming shall not degrade the solderability or cause loss of plating adhesion to the leads.

c. Forming shall not cause mechanical damage to the leads or attachment seals.

d. Leads of dual-in-line and gull-wing packages, flat-packs and other multileaded components may be mechanically re-aligned for co-planarity providing that the lead to package connection is not subjected to plastic deformation.

e. Lead forming shall be symmetrical.

f. Formed leads shall not be re-bent.

8.3.3 Mounting components in solder paste

a. Both leaded and leadless surface mounted components shall be mounted in solder paste prior to reflow soldering.

b. The solder paste deposited on each solder footprint shall be inspected for registration and coverage prior to mounting the components.

8.3.4 Leadless components

a. Components shall not be stacked.

b. The active element, as illustrated in Figure 8-12, shall be mounted with that surface facing away from the printed circuit board or substrate.

NOTE The active element can face the substrate in case required by electrical performance as for RF applications.

c. Components that are bonded to the PCB prior to wave- or reflow-soldering shall be placed in accordance with the requirements given in clause 11.2.

d. The adhesive shall not extend onto the solder footprints.

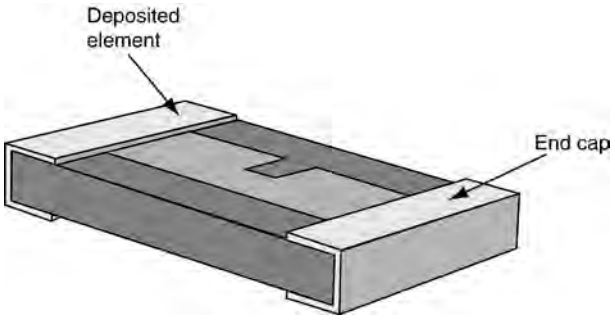


Figure 8-12: Exposed element

9
Attachment of conductors to terminals, solder cups and cables

9.1 General

9.1.1 Conductors

a. A conductor shall be wrapped on to a terminal in the same direction as the final curvature of the wire.

9.1.2 Terminals

a. Gold-plated terminals and solder cups shall have the gold removed in the conductor attachment area in accordance with clause 7.3 and be pretinned in accordance with clause 7.3.4.

b. Terminals shall be selected to fit the conductors.

9.2 Wire termination

9.2.1 Breakouts from cables

a. The length of individual wires routed from a common cable to equally-spaced terminals shall be uniform including wire ends and stress-relief bends.

NOTE Uniform lengths prevent stress concentration in any one wire.

9.2.2 Insulation clearance

a. Where characteristic impedance or circuit parameters are not affected, the insulation clearance values stated in clause 7.2.1.4 shall apply.

b. Where characteristic impedance or circuit parameters are affected, the insulation clearance requirements may be modified providing that sufficient insulation to surrounding conductive elements is kept.

c. The modification implemented in requirement 9.2.2b shall be documented in the process procedures.

NOTE Example: High-voltage circuits or RF coaxial line terminations.

9.2.3 Stress relief

a. Conductors terminating at solder connections shall incorporate stress relief.

b. Wicking shall be controlled.

NOTE Anti-wicking tools can be used for pretinning the stranded wires.

9.3 Turret and straight-pin terminals

9.3.1 Side route

a. Side route connections shall be made as shown in Figure 9-1(a).

b. Conductors shall be wrapped around the post as shown in Figure 9-1(c):

1. a minimum of 1/2 turn.
2. a maximum of 3/4 turn.

c. For turret terminals, all conductors shall be confined to the guide slots.

d. Conductors shall not project beyond the base of the terminal.

e. Wires shall not be wrapped over other wires.

f. More than one wire may be installed in a single slot of a terminal post provided that the combined diameters of the wires are less than the width of the slot.

g. Wires terminating at terminals that do not have a mechanical shoulder or turret shall not be attached closer than one conductor diameter to the top of the terminal.

9.3.2 Bottom route

a. The conductor shall enter the terminal from the bottom, pass through the side slot at the top, and be wrapped as for the side route, as shown in Figure 9-1(b).

b. The solder joints to turret terminals shall meet the solder fillet requirements of Figure E-3and Figure E-4according to twin or single conductor configuration.

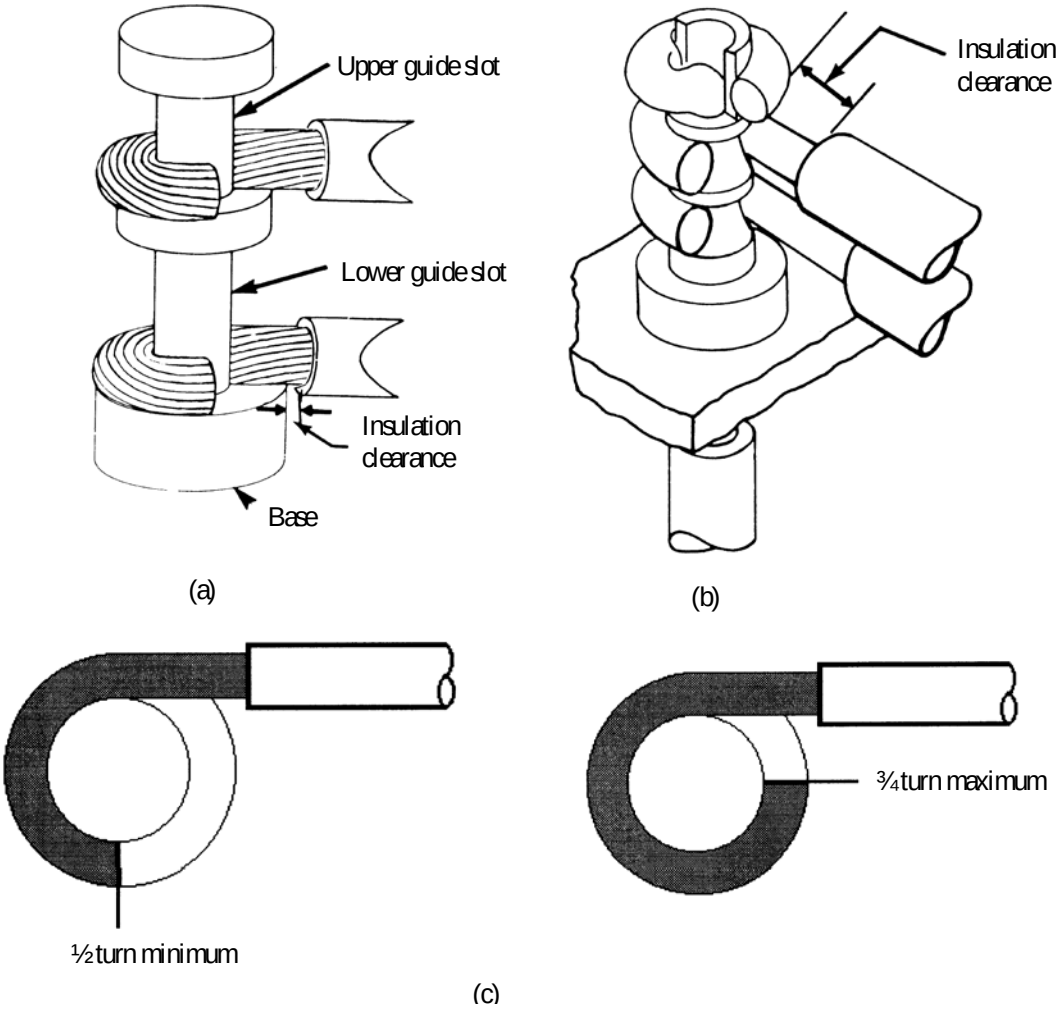


Figure 9-1: Side- and bottom-route connections to turret terminals

9.4 Bifurcated terminals

9.4.1 General

a. Top, side or bottom routes, or combinations thereof, shall be used.

b. Top route and side route shall not be used together on the same terminal.

9.4.2 Bottom route

a. Bottom route connections shall be as shown in Figure 9-2.

b. Conductors may project beyond the diameter of the base, see Figure 9-2(c), provided that clearances, environmental and electrical characteristics are not compromised.

c. The solder joints to bifurcated terminals shall meet the solder fillet requirements of Figure E-1.

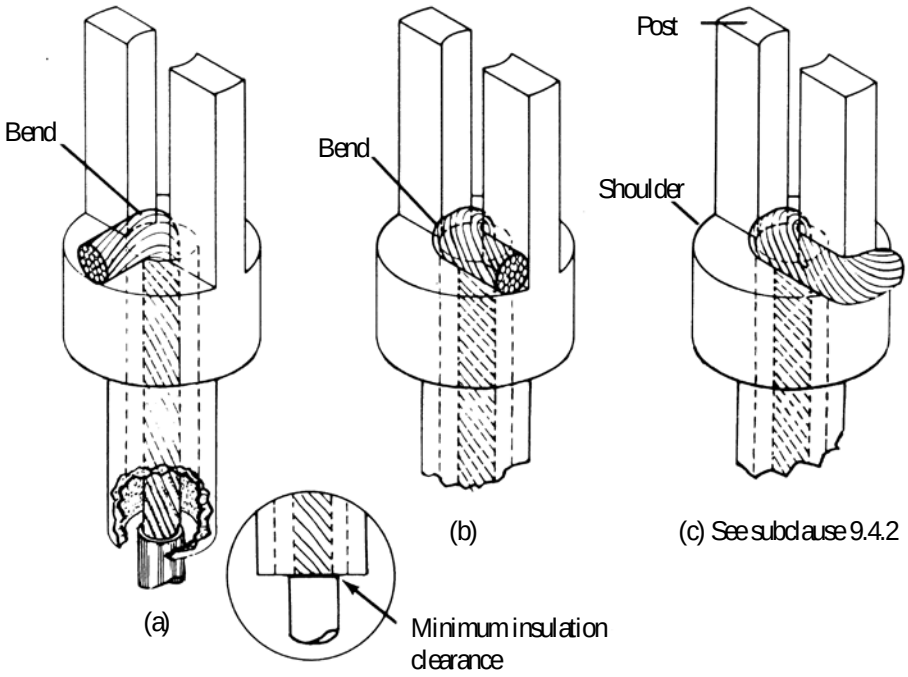


Figure 9-2: Bottom-route connections to bifurcated terminal

9.4.3 Side route

a. Side route connections shall be as shown in Figure 9-3.

b. The conductor shall enter the mounting slot perpendicular to the posts.

c. When more than one conductor is connected to a terminal, the direction of bend of each additional conductor shall alternate, see Figure 9-3(b) and (d).

d. Side-route connections shall not project above the top of the terminal.

e. Conductors may project beyond the diameter of the base, see Figure 9-3(c), provided that clearances, environmental and electrical characteristics are not compromised.

f. Conductors shall be wrapped a minimum of ¼ turn, as shown in Figure 9-3(a), to a maximum of ½ turn, as shown in Figure 9-3(c) around the post.

g. The solder joints to bifurcated terminals shall meet the solder fillet requirements of Figure E-1.

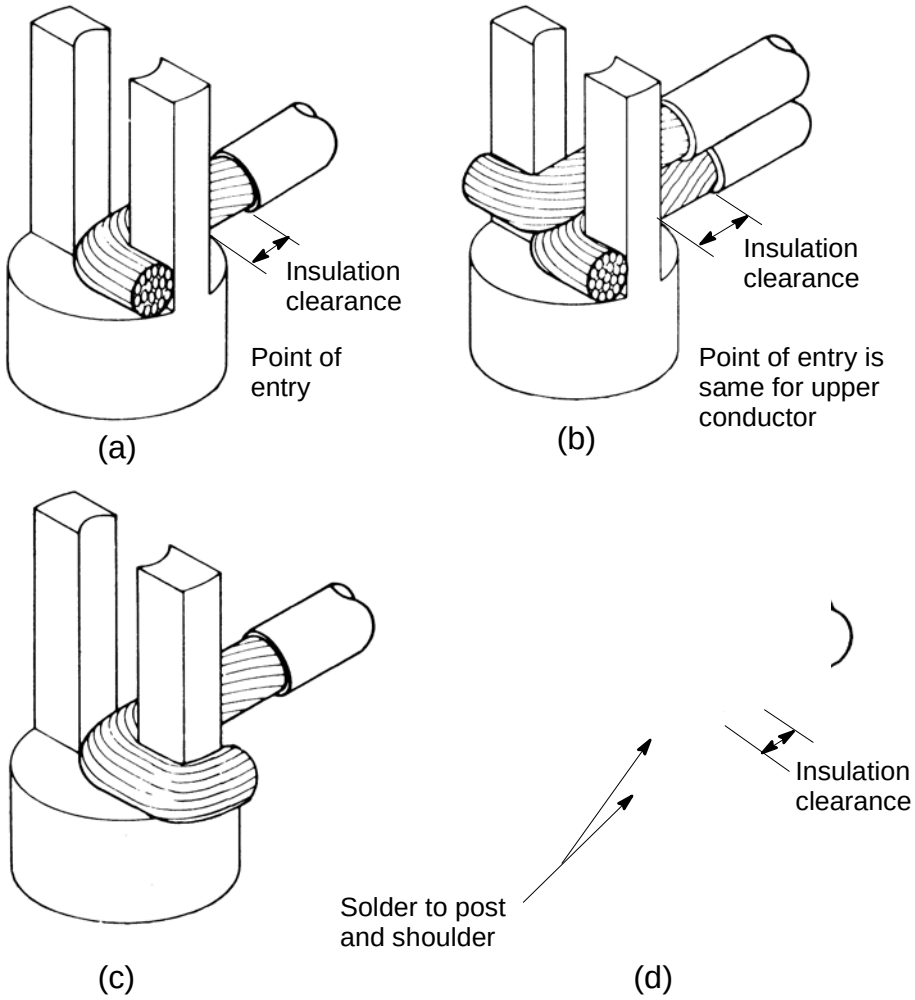


Figure 9-3: Side-route connection to bifurcated terminal

9.4.4 Top route

a. The top route shall not be used where side entry is possible.

b. Top route connections shall be as shown in Figure 9-4.

c. Conductors shall be inserted between the vertical posts to the depth of the shoulder, except for combined top and bottom routes as per clause 9.4.5.

d. Conductors which do not fill the gap, as shown in Figure 9-4, shall be either:

   1. accompanied by a tinned filler solid or stranded wire, such that the combined diameters fill the gap, or

   2. bent double, provided that the combined diameters fill the gap.

e. The top route and side route shall not be used on the same terminal.

f. The solder joints to bifurcated terminals shall meet the solder fillet requirements of Figure E-1.

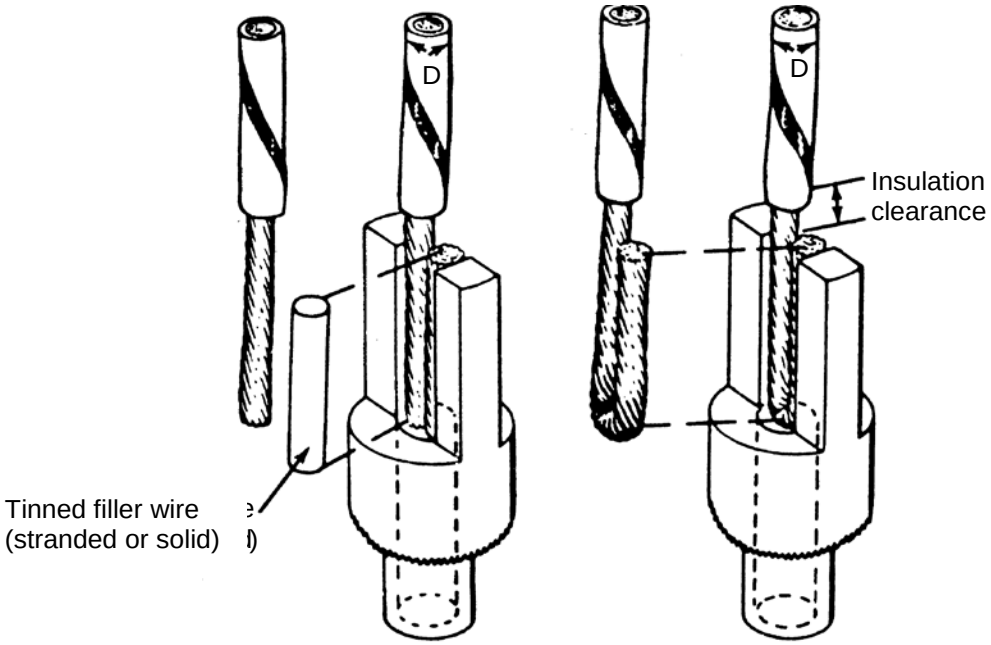


Figure 9-4: Top-route connection to bifurcated terminal

9.4.5 Combination of top and bottom routes

a. The bottom route conductor shall be installed before the top route conductor.

b. The top-route conductor shall be inserted to contact the bottom-route conductor.

9.4.6 Combination of side and bottom routes

a. The bottom route conductor shall be installed before the side route conductor.

9.5 Hook terminals

a. Connections to hook terminals shall be as shown in Figure 9-5.

b. The bend to attach conductors to hook terminals shall be:

1. a minimum of 1/2 turn,
2. a maximum of 3/4 turn.

c. Protrusion of conductor ends shall not damage insulation sleeving.

d. Where more than one conductor is attached to a terminal, the direction of bend of each conductor shall alternate, as shown in Figure 9-5(b).

e. The solder joints to hook terminals shall meet the solder fillet requirements of Figure E-6.

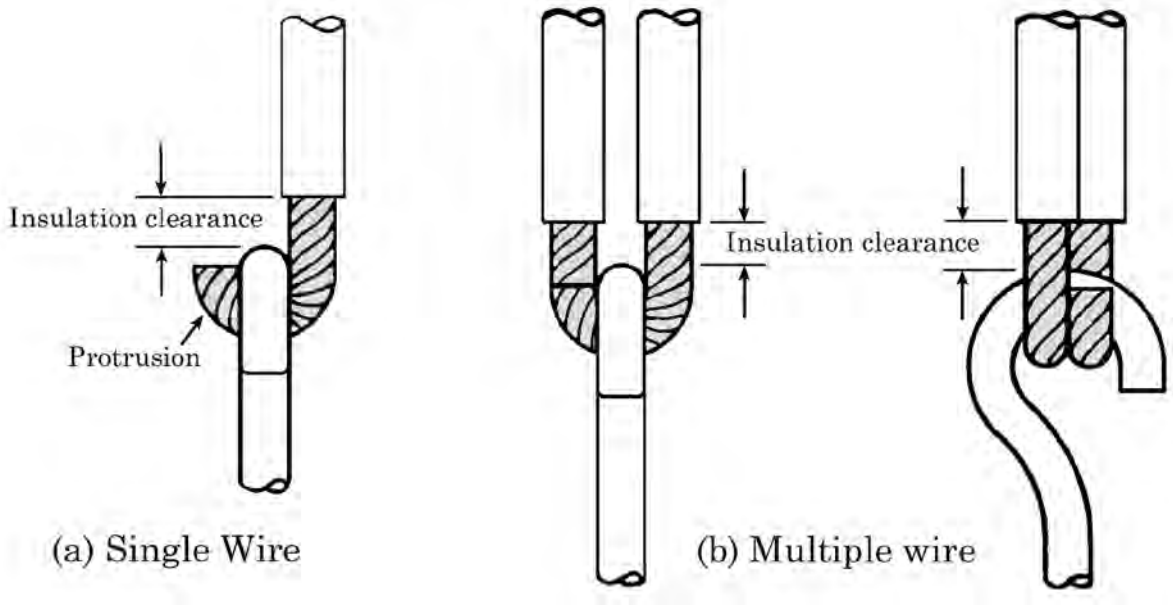


Figure 9-5: Connections to hook terminals

9.6 Pierced terminals

a. Connections to pierced terminals shall be as shown in Figure 9-6.

b. The bend to attach conductors to pierced terminals shall be:

1. a minimum of 1/4 turn,
2. a maximum of 3/4 turn.

c. Protrusion of conductor ends shall not damage insulation sleeving.

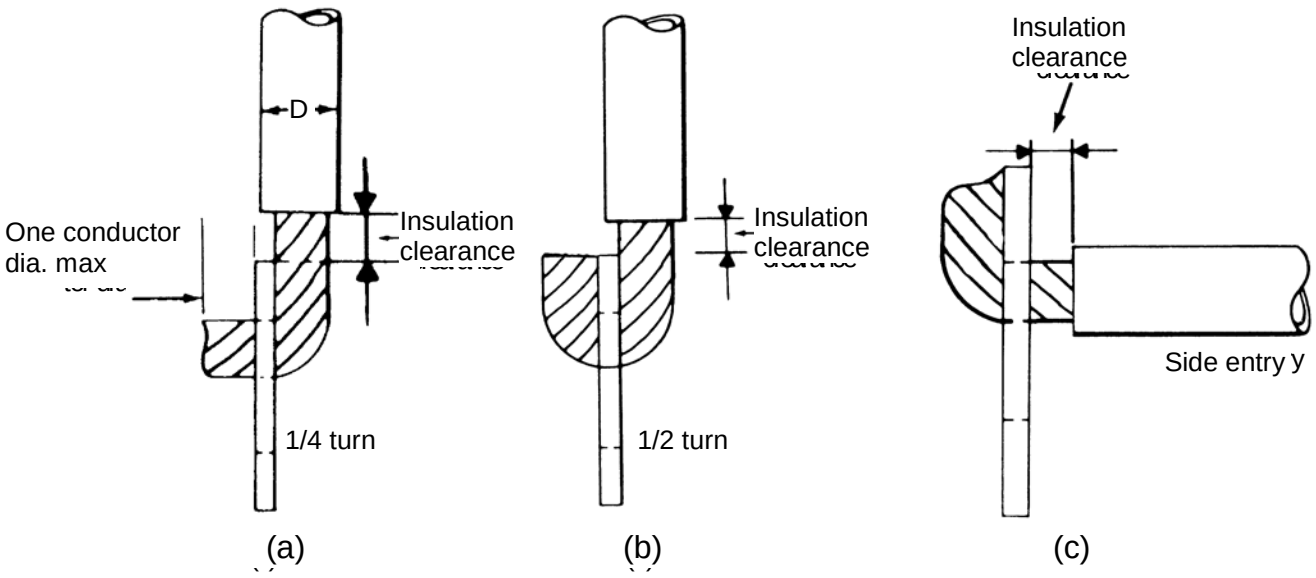


Figure 9-6: Connections to pierced terminals

9.7 Solder cups for connector

a. Conductors shall enter the solder cup as shown in Figure 9-7.

b. Conductors shall be bottomed in the cup.

c. Conductors shall be in contact with the inner wall of the cup.

d. Multiple conductors may be inserted provided that each is in contact with the full height of the inner wall of the cup.

e. Flux shall not be trapped within the solder cup.

f. Conductors shall not misalign floating contacts.

NOTE Example: Solid, rigid conductor wire into connectors.

g. The solder joints to cup terminals shall meet the solder fillet requirements of Figure E-7.

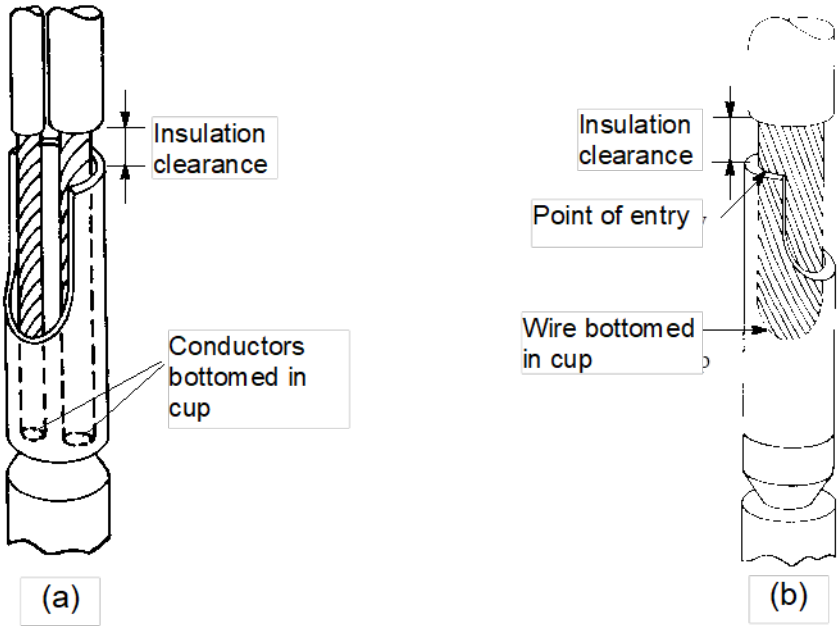


Figure 9-7: Connections to solder cups (connector type)

9.8 Insulation sleeving

a. Connections that are not protected by insulation grommets, potting, or conformal coating shall be protected by insulating sleeving.

NOTE Example: Hook terminals, solder cups and bus wires.

b. Insulation sleeving shall be transparent and heat-shrinkable.

c. A component shall not move within the sleeving when the sleeving is mechanically supported.

d. Heat shrinking of the sleeve shall not damage the assembly.

9.9 Wire and cable interconnections

9.9.1 General

a. Interconnection methods shall not use fluxed solder preforms within heat-shrinkable sleeves.

b. Soldered wire interconnection methods shall enable the removal of flux and flux residue.

c. Soldered wire interconnection methods shall enable visual inspection of the interconnection and surrounding materials.

d. After soldering, conductors shall be covered with heat-shrinkable sleeving.

e. Fluorocarbon sleeves shall not be used.

NOTE Fluorocarbon sleeves have high shrinkage temperatures that can damage or reflow soldered connections.

9.9.2 Preparation of wires

a. Wire insulation shall be removed using insulation strippers in accordance with clause 5.6.6.

b. Wire insulation clearances shall be in accordance with clause 7.2.1.4.

c. Pretinning shall be in accordance with clause 7.3.4.

9.9.3 Preparation of shielded wires and cables

a. The area of exposed shield shall be either:

1. at the end termination of the wire or cable, or
2. at any position along the length of a wire or centre splice cable.

b. The insulation jacket shall be removed for:

1. a minimum length of 5 mm,
2. a maximum length of 12 mm.

c. The insulation jacket shall be scored and removed using a sharp cutting tool.

NOTE Example: A scalpel.

d. The preparation process shall not damage the exposed shield material in accordance with clauses 7.2.1.2 and 7.2.1.3.

e. The shield material shall be of good solderability.

f. The shield material shall not be pretinned.

g. The shield material shall be cleaned using a solvent in accordance with clause 6.4

9.9.4 Pre-assembly

9.9.4.1 Heat-shrinkable sleeving

a. Heat-shrinkable sleeving shall provide electrical insulation and mechanical support to the finished interconnection.

b. The sleeving shall be cut to a length that covers the finished soldered joint and extends over the remaining insulation of each conductor for a distance of 5 mm ±2 mm.

c. The cut sleeving shall be threaded over one of the wires to be joined.

9.9.4.2 Conductors

a. Conductors shall be secured to prevent disturbance during soldering and solidification using one, or a combination of, the following methods:

   1. A holding fixture that clamps the wires ensuring correct alignment.
   2. A strand of binding wire, wrapped a minimum of 3 turns, as shown in Figure 9-8(a).
   3. Rings of heat-shrinkable sleeving positioned over the ends of the wire insulations, see Figure 9-8(b) and (c).
   4. A twist-splice around the braid, see Figure 9-8(c).

      NOTE Example for item 2 are: Bare, tinned-copper wire.

b. The conductors to be joined shall lie parallel and in contact.

c. Conductors may be preformed when the cable insulation prevents a parallel lay.

d. Bending tools for the preforming of conductors shall be in accordance with clause 5.6.4.

e. Wires shall be spliced using lap joints.

f. For shield terminations, the conductor of the grounding wire shall be positioned on the exposed shield.

g. Insulation overlap shall not be greater than the diameter of the largest conductor of the interconnection.

h. The hand solder joints to shielded cables shall meet the solder fillet requirements of Figure E-8.

i. The hand solder joints to shielded wires shall meet the solder fillet requirements of Figure E-9 and Figure E-10.

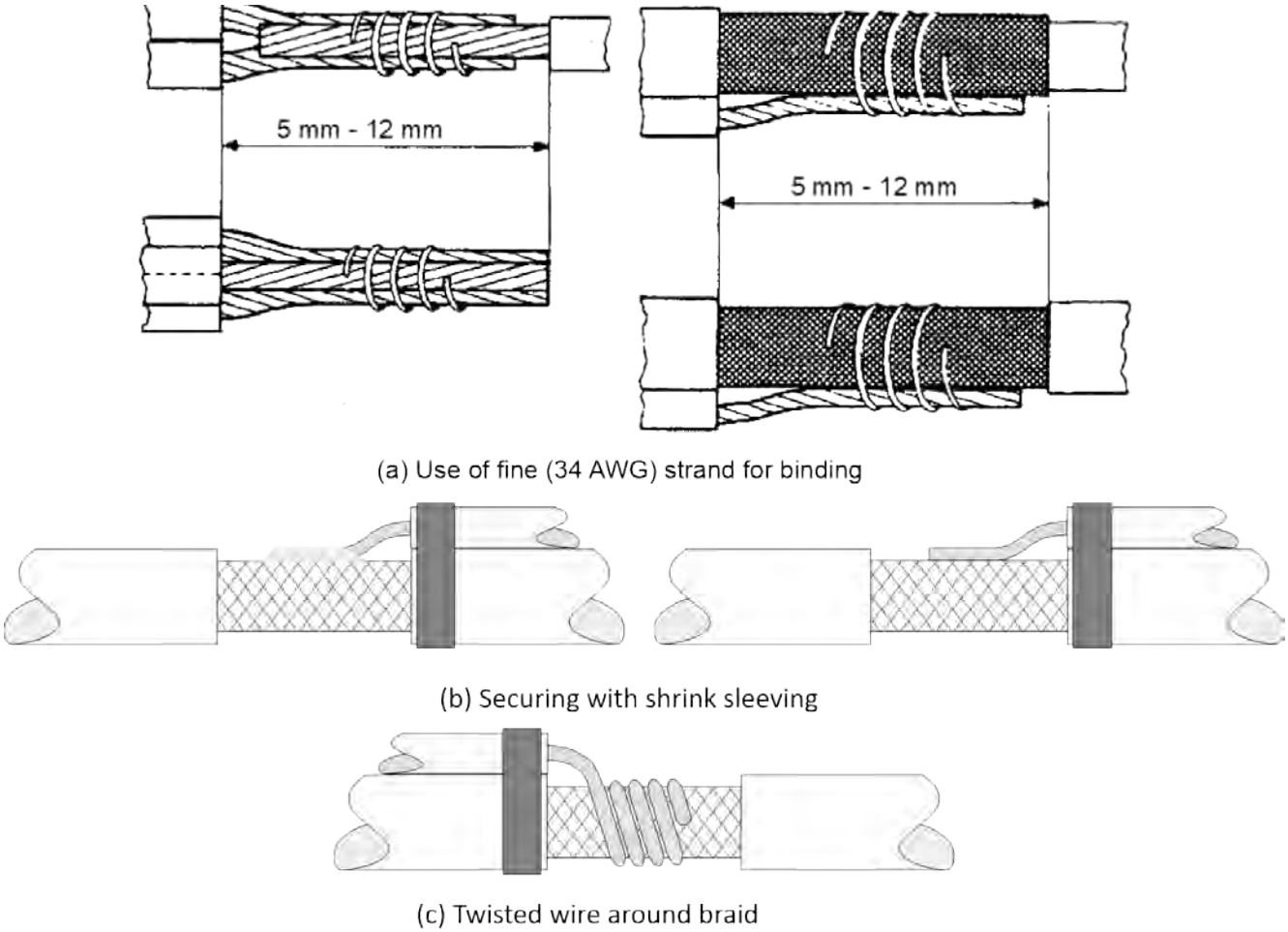


Figure 9-8: Methods for securing wires

9.9.5 Soldering procedures

a. The soldering iron shall be selected in accordance with clause 5.6.8.

b. The solder alloy shall be in accordance with clause 6.2.

c. The flux shall be in accordance with clause 6.3

d. Soldering aids shall be used to restrict wicking of flux or solder under the insulation in accordance with clause 5.6.8.4

e. Each conductor shall be soldered on its entire lap contact.

f. After solder solidification, the contour of each wire conductor shall be visible.

g. After solder solidification, adjacent conductors shall be connected by concave solder fillets.

9.9.6 Soldering of conductors onto terminals except cup terminals

a. A concave fillet of solder shall be present between the terminal and the sides of the conductor.

b. The contour of the conductor shall be visible after soldering.

c. Terminals with more than one wire shall have each wire in contact with, and soldered to the terminal.

9.9.7 Soldering of conductors onto cup terminals

a. The solder shall form a fillet between the conductor and the cup entry slot.

b. The fillet shall follow the contour of the cup opening.

c. Solder spillage may be present on the outside surface of the solder cup provided that it does not interfere with the function or the assembly of the connector.

9.9.8 Cleaning

a. The removal of flux and residues shall be in accordance with clause 11.1.

9.9.9 Inspection

a. Interconnections shall be inspected in accordance with clauses 12.2 and 12.3.

9.9.10 Workmanship

a. Joints shall have a smooth, bright appearance.

b. The workmanship of solder joints shall be in accordance with clause 9.9.

9.9.11 Sleeving of interconnections

a. The heat-shrinkable insulation sleeving shall be centred over the cleaned and inspected interconnection in accordance with 9.9.4.1.

b. The sleeving shall be shrunk using heated gas or radiant energy.

c. Heat shall not be applied for more than 8 seconds.

d. The heat shrinking temperature shall not exceed the maximum temperature recommended by the manufacturer.

e. The heat-shrinking temperature shall not exceed 140 °C.

f. The minimum distance between hot air blower and shrink sleeve shall be demonstrated by the manufacturer to comply with requirement 9.9.11d and 9.9.11e.

9.10 Connection of stranded wires to PCBs

a. Stranded wires shall be soldered to PCB terminations using lap joints or plated-through holes in accordance with Figure 9-9 and Table 9-1.

b. Stress relief shall be provided.

c. For PTFE-insulated wire, the minimum distance between the insulation and the solder fillet shall be 1 mm.

d. Electrical wires shall be supported at 30 mm from the solder and then at intervals not exceeding 50 mm.

e. Electrical wire support shall be provided by staking, conformal coating or lacing.

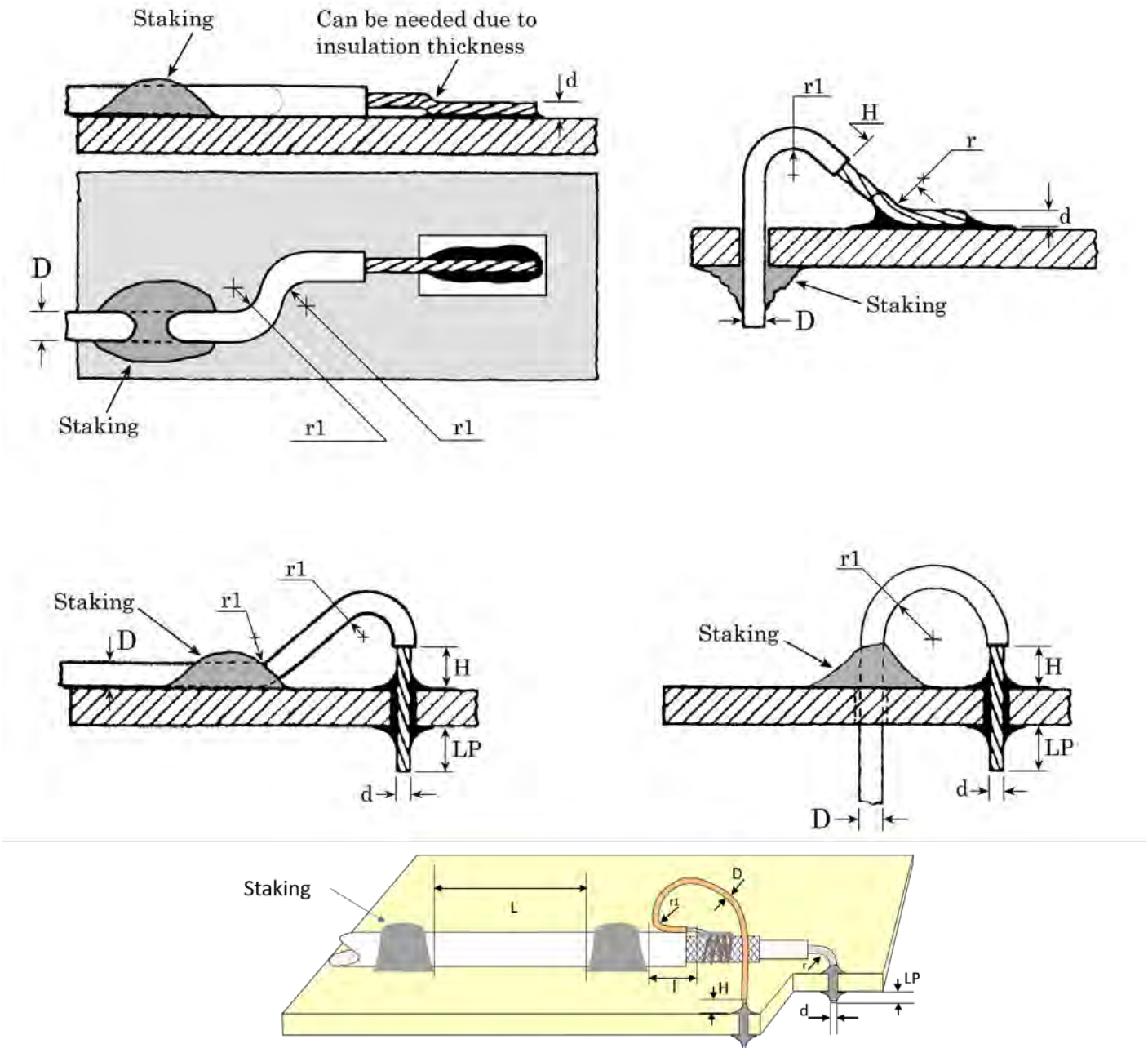


Figure 9-9: Connection of stranded wires to PCBs

Table 9-1: Dimensions for connections of stranded wires to PCBs

r ≥ 2 d	d	= conductor diameter
r1 ≥ 2 D	D	= outer wire diameter
1 mm ≤ H ≤ 2 mm	H	= insulation clearance
1,5 mm ± 0,8 mm	LP	= lead protrusion through board
50 mm max	L	=distance between supporting points
30 mm max	l	= distance between first staking and soldered connection

10
Assembly to terminals and to PCBs

10.1 Overview

Assembly consists of soldering and solderless technologies.

Soldering technologies are characterized by components that are soldered onto the PCB with a solder alloy using a soldering process for example solder iron, wave or reflow soldering.

Some components can be assembled without using a soldering process - solderless technology.

Both technologies can co-exist on the same board. In this case, solderless process is the last assembly operation.

10.2 General

10.2.1 Securing conductors

a. There shall be no relative motion between conductors and terminals during soldering or solder solidification.

b. Conductors shall not be temporarily constrained against spring-back force during solder solidification.

NOTE Residual stresses are produced in the lead material or solder joint.

10.2.2 Thermal shunts

a. Thermal shunts shall be used to protect thermally-sensitive components.

NOTE Example: Conductors, insulation, previously soldered connections and a non-exhaustive list of thermal sensitive components given hereafter:

- PS Capacitors according toMIL-PRF-49470
- CSR Tantalum Capacitors according to MIL-PRF-39003
- CRH capacitors according to MIL-PRF-83421
- Filters according to MIL-PRF-28861
- Coils according to MIL-PRF-39010

- Resistor Networks according to MIL-PRF-55342
- Thermistors according to MIL-PRF-23648
- Thermistors according to GSFC spec. S-311-P-18.

10.2.3 High-voltage connections

a. Soldered joints for corona suppression shall be performed in two stages with an intermediate inspection:

1. The first soldering stage produces a standard soldered connection in accordance with clause 12,
2. This connection is inspected for compliance with clauses 12.2 and 12.3,
3. The joint then has additional solder alloy added,
4. The second soldering stage produces a final joint, see Figure 10-1, having:
   (a) smooth convex fillets,
   (b) no discontinuities,
   (c) no severe changes in contour,
   (d) no sharp edges or points.

Figure 10-1: High voltage connection

10.3 Soldering of components, terminals and wires into plated through holes

10.3.1 General

a. Solder shall be applied only to the solder side of a plated-through hole.

b. Soldering of component and wires into plated-through holes shall be performed with soldering iron or wave soldering or selective wave soldering.

c. The soldering iron tip shall be pretinned.

d. The heated soldering iron tip shall be applied to the PCB pad.

e. If the thermal dissipation in the PCB is too high additional heating may be used to be able to achieve an acceptable solder joint on the component side.

NOTE 1 Too high thermal dissipation can be due to high thermal masses or locally adjacent heat sinks.

NOTE 2 Additional heating can be applied by pre-heating of the PCB or application of heat to both sides of the plated-through hole simultaneously.

f. Additional heating shall not damage the components or materials.

g. The process of additional heating shall be documented.

10.3.1.2 Solder fillets for wires and terminations

a. The molten solder shall flow around the termination and over the PCB pad.

b. Solder shall not obscure the contour of the conductor at the end of the insulation.

c. A conductor mounted as a lap termination shall have a heel fillet where it bends away from the pad.

d. On lap terminations where one side of a conductor is flush with the edge of the termination pad, a fillet of solder shall be present along at least 3 (three) of the four sides of the lead.

e. The fillet of solder along the lead shall extend up the side of the lead to a minimum distance of half the lead thickness or diameter.

10.3.1.3 Solder fillets for component leads in plated through-holes

a. On the solder side, the molten solder shall flow around the termination and over the PCB pad.

b. On the component side, the PCB pad shall show solder flow-through and a solder fillet between the lead and the pad for a minimum of 75 % of the circumference of the lead as illustrated in Figure 10-2.

c. Absence of component side wetting, due to high thermal dissipation, may be accepted when acceptable solder wetting is visible inside the plated-through hole, and the solder flow-through is minimum 90 % as illustrated in Figure 10-2.

d. In case requirement 10.3.1.3c cannot be verified by visual inspection, the solder joint may be accepted providing X-ray inspection is carried out and conforms to the following two criteria as illustrated in Figure 10-3.

   1. the maximum amount of voids is 25 %, and
   2. the solder flow through is 90 %.

e. If the solder flow-through is less than 90 %, the component shall be verification tested in compliance with requirements from clause 13.

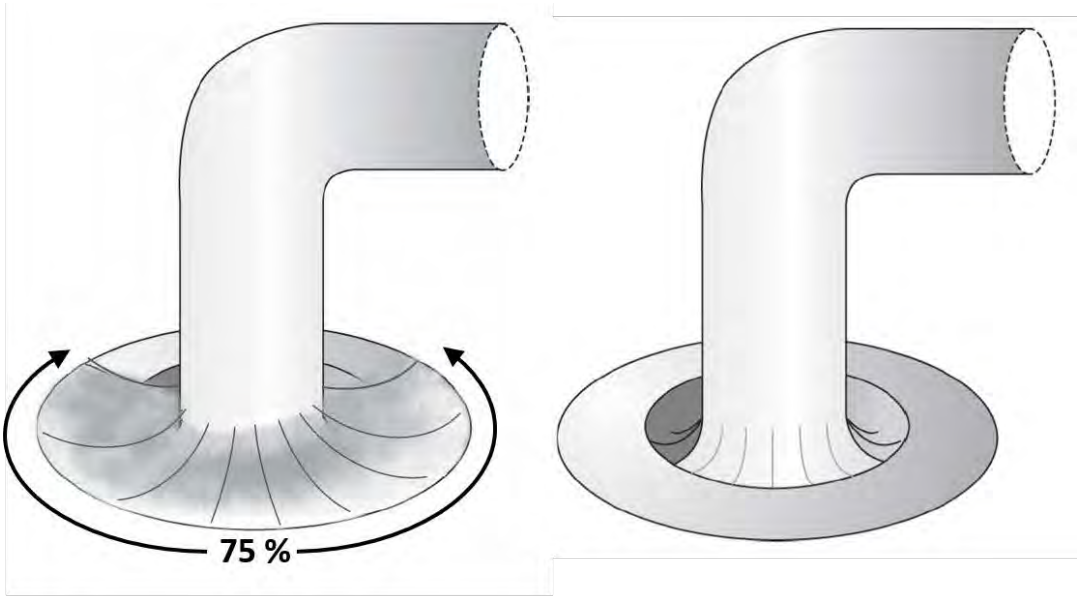


Figure 10-2: Minimum acceptable wetting on component side

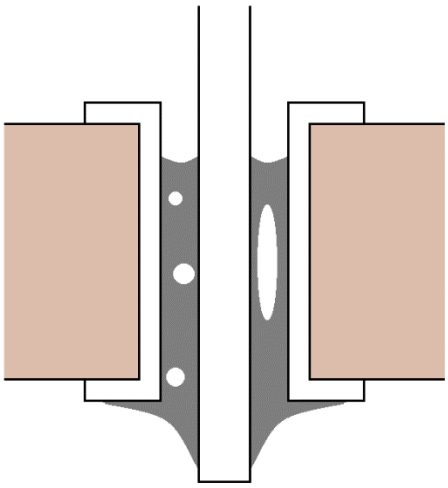


Figure 10-3: Minimum acceptable solder flow through and maximum voids during X-ray

10.3.2 Removal of solder on unpopulated PCB

a. Removal of solder shall be performed after the board has been submitted to bake out in compliance with clause 7.7.

b. Rework of plated through-holes in PCBs may be allowed up to maximum 25% per component position with a maximum of 3 (three) times for the same plated through hole.

NOTE Plated through-holes can be blocked from PCB manufacturer in case of small hole dimensions.

c. The number and location of reworks performed according to 10.3.2b shall be recorded in the traveller sheet of the board.

d. In case more that 25 % per component position are reworked, the removal of solder shall be classified as a repair and be performed in accordance with ECSS-Q-ST-70-28.

10.3.3 Solder rework

a. Rework of soldered PCB assemblies shall be done when the solder joint does not meet the acceptance criteria of clause 12.

b. Rework shall be carried out according to ECSS-Q-ST-70-28.

c. A joint shall not be reworked more than 3 (three) times.

NOTE For reworking, the solder can be completely removed from the termination.

d. The total number of solder reworks, including the ones done prior to soldering according to clause 10.3.3b shall not exceed three times per PCB pad.

10.3.4 Repair and modification

a. Any repairs or modifications shall be in accordance with ECSS-Q-ST-70-28.

10.4 Soldering with wave or selective wave machine

10.4.1 PCB design constraints

a. When assembly process is intended to be done with wave soldering process, PCB design shall respect clause 14.3.3 of ECSS-Q-ST-70-12.

b. The design constraint specification specified in 10.4.1a should at least, include the following statements:

1. Avoid solder bridging, circuit tracks that are spaced close together should be orientated in line with the pass direction of the solder wave.
2. Avoid large heat sink areas for ground planes and leads closely connected to massive metal parts.

10.4.2 Rework

a. Rework shall be carried out according to ECSS-Q-ST-70-28.

b. A maximum of 5 % rework on each wave soldered circuit shall be acceptable for wave soldered joints

NOTE Deficient wave soldered connections are caused most frequently by the movement of component leads during solidification, the presence of solder alloy within stress relief bends and the entrapment of machine oils and solder fluxes within the solder fillet. Rework of any nature is costly. It involves not only the risk of irreparable lifted pads and measling, but also the possibility of heat damage to sensitive components.

10.5 Soldering of Surface Mount Components

10.5.1 General

a. Components shall not be mounted on flexible substrates.

NOTE See definition of flexible PCB in ECSS-Q-ST-70-60.

b. Components shall not be stacked nor bridge the space between other components or terminals.

c. Positioning of components shall not reduce the specified minimum electrical clearance to adjacent tracks or other metallized elements in conformance with requirements from clause 13 and clause 14 of ECSS-Q-ST-70-12.

d. Solder joints on component terminations shall be homogenous in volume.

NOTE Figure 10-5 to Figure 10-17 show minimum and maximum height values on the same component drawing for illustration purpose.

e. Maximum tilt limit shall not exceed 10° as shown in Figure 10-4.

NOTE Tilt is the angle between the PCB plane and the component axis both along length and width.

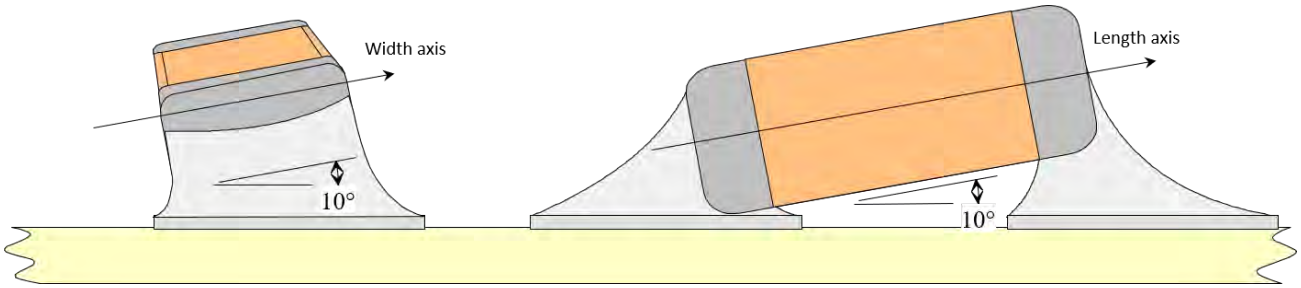


Figure 10-4 Maximum tilt for assembled chip component

f. Non-axial-leaded components shall be mounted with all leads seated on a terminal area to provide mechanical strength.

g. The component shall be centred on its footprints such as the minimum lap contact length is fulfilled.

h. On lap terminations where one side of a conductor is flush with the edge of the termination pad, a fillet of solder shall be present along at least 3 (three) of the four sides of the lead.

i. The fillet of solder along the lead shall extend up the side of the lead to a minimum distance of half the lead thickness or diameter.

j. Solder shall cover and wet the solderable surfaces as specified in clause 12.2.

k. The entire termination length shall be wetted.

l. The footprint shall be such that the entire termination of the component lies on its associated footprint on the finished board.

m. Soldering to gold with SnPb alloys shall not be performed except the case specified in the requirement 6.9.2a.

n. The component footprints on FM shall be the same as used in verification programme.

o. Components verified by similarity shall use same design principle for the footprint.

p. The component positioning shall be such that visual inspection can be undertaken.

q. If visual inspection of a fully populated assembly is not possible, the assembly and inspection shall be made in steps enabling visual inspection.

r. In case of mounting with artificial stand-off, the process shall be repeatable within ± 50 μm.

s. Artificial stand-off value shall be documented in procedure.

t. The footprint design shall be done in such way as to avoid, during soldering, contact between the component and the soldering tip.

u. Any deviation to requirements from clause 10.5.2, 10.5.3, 10.5.4, 10.5.5 and10.5.6 shall be demonstrated by verification in compliance with requirements from 13.

10.5.2 Rectangular and square end-capped and end-metallized leadless chip

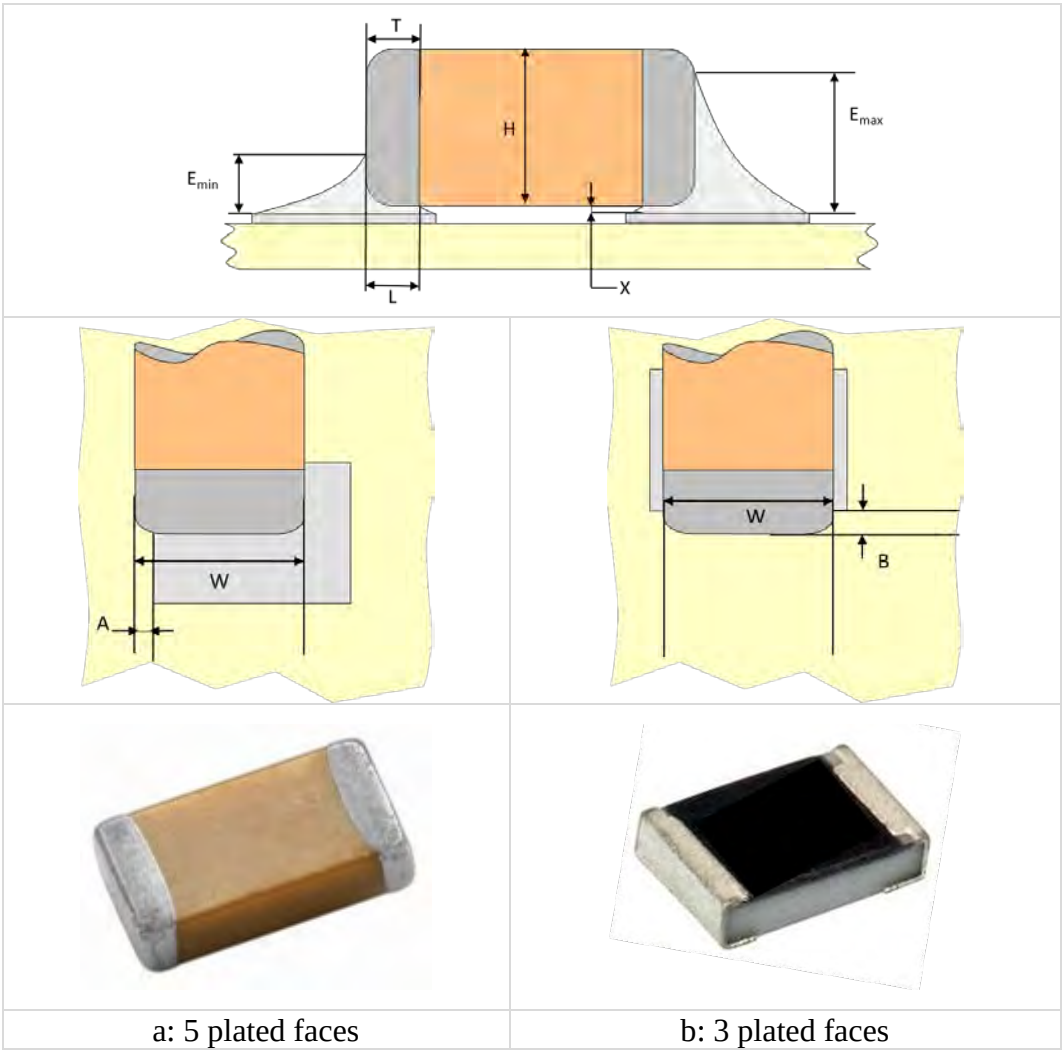
10.5.2.1 Ceramic chip component

a. There shall be no discernible discontinuities in the solder coverage of the terminal areas of components.

b. Solder shall not encase any portion of the body of the component following reflow.

c. The solder joints to these components shall meet the dimensional and solder fillet requirements of Figure 10-5 and Table 10-1.

NOTE End-capped and end-metallized components having terminations of a square or rectangular configuration (such as chip resistors, chip capacitors and similar leadless discrete components) can have three or five face terminations, as shown in “a” and “b” in Figure 10-5.



a: 5 plated faces | b: 3 plated faces

Figure 10-5: Mounting of rectangular and square end-capped and end-metallized components

Table 10-1: Dimensional and solder fillet for rectangular and square end capped components

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
End overhang	B	Not permitted
Minimum termination contact length	L	0,75 × T on one side of the component only 100 % for assembly sensitive components
Minimum fillet height	E_{min}	X + 0,3 × H or X + 0,5 mm whichever is less
Maximum fillet height*	E_{max}	*: only for chip capacitor $E_{max} \leq H$
Solder Stand-off (elevation)	X	Present
Maximum tilt limit	in accordance with 10.5.1d	10°
Termination width	W	
Component height	H	
Termination length	T	

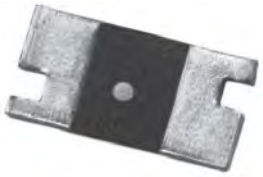
10.5.2.2 Metallic chip component

a. There shall be no discernible discontinuities in the solder coverage of the terminal areas of components.

b. Solder shall not encase any portion of the body of the component following reflow.

c. The solder joints to these components shall meet the dimensional and solder fillet requirements of Figure 10-5 and Table 10-1.

NOTE Figure 10-6 shows examples of metallic chip components.



CSM 2512

Resistor with metallic terminations

Figure 10-6: Examples of metallic chip components

10.5.3 Cylindrical and square end-capped components

a. Solder joints to components having cylindrical terminations shall meet the dimensional and solder fillet requirements of Figure 10-7 and Table 10-2.

b. Solder joints to components having square terminations shall meet the dimensional and solder fillet requirements of Figure 10-8 and Figure 10-3.

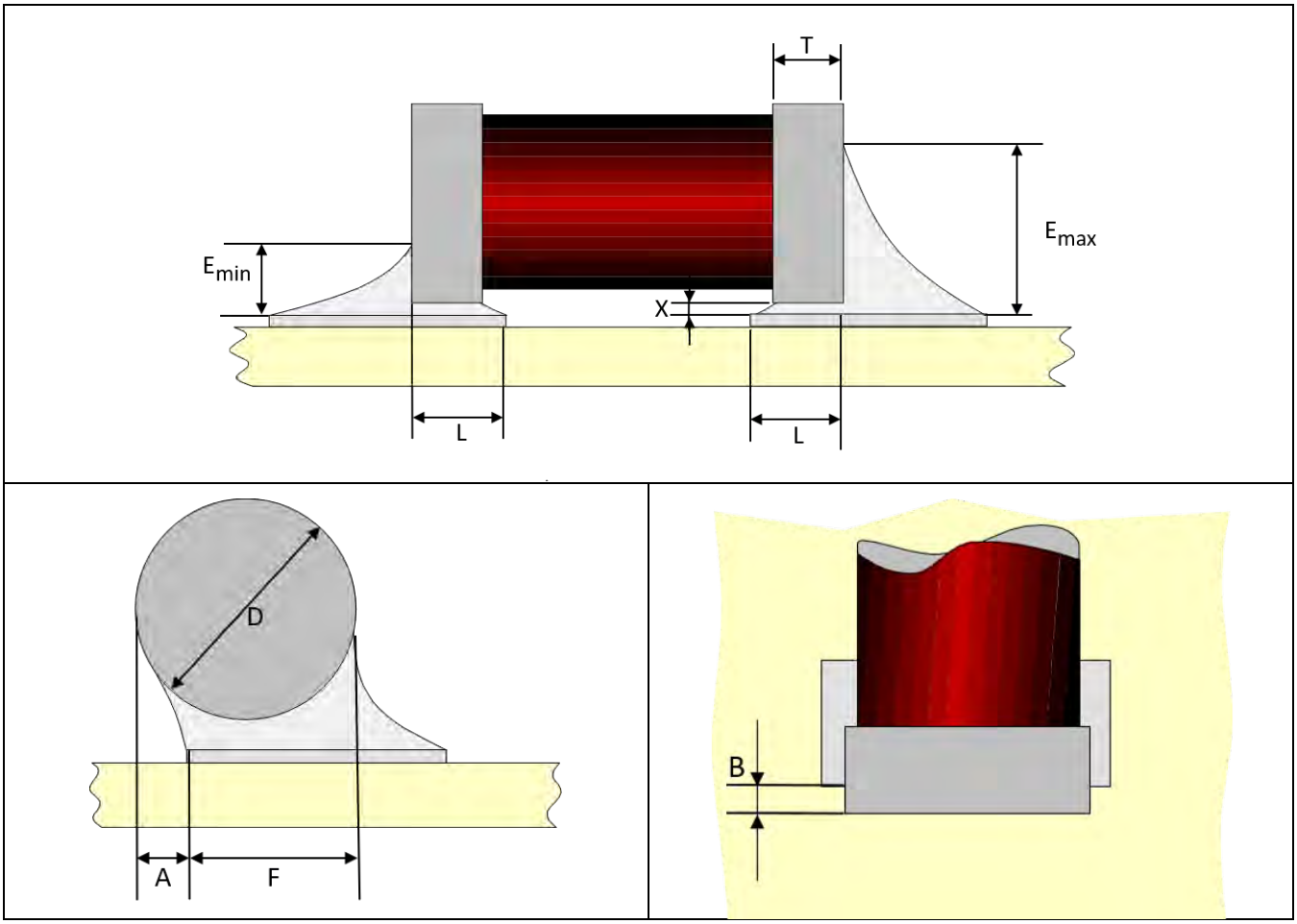


Figure 10-7: Mounting of cylindrical end-capped components

Table 10-2: Dimensional and solder fillet for cylindrical end-capped components

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,25 × D (diameter)
End overhang	B	Not permitted
Minimum fillet width	F	0,5 × D
Minimum fillet height	E_{min}	X + 0,3 × D or X + 1,0 mm whichever is less
Maximum fillet height	E_{max}	D
Minimum termination contact length	L	0,75 × T on one side of the component only 100% for assembly sensitive components
Stand-off (elevation)	X	Present
Maximum tilt limit	in accordance with 10.5.1d	10°
Termination diameter	D	
Termination length	T	

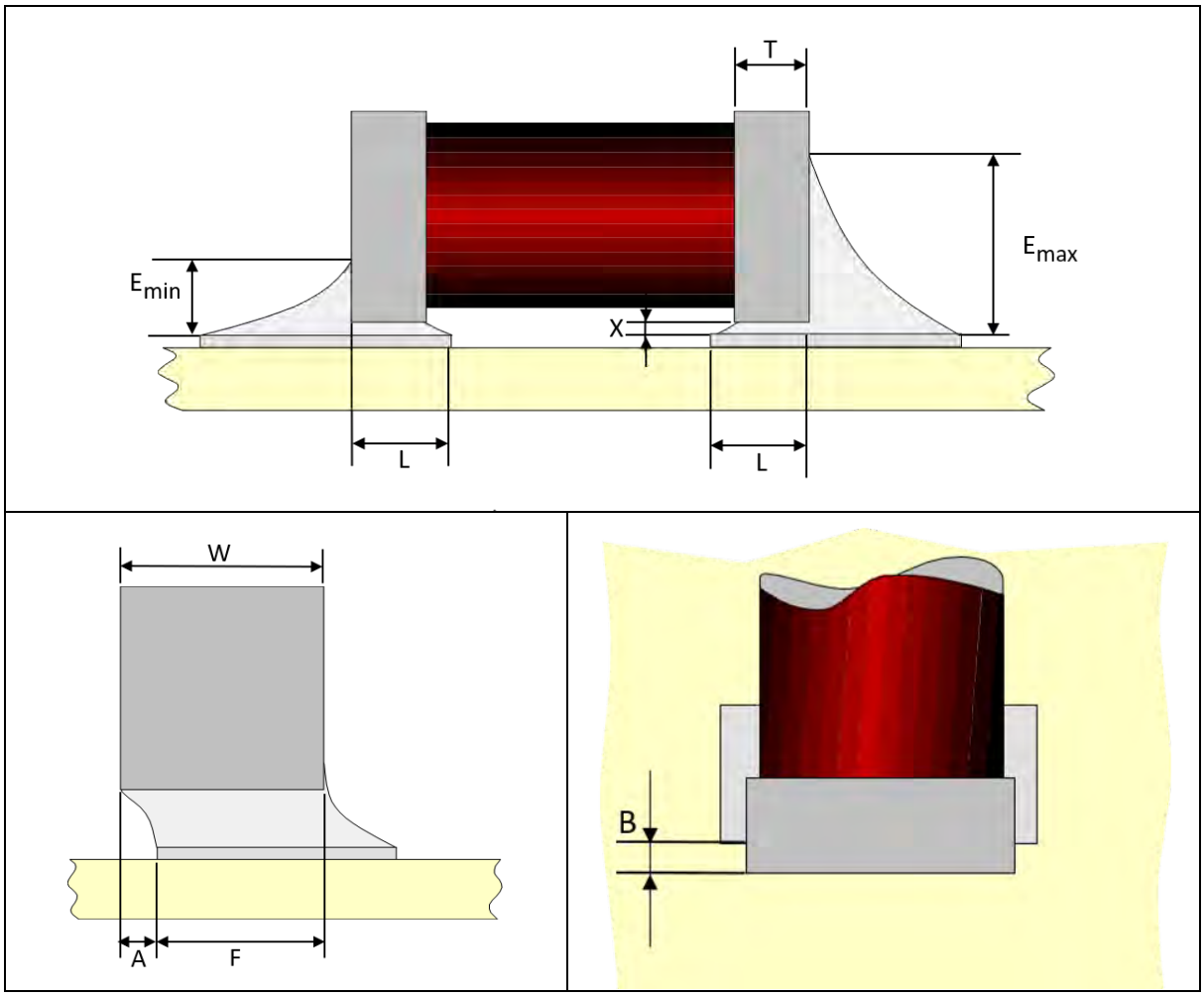


Figure 10-8: Mounting of square end-capped components

Table 10-3: Dimensional and solder fillet for square end-capped components

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,25 × W (square width)
End overhang	B	Not permitted
Minimum fillet width	F	0,5 × W
Minimum fillet height	E_{min}	X + 0,3 × W or X + 1,0 mm whichever is less
Maximum fillet height	E_{max}	W
Minimum termination contact length	L	0,75 × T on one side of the component only 100% for assembly sensitive components
Stand-off (elevation)	X	Present
Maximum tilt limit	in accordance with 10.5.1d	10°
Termination length	T	
Termination width	W	

10.5.4 Bottom terminated chip components

a. Devices having metallized terminations on the bottom side only shall meet the dimensional and solder fillet requirements of Figure 10-9 and Table 10-4.

NOTE Examples of components from this family are SMD coils and QFN.

b. Solder fillet shall show acceptable wetting on all visible sides.

c. Assembly shall be inspected with X-ray equipment according to clause 5.6.20.

d. Assembly shall be inspected with X-ray according to criteria defined in requirements 12.4a.

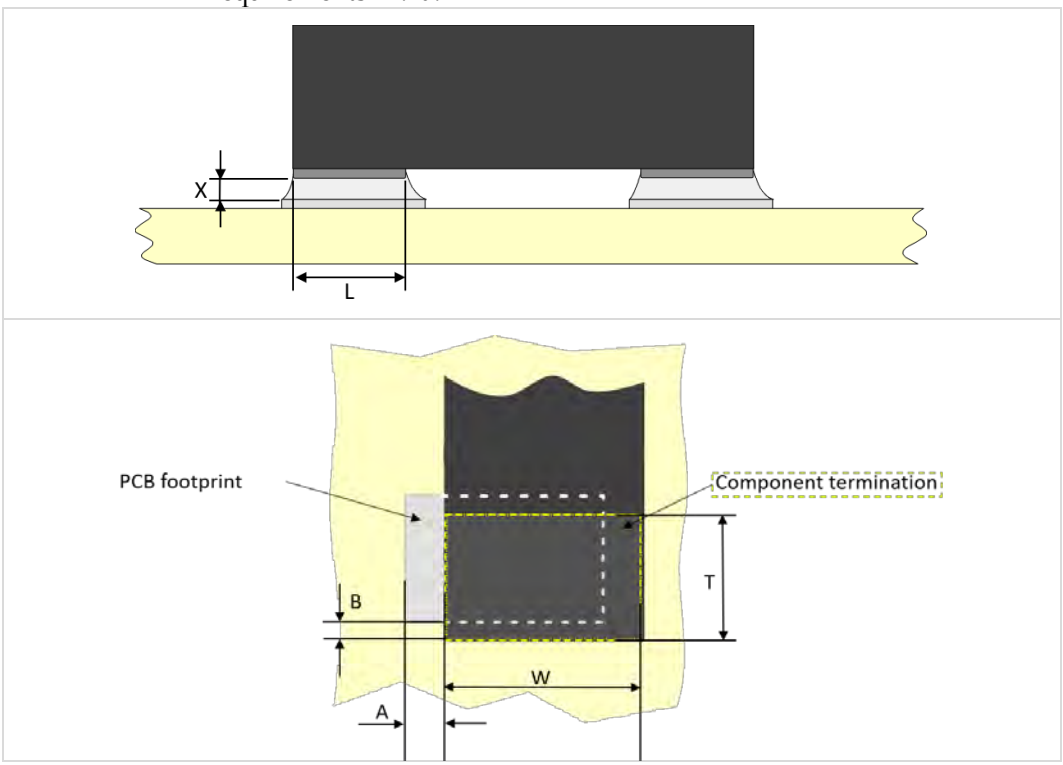


Figure 10-9: Mounting of bottom terminated chip component

Table 10-4: Dimensional and solder fillet for bottom terminated chip components

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W Not permitted for assembly sensitive component
End overhang	B	Not permitted
Minimum termination contact length	L	0,75 × T on one side of the component only Entire termination for assembly sensitive components
Solder Stand-off (elevation)	X	Present
Maximum tilt limit	in accordance with 10.5.1d	10°
Component termination width	W	
Termination length	T	

10.5.5 L-Shape inwards components

a. Components having L-shape inwards terminals shall meet the dimensional and solder fillet requirements of Figure 10-10 and Table 10-5.

b. Solder fillet shall be visible on the side of the terminal on the connection.

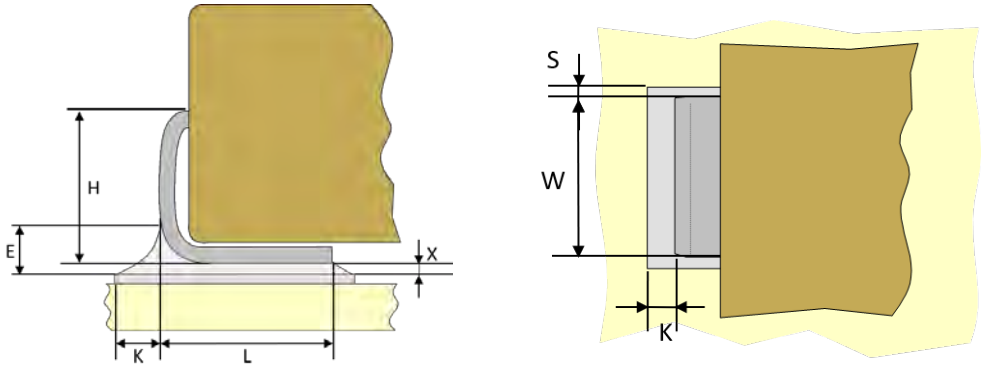


Figure 10-10: Mounting of components with "L-shape inwards" leads

Table 10-5: Dimensional and solder fillet for "L-shape inwards" components

Parameter	Dimension	Dimensions limits
Minimum heel fillet height	E	(0,25 x H) +X or X +1mm whichever is less
Minimum distance to footprint edge	K	0,2 mm
Minimum termination contact length	L	0,75 × T on one side of the component only 100% of T for assembly sensitive components
Stand-off (elevation)	X	Present
Side of terminal wetting	S	Evidence of component termination solder wetting
Lead height	H	
Lead width	W	

10.5.6 Leadless component with plane termination

a. Leadless components with plane termination may have a metallic plane or non-metallic plane termination.

NOTE Example of a metallic plane is: TO276 package (SMD0,5, SMD1 and SMD 2).

b. Leadless components with plane termination shall meet the dimensional and solder fillet requirements of Figure 10-11 and Table 10-6.

c. Assembly shall be inspected with X-ray equipment according to clause 5.6.20.

d. Assembly shall be inspected with X-ray according to criteria defined in requirements 12.4a.

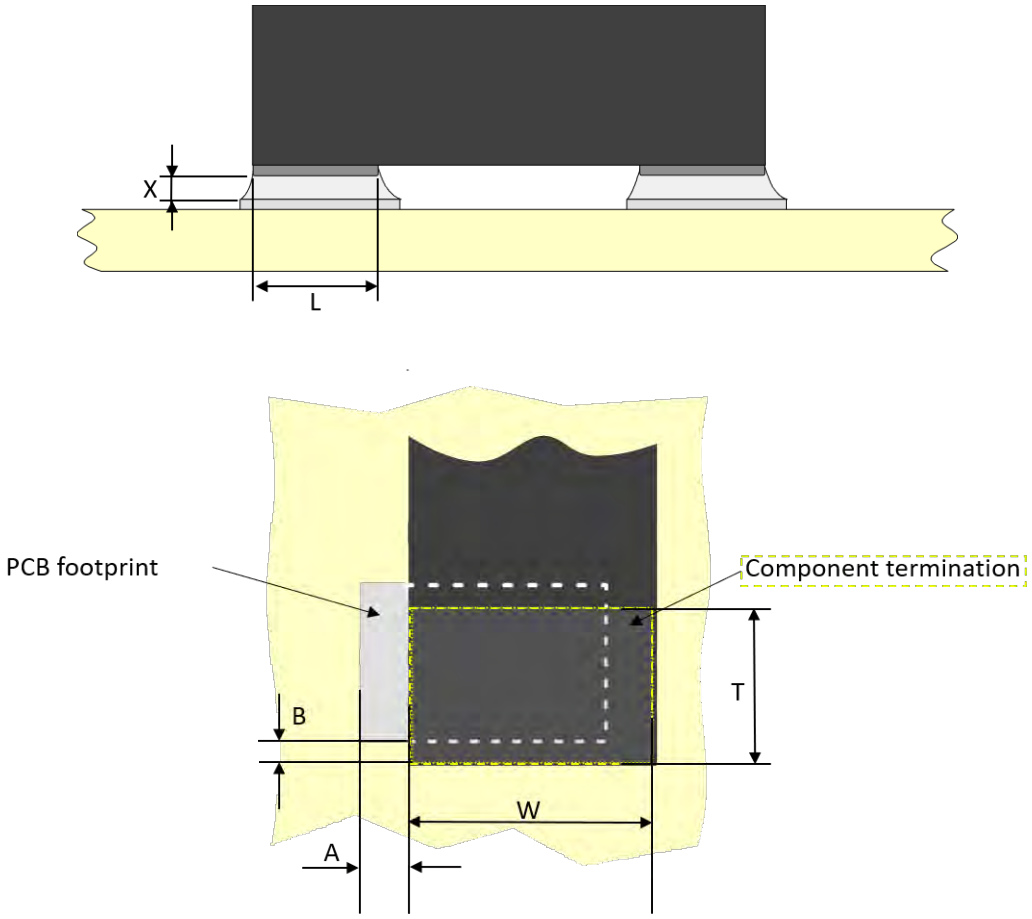


Figure 10-11: Mounting of leadless component with plane termination

Table 10-6: Dimensional and solder fillet for leadless component with plane termination

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W Not permitted for assembly sensitive component
End overhang	B	Not permitted
Minimum termination contact length	L	Entire termination of component
Solder Stand-off (elevation)	X	Present
Maximum tilt limit	in accordance with 10.5.1d	10°
Component termination width	W	
Termination length	T	

10.5.7 Leaded component with plane termination

a. Leaded components with plane termination shall meet the dimensional and solder fillet requirements of Figure 10-12 and Table 10-7.

b. Solder fillet shall be visible in the heel fillet.

c. Termination plane shall be inspected with X-ray equipment according to clause 5.6.20 and according to criteria defined in 12.4a.

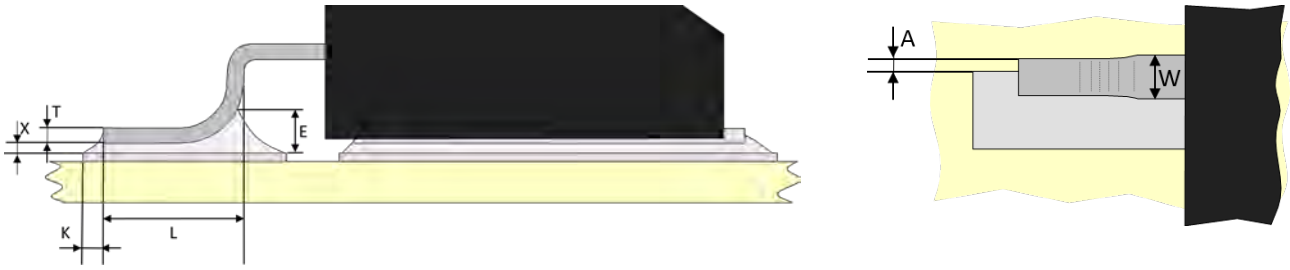


Figure 10-12: Mounting of leaded components with leads with plane termination

Table 10-7: Dimensional and solder fillet for leaded components with plane termination

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum distance to footprint edge at toe	B	0,20 mm
Minimum distance to footprint edge at heel	K	0,5 × W
Minimum termination contact length	L	full lap connection soldered
Minimum heel fillet height	E	X + T
Solder Stand-off	X	Present
Lead thickness	T	
Lead width	W	

10.5.8 Castellated chip carrier components

a. Joints to castellated component terminations shall meet the dimensional and solder fillet requirements of Figure 10-13 and Table 10-8.

NOTE The stand-off enables adequate cleaning beneath the assembled LCCC and also enhances solder fatigue life.

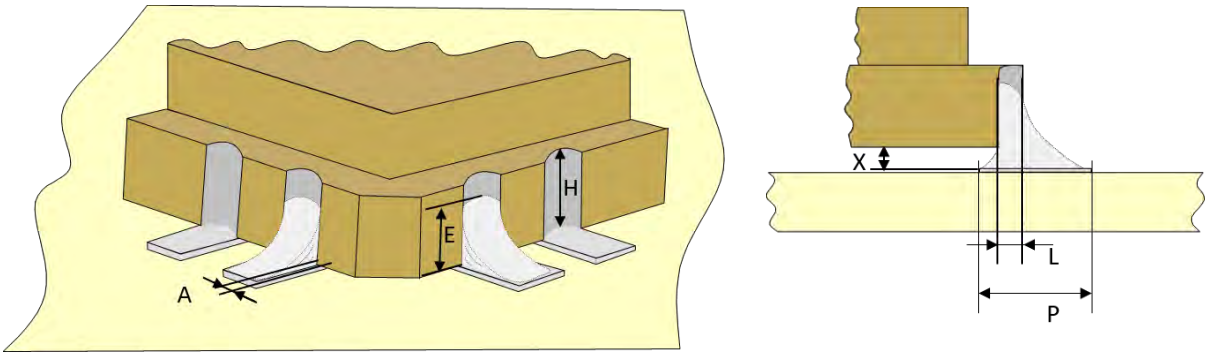


Figure 10-13: Mounting of castellated chip carrier components

Table 10-8: Dimensional and solder fillet for castellated chip carrier components

Parameter	Dimension	Dimension limits
Maximum side overhang	A	Zero
Minimum fillet height	E	0,75 × H
Solder Stand-off (elevation)	X	Present
Minimum termination contact length	L	Entire termination of component
Castellation metallisation height	H	
Pad length	P	

10.5.9 Flat pack and gull-wing leaded components with round, rectangular, ribbon leads

a. Solder joints formed to flat pack and gull-wing leaded components with round, rectangular, ribbon leads shall meet the dimensional and solder fillet requirements of Figure 10-14 and Table 10-9.

b. Solder fillet shall be visible on the side of the terminal lap connection.

c. Surface mount moulded magnetics components shall meet the dimensional and solder fillet requirements of Figure 10-14 and Table 10-9.

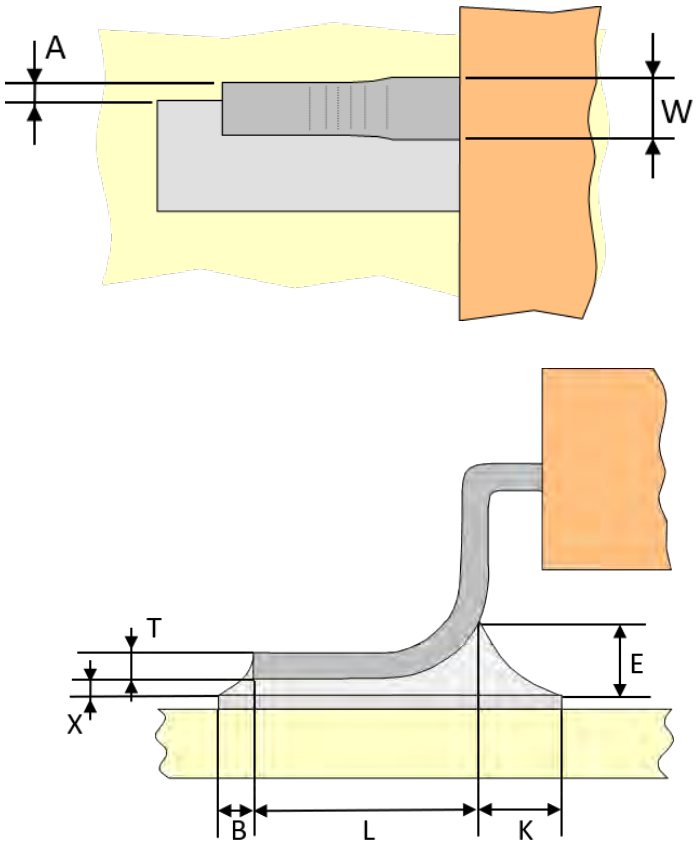


Figure 10-14: Mounting of gull-wing leaded components with round, rectangular, ribbon leads

Table 10-9: Dimensional and solder fillet for gull-wing leaded components with round, rectangular, ribbon leads

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum distance to footprint edge at toe	B	0,20 mm
Minimum distance to footprint edge at heel	K	0,5 × W
Minimum termination contact length	L	100% of D
Minimum heel fillet height	E	X + T
Solder Stand-off	X	Present
Lead thickness	T	
Lead width	W	

10.5.10 Components with “J” leads

a. Solder joints formed to “J” and “V” shaped leads shall meet the dimensional and solder fillet requirements of Figure 10-15 and Table 10-10

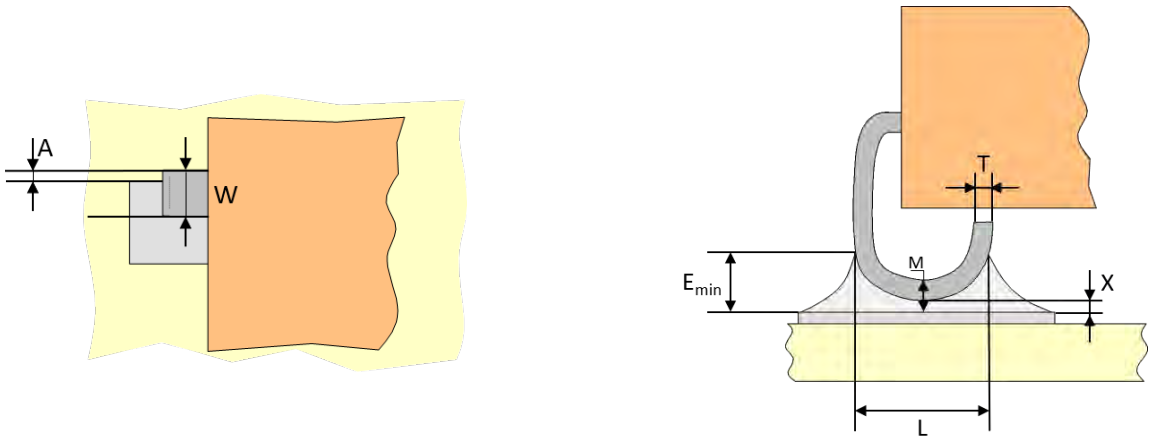


Figure 10-15: Mounting of components with “J” leads

Table 10-10: Dimensional and solder fillet for components with “J” leads

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum termination contact length	L	100% of the pad
Minimum heel fillet height	E_{min}	>M (M=X+T)
Minimum stand-off	X	Present
Lead thickness	T	
Lead width	W	

10.5.11 Components with ribbon terminals without stress relief

a. Solder joints formed shall meet the dimensional and solder fillet requirements of Table 10-11 and Figure 10-16.

b. The degolding and pretinning zone shall be larger than the PCB footprint.

NOTE The aim is to prevent soldering to gold plated surfaces

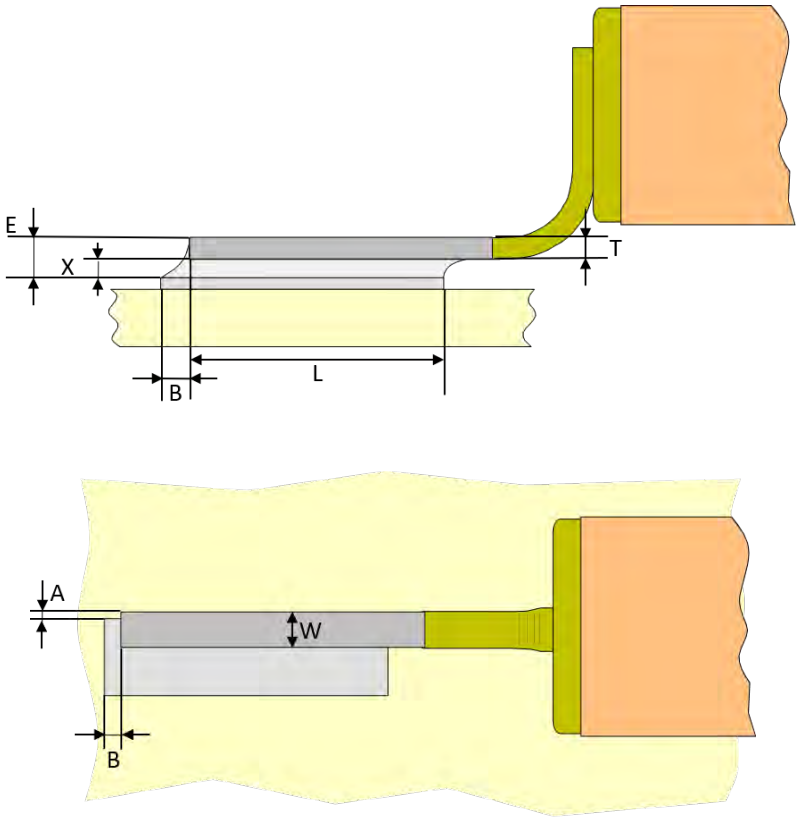


Figure 10-16: Mounting of components without stress relief

Table 10-11: Dimensional and solder fillet for components without stress relief

Parameter	Dimension	Dimensions limits
Maximum side overhang	A	≤ 0,1 x W
Minimum distance to footprint edge at toe	B	≥ 0,20 mm
Stand-off	X	Present
Minimum termination contact length	L	3xW with full lap soldered connection
Maximum tilt limit	in accordance with 10.5.1d	10°
Lead thickness	T	
Lead width	W	

10.5.12 Stacked modules components with leads protruding vertically from bottom

a. Stacked module components shall meet the dimensional and solder fillet requirements of Figure 10-17 and Table 10-12.

b. Solder fillet shall be visible in the heel fillet.

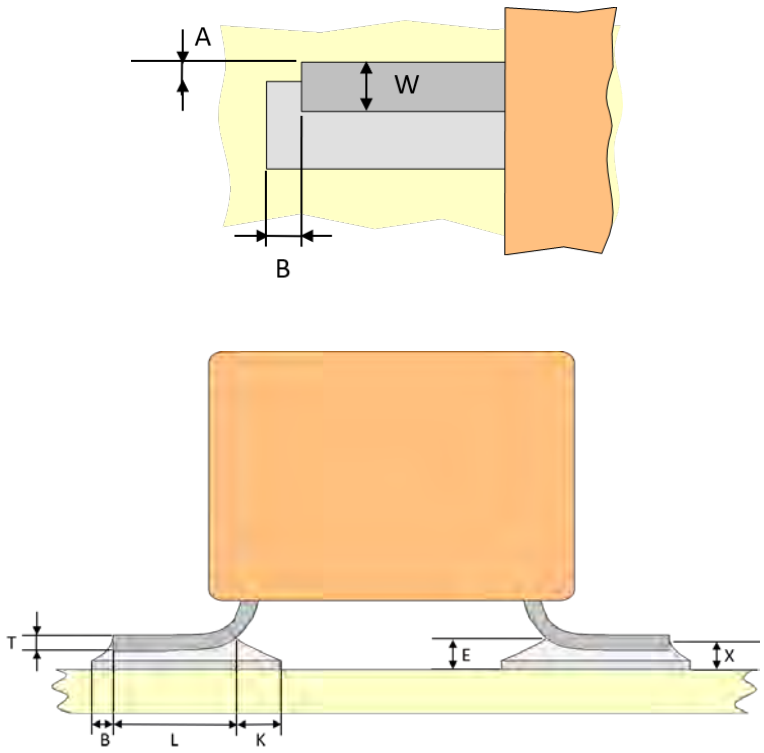


Figure 10-17: Mounting of stacked module components with leads protruding vertically from bottom

Table 10-12: Dimensional and solder fillet for stacked module components with leads protruding vertically from bottom

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum distance to footprint edge at toe	B	0,20 mm
Minimum distance to footprint edge at heel	K	0,5 × W
Minimum termination contact length	L	full lap connection soldered
Minimum heel fillet height	E	Wetting solder visible in the heel fillet, X+ 0,5T
Solder Stand-off	X	Present
Lead thickness	T	
Lead width	W	

10.5.13 Area array components

a. The outer row of solder joints to area array components shall be visually inspected by looking from the side in accordance with the requirements in clause 10.5.1, Table 10-13 and with the visual rejection criteria specified in clause 12.3.

b. Solder joints shall be inspected using X-ray techniques in accordance with clause 5.6.20 and according to criteria defined in 12.4.

NOTE 1 As it is impossible to visually inspect solder joints to area array components, reliability of these components cannot be assured by inspection and rework. Even using X-Ray techniques, some types of defect are difficult to detect. Therefore, reliability of these solder joints can only be assured by robust process control.

NOTE 2 Examples of typical area array components are shown in Figure 10-18 and Figure 10-19.

c. X-ray techniques shall be used to verify the acceptable wetting, the absence of bridge, solder balls and minimum electrical clearance.

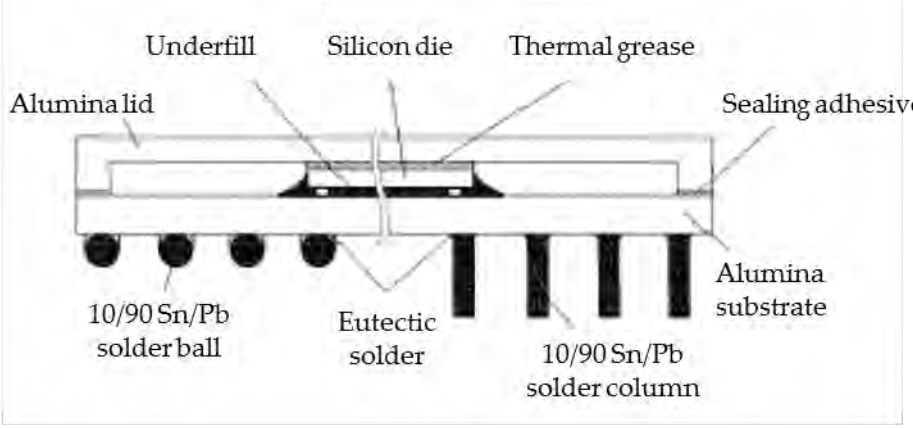


Figure 10-18: Typical ceramic area array showing ball grid array configuration on left and column grid array on right (CBGA & CCGA)

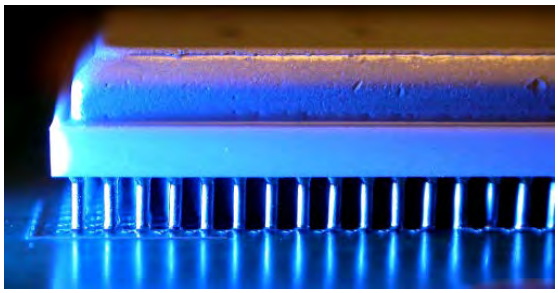


Figure 10-19: Typical assembled CCGA component

Table 10-13: Dimensional and solder fillet for area array components

Parameter	Dimension limits
Misalignment	No footprint overhang
BGA ball	Collapse of BGA ball does not violate minimum electrical clearance or become less than 0,10 mm
Maximum component height	Overall height of component does not exceed maximum specified
Soldered connection	BGA balls contact and wet to the land forming a continuous connection CGA solder columns contact and wet to the land forming a continuous connection
Solder balls	No solder balls
Maximum CGA column tilt	10°
D = Ball or column diameter	

10.6 Solderless components

a. Solderless assembly configurations shall be considered as interconnections.

NOTE Pressfit connectors are not covered by this standard.

b. Solderless connection configuration shall be identified in the DCL.

c. Solderless components shall meet the dimensional and placement requirements of Table 10-14.

d. The component shall be centred on its footprints.

Table 10-14: Dimensional and placement for solderless components

Parameter	Dimension	Dimension limits
Maximum side overhang	0	No overhang permitted
Contact	X	Visible

11
Post soldering process requirements

11.1 Cleaning of PCB assemblies

11.1.1 General

a. The verification of the PCB cleanliness shall be performed for the following cases:
   1. for the first verification programme performed by a company,
   2. when the conditions of Table 13-2 request it.

b. When the solder has solidified and cooled, flux and residue shall be removed from soldered connections using a solvent in accordance with clause 6.4.

c. Solvent shall be applied in such a manner that avoids its penetration under wire insulation and prevents its entry into the interior of parts.

d. Flux and residue shall be removed within a maximum period of 8 hours after soldering operations.

NOTE It is good practice to remove flux as soon as possible because even rosin fluxes are difficult to remove after longer ageing.

e. PCB assemblies shall not be immersed in cleaning solvents for more than 30 minutes for each cleaning operation.

NOTE Long immersion times can promote galvanic corrosion between adjacent metallic surfaces.

11.1.2 Ultrasonic cleaning

a. Ultrasonic cleaning shall not be used for PCBs populated with components.

11.1.3 Monitoring for cleanliness

11.1.3.1 Cleanliness testing

a. The effectiveness of the cleaning process employed for PCB assemblies (post-soldering) shall be tested using a sodium chloride (NaCl) equivalent ionic contaminants test in accordance with clause 11.1.3.4.

b. Cleanliness testing may be omitted for solder assemblies using only pure rosin (ROL0) fluxes as defined in Table 6-2.

11.1.3.2 Testing frequency

a. For fluxes, other than pure rosin, cleanliness testing shall be done:
   1. at maximum intervals of six months,
   2. following a change in flux materials,
   3. following a change in process parameters,
   4. following actions affecting cleanability.

      NOTE Statistical control methods can be used to control continuous solvent cleaning processes.

b. The supplier shall implement and maintain records of test results.

   NOTE The records can aid early detection of a trend towards nonconformance.

c. When a test result is unacceptable, all PCB assemblies cleaned since the last successful test shall be subject to review by the Approval Authority in accordance with ECSS-Q-ST-20.

11.1.3.3 Test limits

a. The sodium chloride (NaCl) ionic contaminants equivalence value shall be less than 0,70 μg/cm² of PCB surface area.

11.1.3.4 Test method

a. Sodium chloride (NaCl) equivalent ionic contaminants shall be measured as follows:
   1. Use a solution of 75 % isopropyl alcohol and 25 % deionized water for the sodium chloride (NaCl) equivalent ionic contaminants test.
   2. Calibrate the equipment using a sodium chloride solution of known quantity and composition.

b. Testing shall be performed according to the equipment manufacturer's specification.

c. The cleanliness test values shall be as follows:
   1. Starting resistivity: greater than 20×10^6 Ω cm.
   2. Ending value: less than 0,70 μg/cm².

      NOTE ESA STM-275 contains an evaluation of PCB cleanliness testing.

11.2 Staking and bonding

a. Adhesive shall be selected in conformance with clause 6.11.

   NOTE Some surfaces can be prepared to enhance the adhesion (e.g. by mechanical abrasion).

b. Adhesive shall be mixed and cured in accordance with the manufacturer's recommendations.

c. The process of mixing and applying the adhesive shall be documented by a written procedure or by configured drawings which define the location of the adhesive, the shape and the spread area (between component bottom surface and substrate upper surface).

d. The adhesive shall not be in contact with the terminal or negate the stress relief of the component, nor come into contact with surrounding components.

e. All PTH components weighing more than 5g shall be staked.

NOTE Staking and bonding can be applied before or after soldering depending on configuration.

f. All SMD weighing more than 5 g should be staked.

NOTE 1 This is to minimize shock and vibration loading on the leads

NOTE 2 The adhesive compound can be applied either before or after soldering in conformance with the supplier's process identification document.

g. Staking and bonding shall be performed on clean surfaces.

h. Staking and bonding shall not be performed on fused tin lead unless the tin lead surface is limited to < 25 % by area of the bonding surface and demonstrated by verification as specified in clause 13.

i. Spread of staking and bonding material onto surrounding areas shall not be accepted unless it does not reduce the volume of the initial bonding joint.

j. Staking and bonding material shall not be in contact with surrounding components.

k. Staking and bonding material shall not be in contact with glass bodied components.

NOTE It is good practice to use a sleeve between glass body and adhesive material.

11.3 Conformal coating, potting and underfill

a. Pottings, underfill and conformal coatings shall not negate stress-relief of component leads or connecting wires.

NOTE Underfill can be applied before or after soldering depending on configuration.

b. Pottings, underfill and conformal coatings shall not have adverse effects upon materials used on the substrate, or components attached thereon.

NOTE 1 This is particularly important at low service temperatures.

NOTE 2 The coefficient of expansion, glass transition temperature and modulus of adhesives used under components for thermal reasons, for achieving stand-off heights or mechanical support during vibration, can be considered not to degrade the solder joint reliability when additional stress is put on the solder joints.

12
Final inspection

12.1 General

a. Each soldered connection shall be visually inspected in accordance with the criteria specified in the requirements 12.1b and 12.1c.

NOTE 1 Annex F includes examples of acceptable and unacceptable workmanship for SMDs.

NOTE 2 Annex E includes examples of acceptable and unacceptable workmanship for PTHs.

b. Components and conductors shall not be physically moved prior or during visual inspection.

c. The substrate, solder joint, components and component position, shall be inspected for SMDs in accordance with the requirements from clause 10.5 and for PTHs in accordance with requirements from clauses 8.2, 9 and 10.3.

d. The assembly shall be visually inspected in two steps with the following methodology:

1. Visual inspection of the assembly is aided by magnification appropriate to the size of the connections between 4x and 10x.
2. Detailed inspection is performed with a minimum magnification 20x.

e. Additional magnification shall be used to resolve suspected anomalies or defects up to 40x.

f. X-ray inspection shall be applied when there are hidden solder joints that are not visually accessible.

NOTE Rejection criteria are defined in clause 12.4.

12.2 Visual acceptance criteria

a. Acceptance criteria for visual inspection shall be as following:

1. a clean, smooth satin to bright undisturbed surface,
2. solder fillets between conductor and termination areas,
3. for solder fillets of plated-through hole connections, the criteria in clause 10.3 apply,
4. visible contour of wires and leads such that their presence, direction of bend and termination end can be determined,

5. complete wetting as evidenced by a low contact angle between the solder and the joined surfaces,
6. acceptable amount and distribution of solder,
7. absence of any of the defects specified in clause 12.3,
8. high-voltage connections in accordance with clause 10.2.3,
9. stress relief,
10. exposed base metal at the ends of cut leads in the soldered connection,
11. exposed base metal at the ends of cut wire,
12. exposed base metal on sides of tracks and soldering pads on substrate,
13. delamination within break-out regions for processed multi-panel boards in accordance with Table 10-45 of ECSS-Q-ST-70-60.

NOTE Illustrations of criteria are given in Annex F and Annex E.

12.3 Visual rejection criteria

a. The following non-conformances shall be cause for rejection:

1. charred, burned or melted insulation of parts,
2. conductor pattern separation from circuit board,
3. burns on base materials,
4. continuous discolouration between two conductor patterns,
5. excessive solder including peaks, icicles and bridging, see clause 10.3.2,
6. contaminated solder joints including flux, lint and extraneous material,
7. flux residue, solder splatter, solder balls, or other foreign matter on circuitry, beneath components or on adjacent areas,
8. dewetting,
9. insufficient solder,
10. pits, holes or voids, or exposed base metal except criteria specified 12.2a.10,
11. granular or disturbed solder joints,
12. fractured or cracked solder connection,
13. cut, nicked, gouged or scraped conductors or conductor pattern,
14. incorrect conductor length,
15. incorrect direction of clinch or lap termination on a PCB,
16. damaged conductor pattern,
17. bare copper or base metal, except criteria specified 12.2a.10,12.2a.11,12.2a.12
18. soldered joints made directly to gold-plated terminals or gold-plated conductors using tin-lead solders,
19. cold solder joints,
20. component body embedded within solder fillet,
21. open solder joints,
22. probe marks present on the metallization of chip components caused by electrical testing after assembly,

23. glass seal does not in compliance to MIL-STD-883 Method 2009.8,
24. impaired stress relief,
25. measling which violates the minimum insulation distance,
26. delamination, except criteria specified in 12.2a.13,
27. exposed base metal except criteria specified 12.2a.10,
28. cracks detected in glass diodes outside the relevant components procurement standard,
29. bent connector pins outside the relevant components procurement specification,
30. modified component leads after assembly even if still within that defined in procurement standard of the item,
31. damage of the lead, component or PCB beyond that defined in the procurement standard of the item,
32. reduced insulation between leads down to unacceptable value,
33. degraded insulation material of the connector in contact area,
34. bubble or void in the conformal coating or potting that are bridging conductive elements,
35. bubble, void or delamination in conformal coating and potting between high voltage conductors,
36. lack of conformal coating specified on drawing,
37. not specified and continuous adhesive forming a bridge in contact with terminals, component body or solder joints,
38. excessive degolding,
39. insufficient degolding,
40. direct bonding on glass component body with epoxy,
41. separation of adhesive from the bonded surface,
42. separation of conformal coating from the surface,
43. any longitudinal misalignment on assembly sensitive components,
44. longitudinal misalignment of end capped and end metallized components,
45. presence of cracks in the ceramic of components or cover of component.

NOTE 1 Example to item 4: measling, delamination, halo effect.

NOTE 2 Example to item 21: tombstoning.

NOTE 3 Examples to item 31:

- End cap metallization peeling cracks in component, missing metallization are examples of damage.
- Cracks in ceramics mainly occur in chip capacitors, and leadless component with thermal plane termination.

NOTE 4 Example to item 35: High voltage applications are described in ECSS-E-HB-20-05.

12.4 X-ray rejection criteria

a. The following non-conformances while performance of X-ray inspection, utilizing equipment defined in clause 5.6.20, shall be cause for rejection:

1. bridges and other unintended metallic materials,
2. non-wetting of the solder,
3. cumulative voids greater than 25 % by area of the solder joint,
4. a single void which traverses either length or width of the terminal and exceed 10 % of the total area.

NOTE For requirement 12.4a.1 solder balls are a typical example of unintended metallic material.

b. For area array components the criteria and dimensions outside the limits given in Table 10-13 shall be met in addition to the requirements of 12.4a.

c. Any deviation to requirement 12.4a.3 shall be demonstrated by verification in compliance with requirements from clause 13.

12.5 Warp and twist of populated boards

a. The PCB assembly shall be supported during handling and transportation in order to avoid any mechanical stress on the assembly or component damage.

NOTE Mechanical support can be provided by spacer and frame.

b. The PCB shall not be forced during any operation to compensate warp and twist.

NOTE Shims or spacers can be used to accommodate warp and twist during integration.

12.6 Inspection records

a. The result of the final inspection shall be recorded on the shop traveller.

13
Verification procedure

13.1 Verification approval procedure

13.1.1 Request for verification

a. The supplier shall provide the following items to the Approval Authority:
   1. A letter from the supplier signed by the contact person and the quality assurance organization of the supplier describing his experience in assembly and making the request for verification.
   2. A verification programme in compliance with clause 13.1.4.
   3. 1 (one) technology-sample in compliance with clause 13.1.2.

13.1.2 Technology sample

13.1.2.1 Description of technology sample

a. Technology sample shall be made when introducing a new assembly process or new supplier.

b. The supplier shall provide 1 (one) technology sample of flight representative board showing the Flight assembly process capability with components of typical complexity and illustrated in space quality workmanship standards.

NOTE Examples of solder joints quality according to space industry are presented in Annex F and Annex E.

c. Technology sample shall include areas with and without conformal coating if used.

d. The supplier shall provide a listing of the assembly procedures.

e. Approval Authority may waive the needs of technology sample.

13.1.2.2 Evaluation of technology sample

a. The technology sample shall be assessed by Approval Authority or by a test house recognized by Approval Authority.

b. The assessment of the technology sample shall include visual inspection and microsection reports.

c. Approval Authority shall inform the supplier on the result of inspection of the technology sample specified in the clause 13.1.2.

d. After examination, the technology sample examination report shall be sent to the supplier.

e. Approval Authority shall inform the supplier on acceptance regarding the start of the next stages of the approval process.

13.1.3 Audit of assembly processing

a. Provided the technology sample specified in 13.1.2 is acceptable, Approval Authority shall audit the assembly facility at a time when the assembly line is in operation.

b. The findings of the audit shall remain confidential between Approval Authority and the supplier.

c. The audit of the supplier's assembly line shall be performed prior to the start of a verification programme.

d. The Approval Authority shall submit to the supplier a copy of the audit report.

NOTE The assembly line audit report is a customer document provided to the supplier and is used as input for the customer to decide if the verification programme can be further implemented.

e. The audit shall also include a further on-site review of the documentation listed in Annex A.2.1.

f. Assembly line audit shall be conducted every four years by Approval Authority.

13.1.4 Verification programme documentation

a. A verification programme shall be submitted to the Approval Authority for acceptance prior to the start of assembly verification in accordance with DRD from Annex A.

NOTE Requirement A.2.1b gives possibility to tailor verification programme.

b. Verification programme shall be in compliance with the depicted flow from Figure 13-1.

c. Depending on the assembly process to be verified, verification programme shall also be in compliance with specific requirements from clauses 13.3, 13.4 or 13.5.

d. The supplier shall organise a Verification Review with the Approval Authority during which verification programme is reviewed and approved.

NOTE The PCB design is reviewed for compliance with requirements from clause 13.1.5.

e. Prior to start of verification assembly the supplier shall organise a Manufacturing Readiness Review with the Approval Authority.

NOTE During the review, the Approval Authority can check that the verification programme is approved by all parties and that all open actions are closed.

f. The schedule of the verification activities shall be provided and maintained.

g. Any nonconformance or major change with reference to the verification plan shall be notified to the Approval Authority within one week.

h. NRBs shall be organised by the supplier.

13.1.5 Verification samples and testing

a. The PCB material, PCB build-up and footprint used for the verification shall be representative of the FM hardware.

b. Assembled components shall be flight representative with regards to construction, materials and lead finish.

c. For some assembly sensitive components, as defined in the ESCIES list, EQM quality level components should be used as a minimum.

NOTE The ESA list of assembly sensitive components is published on ESCIES for information, see www.escies.org, Technologies - ESA SMT Verification. ESA-TECQTM-MO-1143 Last release.

d. The components used for the verification shall be listed in the Verification programme documentation, in accordance with the DRD in Annex A~~Figure D-1~~.

NOTE It is the responsibility of the company that the soldering method and temperature are compliant with the manufacturer datasheet or technical notes.

e. Only component types used during the verification programme shall be regarded as approved.

NOTE 1 Approved components are listed in the assembly summary table.

NOTE 2 Component approved by similarity, as per clause 13.7, are not listed in the Assembly Summary Table

f. The verification samples shall be assembled and tested according to agreed verification programme.

g. All tests conditions shall be compliant with requirements from clause 14.

13.1.6 Final verification review

a. The verification report shall be in compliance with DRD from Annex B.

b. The verification report shall be made available to the Approval Authority.

c. The supplier shall organise with the Approval Authority a final verification review.

NOTE The Assembly processes can be reviewed during the meeting in order to have the PID issued. Verification of closure of the actions identified during the audit of the manufacturing line.

13.1.7 Approval of assembly line

a. Following the completion of the final verification review, the following documents shall be submitted to the Approval Authority:

   1. PID
   2. Assembly summary tables.

b. The assembly summary tables shall be prepared by the supplier according to DRD from Annex D.

c. In case of changes in assembly line impacting its approval, an audit shall be conducted to re-establish the approval as specified in clause 13.1.3.

d. A letter confirming the completion of a successful verification programme shall be sent to the contact person of the supplier from the Approval Authority, with the Assembly summary table in conformance with the DRD of Annex D.

   NOTE 1 The letter and the Assembly summary table provide evidence of the verification approval to a third party.

   NOTE 2 The approval of verification applies to all space projects from the date of the approval until withdrawal.

e. Reference to the Assembly summary table number shall be made on each Space project declared processes list.

   NOTE See ECSS-Q-ST-70 Table C-2.

13.1.8 Withdrawal of approval status

a. The approval status of the supplier shall be withdrawn if any of the following occurs:

   1. Repetitive supply problems and manufacturing defects.
   2. Undeclared changes to the PID.
   3. Numerous noncompliances to the PID.

      NOTE 1 Renewed approval can be granted following a review of the discrepancies.

      NOTE 2 A repeat, or partial repeat of the verification programme can be requested by the Approval Authority.

13.2 Verification programme

13.2.1 General

a. The approval of mounting and supporting of components, terminals and conductors, as specified in this standard, shall be applicable only to assemblies designed to continuously operate over the mission within the temperature limits of -55 °C to +85 °C at solder joint level.

b. The supplier shall demonstrate verification for each combination of substrate material type, PCB footprint, component type, soldering technique applied, staking and bonding, lead forming configuration, solder mask and conformal coating as used on FM.

NOTE 1 Substrate material types are defined in Table 6-1 of ECSS-Q-ST-70-12.

NOTE 2 The updated ESA list of material types is published on ESCIES for information, see www.escies.org, Technologies - ESA SMT Verification. ESA-TECMSP-MO-011418 Last release.

NOTE 3 Machine reflow, hand soldering are examples of different assembly methods.

c. The verification shall be performed on at least 3 (three) components except for the assembly sensitive components where 5 (five) parts are used per configuration in the verification programme.

NOTE For the components listed in the ESCIES sensitive list that have not been demonstrated to be non-sensitive by the supplier, the first verification test plan is with 5 (five) components.

d. Verification of the assembly shall be performed with a nominal process and a repair process for each component.

NOTE Manual process can cover a range of processes in addition to hand soldering e.g. hot gas station, IR station.

e. No rework shall be performed before MIP1 except for manually soldered components.

f. Rework of components, other than manually soldered, shall be decided during the MIP1 in compliance with requirement 13.2.1x.

g. The supplier's repair process including removing and replacing of 1 (one) of each type of mounted component shall be submitted to verification testing.

NOTE 1 Verification of the number of repairs as permitted in ECSS-Q-ST-70-28.

NOTE 2 The supplier has the option to perform more than 1 (one) repair for each type of component.

h. A repair, not included in ECSS-Q-ST-70-28, shall be submitted to a verification programme.

i. For each type of component, per configuration, the repair shall be performed on the largest component.

j. The repair shall be performed only on the components being assembled by manual soldering method.

NOTE 1 No repair verification is needed on the components being assembled by machine method as this is covered under the manual soldering verification method providing same bonding configuration.

NOTE 2 For AAD, the repair verification is a part of the verification flow.

k. Verification testing of commercial components shall be performed for each lot in conformance with this clause.

l. Terminations to be microsectioned shall be connected to the internal PCB layers

NOTE The terminations to be microsectioned are described in Table 14-5.

m. The verification of area array components shall meet the requirements of clause 13.5.

n. The supplier shall maintain a list of assembly sensitive components.

o. Assembly sensitive components shall be submitted to re-verification every four years to monitor the stability of the assembly.

p. The re-verification of assembly sensitive components specified in the requirement 13.2.1o may be performed on limited verification programme with worst case configuration identified during initial verification.

NOTE 1 1 (one) substrate, one package per component type, 3 (three) samples per component.

NOTE 2 For leadless components, mechanical testing can be omitted.

NOTE 3 Non-destructive characterization can be proposed as alternative to microsection.

q. The verification sample shall be submitted to 2 (two) nominal soldering method reflows when reflow is performed on the both PCB sides of the FM.

NOTE The supplier has the option to flip the board for the second reflow.

r. The SMD type classification shall be in accordance with Table 13-1.

Table 13-1: Component type classification

Component type	Classification
Rectangular and square end-capped or end-metallized component with rectangular body	Leadless chip
Cylindrical and square end-capped components with cylindrical body	Leadless chip
Bottom terminated chip component	Leadless
Component with Inward formed L-shaped leads	Leaded
Leadless component with plane termination	Leadless
Leaded component with plane termination	Leaded
Castellated chip carrier component	Leadless
No lead Quad Flat Pack	Leadless
Flat pack and Gull-wing leaded component with round, rectangular, ribbon leads	Leaded
“J” leaded component	Leaded
Components with ribbon terminals without stress relief (flat lug leads)	Leaded
Staked modules components with leads protruding vertically from bottom	Leaded
Area array components	AAD

s. The verification programme as shown in Figure 13-1 shall consist of:

1. Visual inspection in conformance with clause 12,
2. Cleanliness in conformance with requirement 11.1.3.3a,
3. Initial electrical continuity in conformance with requirement 14.2.5a,
4. Shock testing in conformance with clause 14.4,
5. Vibration in conformance with clause 14.3,
6. Thermal cycling performed in compliance with requirement 14.6i except for area array components,
7. For area array components, temperature cycling in conformance with requirements from requirement 14.6j,
8. Microsectioning in conformance with clause 14.8.

t. When mechanical bonding is underneath the component, microsectioning of one component may be performed after vibration and 50 thermal cycles to justify the integrity of the bonding.

NOTE The component can be 1 (one) of the 3 (three) assembled components.

u. The environmental conditions of the mission including ground testing shall be reviewed to envelop the mission conditions in the verification programme.

v. The conditions associated with long term storage, extensive ground testing, mechanical stress after launch, high temperature application with or without thermal cycles shall be assessed by the supplier.

w. The supplier shall organise a Verification review (VR) with the Approval Authority during which verification programme is reviewed and approved.

NOTE 1 The PCB design is reviewed to check compliance with requirements from clause 13.1.5.

NOTE 2 During the review, the Approval Authority can check that the verification programme is approved by all parties and that all open actions are closed.

x. Prior to start of verification assembly the supplier shall organize a Manufacturing readiness review (MRR) with the Approval Authority.

y. The supplier shall organise a Mandatory inspection point (MIP1) with the Approval Authority prior to any conformal coating with five days notification.

NOTE The Approval Authority can delegate the MIP1 to the supplier.

z. Prior to any environmental testing the supplier shall organise with the Approval Authority an action review during which the MIP and outstanding actions are reviewed, with five days notification.

NOTE The Approval Authority can delegate the action review to the supplier.

aa. The supplier shall organise with Approval Authority a Mandatory Inspection Point (MIP2) at the completion of the environmental test with five days notification.

NOTE The Approval Authority can delegate the MIP2 to the supplier.

bb. The supplier shall organize with the Approval Authority a Test review board (TRB) during which the environmental tests results are reviewed.

NOTE The Approval Authority can delegate the TRB to the supplier.

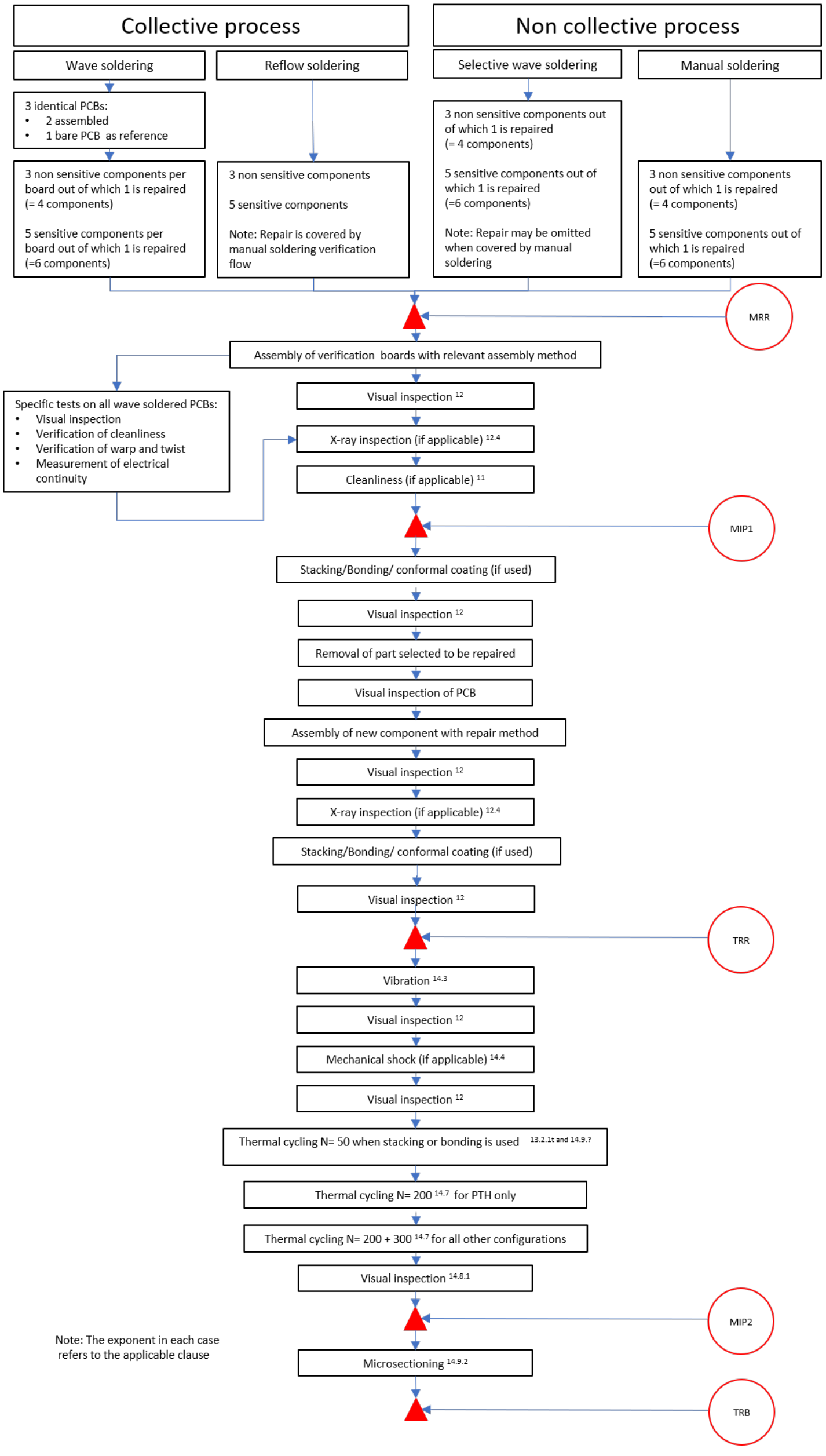


Figure 13-1 : Generic soldering verification flow

13.2.2 Verification for PTH manual soldering

a. Any soldering configuration not covered by requirements from clauses 8.2, 9 and 10.3 shall be verified in accordance with clause 13.2.1.

b. A process specific verification programme shall be performed for through hole component assemblies with stress relief that are not compliant to clause 8.2.

13.2.3 Additional verification for wave soldering

a. For non-assembly sensitive components, the supplier shall provide 2 (two) assembled PCBs with at least 3 (three) components of each type per board and 1 (one) non-assembled PCB as reference.

b. For assembly sensitive components, the supplier shall provide 2 (two) assembled PCBs with at least five components of each type per board and 1 (one) non-assembled PCB as reference.

c. Each board shall have an identical layout and be from the same batch.

d. The layout and component density shall be similar to that envisaged for spacecraft circuits.

e. Soldering log compliant with clause 14.9 shall be made available to the Approval Authority.

f. The soldering log shall include evidence that all the following conditions are met:

   1. maximum 5 % of reworked soldered connections,

   2. all the visual inspection of clause 12 and cleanliness requirements of clause 11.1 are met.

13.3 Special verification testing for ceramic area array components

13.3.1 General

a. The assembly verification of ceramic AADs shall be divided in the following 2 (two) parts, as shown in Figure 13-2.

   1. electrical monitoring, and

   2. demonstration of capability.

      NOTE 1 The purpose of the capability samples is to show that the PCB and the component are intact after the assembly and repair of AAD and environmental testing (vibration, mechanical shock and 500 temperature cycles). A crack in the columns or balls is not considered as reason for rejection.

      NOTE 2 Once the capability samples show a satisfactory result the verification of AAD can commence.

NOTE 3 Capability samples can be excluded from the programme if the supplier can demonstrate through previous verification heritage.

b. When nominal and repair processes are identical then total number of parts during verification may be reduced to 5 (five) with 3 (three) assembled and 2 (two) repairs among the 3 (three) assembled.

c. The verification shall be performed with daisy chain components to demonstrate a reliable electrical function of the PCB and the package interface throughout the environmental test campaign.

NOTE Environmental test campaign to include vibration, mechanical shock and 1500 temperature cycles.

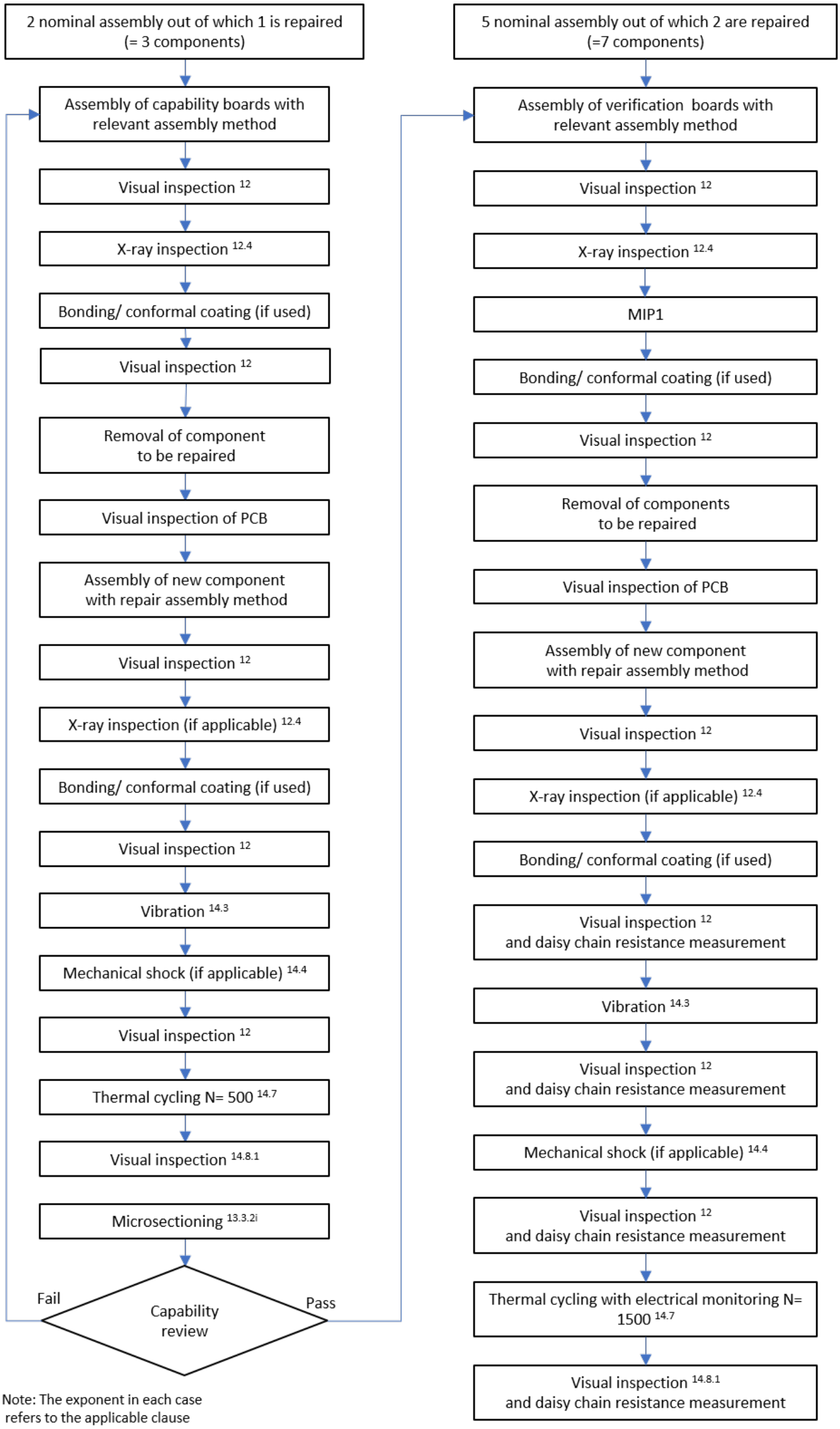


Figure 13-2: Area Array component verification programme flow chart

13.3.2 Evaluation of capability samples

a. The supplier shall manufacture and demonstrate that the 2 (two) capability samples are in conformance with the requirement 13.3.2i before the manufacture of the verification samples using daisy chain components can be initiated.

b. The PCB material, PCB build-up, foot print and components used as capability samples shall be representative for the FM of the hardware.

c. 2 (two) components shall be assembled with the nominal reflow process.

NOTE The supplier can use daisy chain packages for the capability assessment with or without electrical monitoring.

d. One of the components from requirement 13.3.2c shall be removed and replaced with a new component using the repair process.

e. The components shall be inspected in conformance with requirements from the clause 10.5.11.

f. The components shall be submitted to vibration testing in conformance with requirements from the clause 14.3.

g. The components shall be submitted to 3 (three) shock axes in conformance with requirements 14.4b and 14.4e.

h. The components shall be submitted to 500 thermal cycles in conformance with requirements from the clause 14.5.

i. After environmental tests completion, microsectioning of the component shall be performed to demonstrate PCB integrity in the AAD area with respect to:

1. Clause 10 of ECSS-Q-ST-70-60,
2. Damage to the component outside the procurement specification,
3. Footprint lifts,
4. Cracks in laminate,
5. Cracks in via,
6. Cracks in track,
7. Delamination in the PCB,
8. Measling in the PCB,
9. Cracks in bonding if used.

13.3.3 Verification

a. The PCB material, PCB build-up, foot print and daisy chain components used for the verification shall be representative of the FM of the hardware.

b. For each assembly method and mounting configuration 5 (five) components shall be assembled with the nominal process.

c. 2 (two) of the assembled components shall be removed and replaced with new components using the repair process.

d. The components shall be inspected in conformance with requirements from the clause 10.5.11.

e. The 5 (five) components shall be submitted to vibration testing in conformance with requirements from the clause 14.3.

f. The 5 (five) components shall be submitted to 3 (three) mechanical shock pulses in each direction in conformance with requirements 14.4b.

g. The 5 (five) components shall be submitted to 1500 thermal cycles with temperature conditions in conformance with requirement 14.6j.

h. Resistance measurement should be done, at ambient, before and after any mechanical testing in accordance with clause 14.2.5.

13.4 Component verification with electrical testing procedure

a. Except the cases specified in requirement 13.4c the supplier may propose electrical monitoring as an alternative method, for each assembly configuration, including the repair assembly process, to achieve verification providing all the following conditions are met:

1. one component for initial construction analysis except the case for sensitive and leadless components,
2. for assembly sensitive components, a minimum of five components to be assembled,
3. minimum number of 32 components for electrical monitoring,
4. all solder terminations to be continuously electrically monitored throughout the temperature cycling,
5. minimum of 1500 thermal cycles in accordance with requirement 14.6j,
6. the number of successfully completed cycles for each failed component is recorded.

b. Electrical monitoring shall be performed for ceramic area array components in conformance with requirements in requirement 13.3.

c. Leadless chip capacitor and leadless components with plane termination shall be excluded from electrical monitoring.

NOTE Capacitor and TO276 packages such as SMD05, SMD1, SMD2 and SMD5C, are excluded as the failure mechanism is crack in ceramic.

d. First failure in case number of cycles <1500 shall be identified as the component assembly verification limitation.

e. Any failed component shall be subjected to failure analysis.

f. The electrical value of components shall be selected to detect anomalies in the solder joint:

1. for resistor zero ohm or the lowest value in the procurement specification,
2. for other types, custom daisy chain.

g. The maximum increase of each individual daisy chain or device resistance, across the entire temperature cycling range during 1500 thermal cycles, shall not be more than 10 % of initial resistance recorded during the first 5 (five) cycles.

NOTE Depending on application the acceptable drift of resistance can be adapted.

h. For each assembly method and type of components at least 32 components shall be assembled for electrical monitoring.

NOTE 1 Machine reflow, hand soldering are the examples of assembly method.

NOTE 2 The assembly of the capability and the electrical verification samples can be made on the same board.

i. If capability and electrical monitoring samples are on the same board they shall be separated before the microsectioning of the capability samples and before the environmental tests for the electrical verification samples.

NOTE Illustration is given in the flow diagram of Figure 13-3.

j. Capability samples may be excluded from the programme if it can be demonstrated through previous verification heritage.

k. Microsectioning shall be performed in accordance with requirements from clause 14.8.

l. Vibration and shock testing shall be performed in conformance with requirements from clauses 14.3 and 14.4.

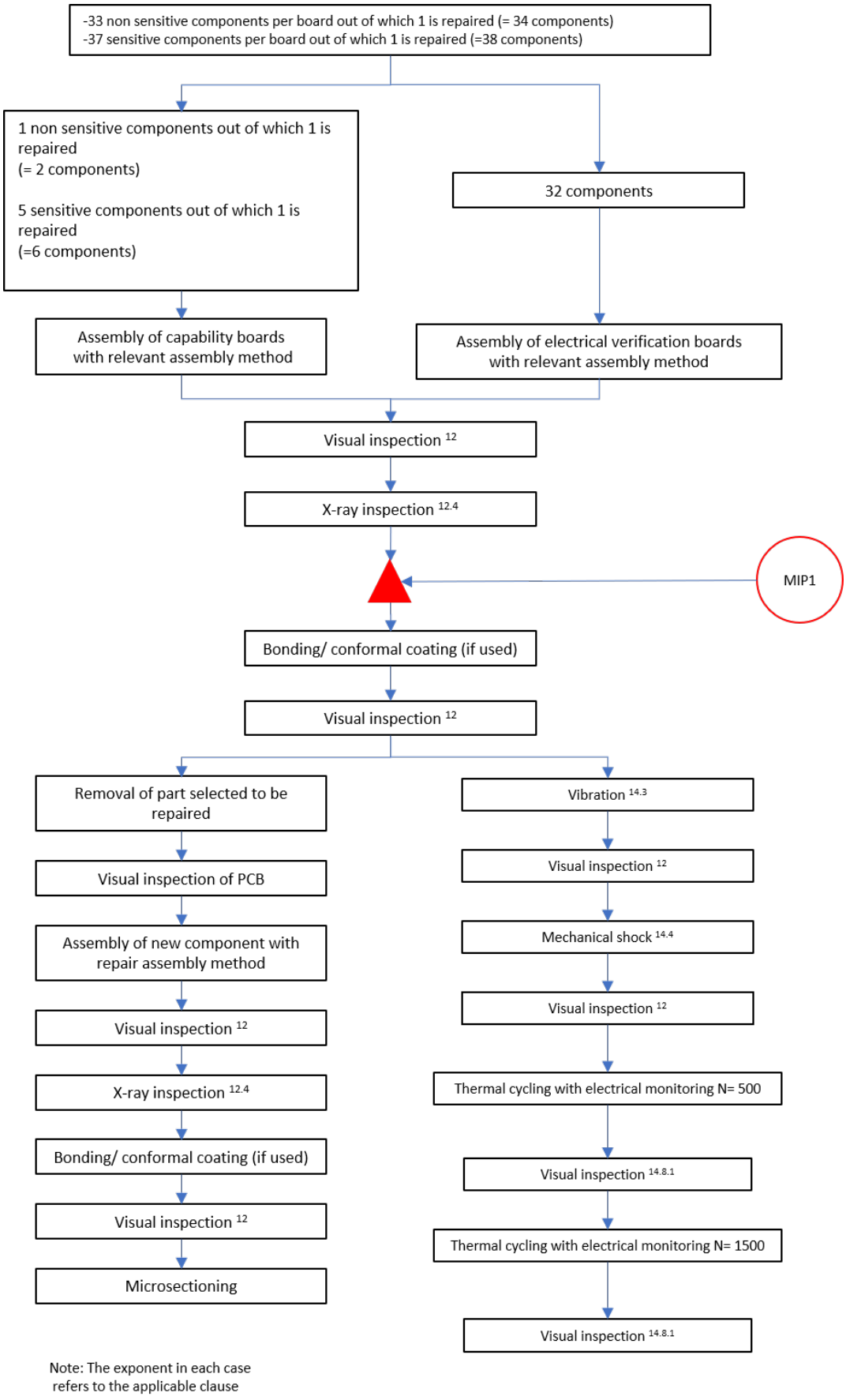


Figure 13-3: Component verification with electrical testing procedure

13.5 Verification for solderless process

a. The verification tests shall be performed on representative assembly configuration and under electrical monitoring when identified in Figure 13-4.

b. The verification tests shall be performed in order to show absence of degradation within the solderless interconnection part, PCB and component during all ground and in-orbit mission.

NOTE Possible degradations can be creeping of the spring, fretting degradation of the contact.

c. 6 (six) parts shall be assembled with the same mechanical configuration as flight model.

d. Mate-demate number shall permit to cover the application requirement with a margin of 4 in compliance with Table 4-4 of ECSS-E-ST-33-01.

e. Minimum vibration levels shall be in compliance with requirement 14.3h.

f. Shock test shall cover project requirement.

g. Electrical monitoring shall be applied during mechanical tests, vibration and shock when equipment is functional during launching phases.

h. Number of thermal cycles shall be 500, under electrical monitoring providing it is sufficient to cover the mission with margin of 2 (two).

NOTE Mission includes ground and flight environment.

i. Damp heat test shall be performed for all applications in compliance with Table 5-2 of ECSS-Q-ST-70-14.

j. In case of long-term storage application, project specific requirements may apply instead of requirement 13.5i.

k. Electrical continuity test according to clause 14.2.5 shall be performed to verify absence of degradation of the connection after damp heat test.

l. Life test shall be performed according to requirement 2000 hours at 125 °C or at maximal storage temperature to evaluate the spring reliability under electrical monitoring.

m. The supplier may waive requirement 13.5l providing representative test has been performed by the manufacturer.

n. Visual inspection criteria in compliance with clause 12 shall apply to connector, component and PCB.

o. Microsections of connector, component and PCB shall be done according to clause 14.8 in order to verify absence of plating damage at connector level and PCB damage.

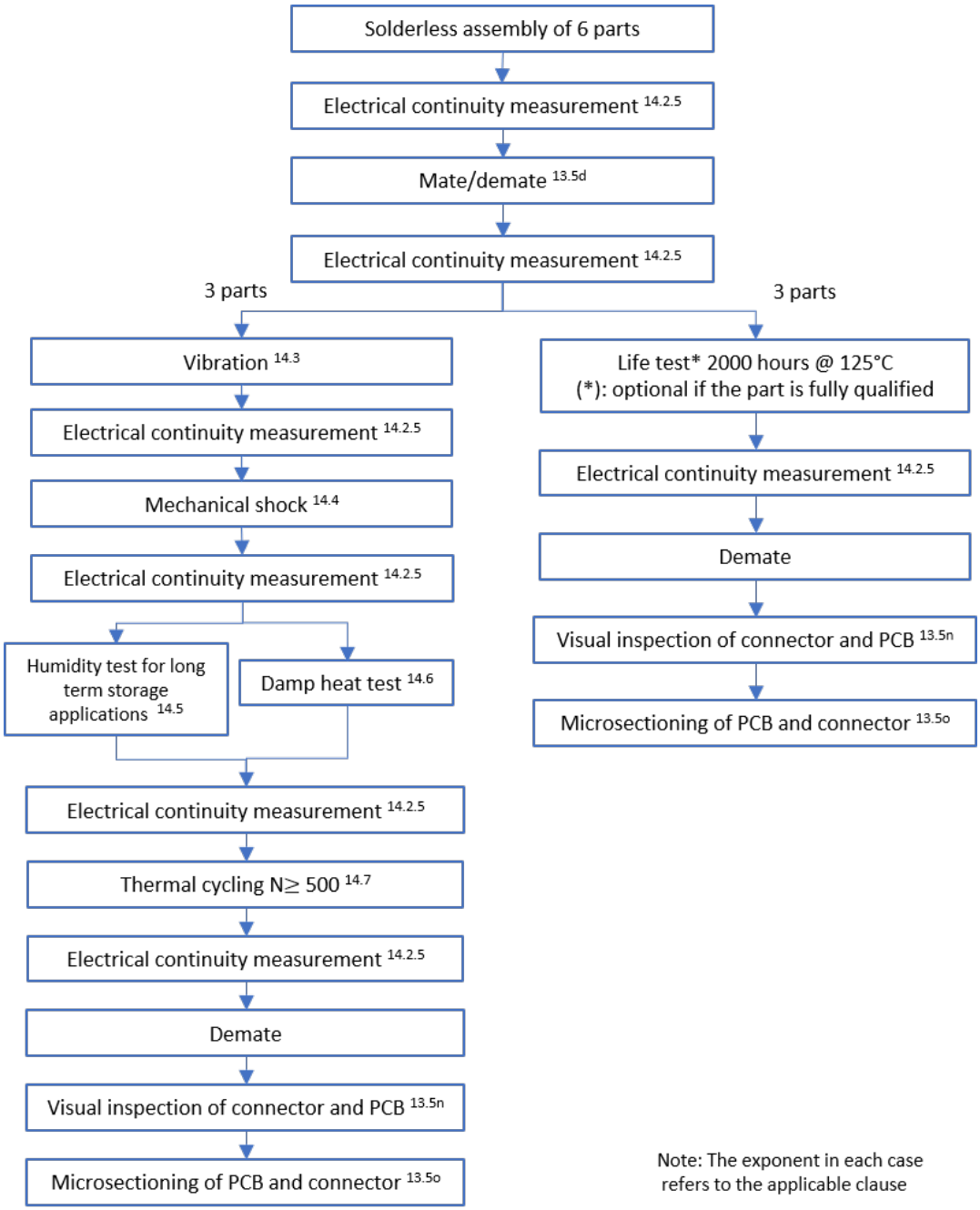


Figure 13-4: Verification procedure for solderless technology

13.6 Conditions for delta verification

a. The supplier shall undertake a verification for any new configuration not covered by similarity rules in accordance with requirements from clause 13.7.

b. The delta verification shall be performed when changes are undertaken as specified in Table 13-2.

c. For a process change verification programme based on assembly of already verified PCB materials, the choice of the PCB type or a sampling of several PCB types instead of all PCB materials may be selected, subject to agreement by Approval Authority.

NOTE 1 The selection criteria are based on worst cases depending on the change of process to be verified.

NOTE 2 Examples of worst cases are CTE mismatch, thermal dissipation, stiffness.

d. For delta-verification associated with process change the verification boards shall be specified, in order to be representative of the process evolution.

e. The types and number of parts to be mounted on the test vehicles shall be specified as agreed by Approval Authority.

NOTE This allow to track any impact of the process evolution as defined in Table 13-2.

f. A delta-verification programme in accordance with the DRD from Annex A shall be submitted for approval to the Approval Authority.

g. Number of sensitive parts to be assembled and microsectioned shall be 5 (five).

h. Number of sensitive parts to be assembled and microsectioned may be reduced to 3 (three) if the initial verification showed reproducible results.

NOTE Sensitive parts are from the ESCIES list and company PID.

i. Small size packages may be omitted from microsectioning providing that these package sizes are already in the company PID.

Table 13-2: Conditions invoking verification

Changes	Verification boards without any test	Cleanliness tests (Ref 14.2.3)	Material compatibility with cleaning solvent	Verification boards with tests according to Figure 13-1, Figure 13-2 or Figure 13-3
New component mounting configuration (example, already verified with conformal coating and now mounted without)				X
New SMD package size, not covered by similarity rules				X
New manufacturer of ceramic leadless chip component	X +microsections[1]			
New material of printed circuit board **Epoxy, Polyimide, Aramid, mixed material build-up are different materials, PCB surface finish**				X
New thermal and/or mechanical adhesive				X
New conformal coating				X
New solder paste with same alloy, same powder size distribution, same flux activation type	X +microsections[1]	X		
New solder paste with new alloy, flux activation type and/or different physical-chemical characteristics				X
New flux activation type for hand solder	X +microsections[1]	X		

Changes	Verification boards without any test	Cleanliness tests (Ref 14.2.3)	Material compatibility with cleaning solvent	Verification boards with tests according to Figure 13-1, Figure 13-2 or Figure 13-3
New cleaning solvent and or new cleaning process		X	X	
New reflow profile, Peak temp +/-5°C, duration above liquidus [2]				X
New equipment to deposit soldering paste without change of process	X +microsections[1]			
New solder paste depositing process				X
New component placing equipment	X +microsections[1]			
New component placing equipment of same process method	Visual inspection only			
New type of reflow equipment with process change				X
New reflow equipment without process change	X +microsections[1]			
Move Manufacture location outside the clean room approved in the PID	X +microsections[1]			

[1] For microsection, one part per family type from the SMT summary table as per Annex D.

[2] The reflow profile is identical when the duration of the pre-heating, ramp of flux activation phase, peak temperature and time above solder liquidus, ramp of cooling phase can be repeated between different types of PCBs.

13.7 Verification by similarity

13.7.1 Conditions for similarity for PTH components

a. Verification by similarity for manually soldered PTH components, described in clause 13.2 shall apply when following conditions are met:

1. Components are smaller than the verified Lmax, Wmax and Hmax,
2. Construction of the component is identical to that verified,
3. Assembly configuration is the same,
4. Materials are identical,
5. Lead material is the same,
6. Lead section is the same, and
7. Pitch is smaller than the one verified.

b. Verification by similarity for wave or selective wave soldered PTH components shall apply when following conditions are met:

1. Smaller than the verified Lmax, Wmax and Hmax,
2. Construction of the component is identical to that verified,

3. Same assembly configuration,
4. Materials are identical,
5. Lead material is the same,
6. Lead section is the same, and
7. Pitch is smaller than the one verified providing evidence that the PCB is not damaged.

NOTE Absence of PCB damage can be demonstrated by successful verification on a different component with same small pitch

c. Verification by similarity for a PTH shall be declared successful when the PCB is similar to that used for the verification.

13.7.2 Conditions for similarity for SMD

a. Verification by similarity shall not apply to commercial components.

b. Verification by similarity shall not apply to castellated components.

NOTE Some resistors networks and LCCs are castellated components examples.

c. Verification by similarity for leaded package according to clauses 10.5.9, 10.5.10,10.5.12 shall not be declared successful unless all the following conditions are met:

1. the package is smaller than the verified Lmax, Wmax,
2. the package is thinner than the maximum height verified,
3. the package weight is lower than the maximum verified,
4. the lead pitch, nominal thickness, nominal width and materials composition are identical,
5. the coated lead finishes on the termination are identical,
6. the bending dimensions and shape are identical,
7. the packages are constructed from the same materials.

NOTE 1 to item 3: Radiation shielded packages can be heavier than standard flatpack and are not covered by similarity.

NOTE 2 to item 7: Glass to metal sealed, glass sealed side-brazed, top-brazed, and bottom-brazed packages are different families.

NOTE 3 to item 7: Dual side pin arrangements are different to quad side pin families.

d. For flat pack, verification by similarity may apply even if the lead materials are different.

e. Verification by similarity for end-capped and end-metallized components with rectangular body in accordance with clause 10.5.2, shall not be declared successful unless all the following conditions are met:

1. the component length is between Lmin and Lmax of that verified,
2. the component width is between Wmin and Wmax of that verified,

3. the component height is less than Hmax of that verified,
4. the ceramic material type is identical,
5. the metallization of the termination and the barrier layers on components are identical,
6. the component manufacturer is identical.

NOTE 1 to item 1 and 2: For example, 0402 – 2220 does not qualify 1825 as the width is outside the max 20 verified.

NOTE 2 to item 4: ceramic chip capacitors can be very sensitive to mounting conditions. Generally, type I chip capacitors show less sensitivity to mounting constraints than Barium Titanate based type II chip capacitors. This sensitivity is design and process related and can therefore vary from one manufacturer to another. Within a manufacture type II range, one or more ceramic material can be used but one can say that generally the highest end of the capacitance ranges is the most sensitive to mounting conditions. In order to increase capacitance value for a given chip format with a specified maximum chip thickness, manufacturers increase the number of dielectric layers, thus increasing the volume ratio between electrode material and ceramic, which is not favourable in terms of sensitivity to mounting constraints.

NOTE 3 to item 4: It is therefore impossible to apply similarity rules between type I and type II ceramic chip capacitors as well as between different manufacturers. It is also good practice to select in priority the highest capacitance values in a class or type I or type II ceramic capacitors range to be submitted to assembly verification.

NOTE 4 to item 4: Examples of ceramic types are NPO, Z5U and Y7R.

NOTE 5 to item 5: Flexible and non-flexible terminations are not identical.

f. Ceramic chip capacitors with end-capped and end-metallized components with rectangular body in accordance with clause 10.5.2 and strictly smaller than 1825, from alternative component manufacturers, may be verified by similarity provided the following:

1. The supplier has successfully performed a full verification programme according to clause 13.2 for at least one component manufacturer, covering the dimensions, termination plating and the type of ceramic of the alternative manufacturer, in accordance with requirement 13.7.2e.1, 2, 3, 4 and 5.
2. The supplier ~~shall verify~~has verified that the component is not damaged after manual soldering.
   (a) For non-assembly sensitive components, 3 (three) parts each of the smallest and largest sizes ~~shall be~~were manually soldered.
   (b) For assembly sensitive components, 5 (five) parts of the smallest and largest size ~~shall be~~were manually soldered.

(c) Microsectioning ~~shall be~~was performed on all samples in conformance with clause 14.8.2.

NOTE 1 For item 1, termination plating, Sn60 and Sn63 are equivalent and different from Sn85 to Sn95.

NOTE 2 For item 2, manual soldering covers collective soldering.

g. For leadless chip resistors according to clause 10.5.2, thick film resistors may be verified by similarity to thin film resistors providing the following:

1. The supplier has successfully performed a full verification programme according to clause 13.2for at least one thin film resistor technology, covering the dimensions, termination plating and the type of material, in accordance with requirements 13.7.2e.1, 2, 3 and 4.

NOTE For termination plating, Sn60 and Sn63 are equivalent and different from Sn85 to Sn95.

h. Verification by similarity for leadless chip inductors (10.5.4, MELF resistors (10.5.3, L-Shape inwards components 10.5.5), thermistors (TO BE ADDED), diodes and fuses (TO BE ADDED) shall not be declared successful unless all the following conditions are met:

1. the component length is less than Lmax of that verified,
2. the component width is less than Wmax of that verified,
3. the component height is less than Hmax of that verified,
4. the material type is identical,
5. the metallization of the termination and the barrier layers on components are identical,

i. Verification by similarity for leadless component with plane termination according to clause 10.5.6 shall be valid in case the following conditions are met:

1. smaller than the verified L_{max} and W_{max},
2. the construction of the component package is identical to that verified,
3. the materials are identical.

NOTE To item 1: The outline dimensions of the component are length L and width W.

NOTE To item 2: SMD0.2 exists in 2 versions which are not identical.

j. Verification by similarity for area array components shall be valid in case all the following conditions are met:

1. lower number of columns,
2. the same pitch,
3. same column dimensions,
4. same column distribution,
5. same column materials,
6. same column construction,
7. same column manufacturer,
8. same column assembly process,
9. lower mass,

10. same material and same package construction,
11. same body shape.

14
Environmental tests conditions

14.1 Overview

Whenever a test is referred in this document, test conditions are described in the following clauses.

14.2 Initial tests

14.2.1 Visual inspection

a. Visual inspection shall be performed on each of the verification boards according to clauses 12.2 and 12.3.

14.2.2 X-ray inspection

a. X-ray inspection shall be performed on each of the verification boards according to clause 12.4.

14.2.3 Cleanliness test

a. The supplier shall perform cleanliness test on one of the verification boards according to clause 11.1.3.4.

b. The cleanliness test of the board shall be conducted in accordance with requirements from the method 2.6.3.3 of IPC-TM-650.

14.2.4 Warp and twist of PCB

a. The supplier shall measure and record warp and twist of each of the verification boards according to requirements of clause 9.9.3 of ECSS-Q-ST-70-60.

14.2.5 Electrical continuity measurement

a. Electrical continuity shall be measured with a daisy chained component including 100 % of the component connections.

NOTE Electrical continuity measurements are mainly used for AAD and solderless assemblies.

b. Electrical monitoring of the daisy chain shall be performed during the 1500 thermal cycling.

NOTE 1500 thermal cycling is mainly dedicated to CCGA components.

c. The electrical monitoring shall be continuous throughout all 1500 cycles.

d. The sampling time of the electrical measurement shall be maximum 10 s throughout the 1500 cycles.

NOTE Different electrical monitoring methods can be agreed with the Approval Authority.

e. The maximum increase of each individual daisy chain resistance, across the entire temperature cycling range during 1500 thermal cycles, shall not be more than 10 % of initial resistance recorded during the first 5 (five) cycles.

f. No interrupts in the electrical monitoring shall be detected throughout the thermal cycling.

g. The supplier may provide their own criteria for an electrical failure to Approval Authority for approval.

14.2.6 Electrical continuity of multilayers PCB

a. When wave soldering is tested for multilayer boards, electrical continuity shall be measured on at least 25 % of all holes.

b. The electrical continuity measurement shall include at least one internal connection per hole in conformance with the requirements of the clause 9.3.8 from ECSS-Q-ST-70-60.

c. For multilayer PCBs, electrical continuity measurements shall be performed throughout a further 10 thermal cycles at the end of thermal cycling test.

14.3 Vibration

a. The test specimen shall be vibration tested according to test flow chart described in Figure 14-1.

NOTE Vibration testing methodology - From the input levels required by the projects in progress, the maximum deformation of the printed circuit board at the part level is established for each configuration (part type, location on the printed circuit board).

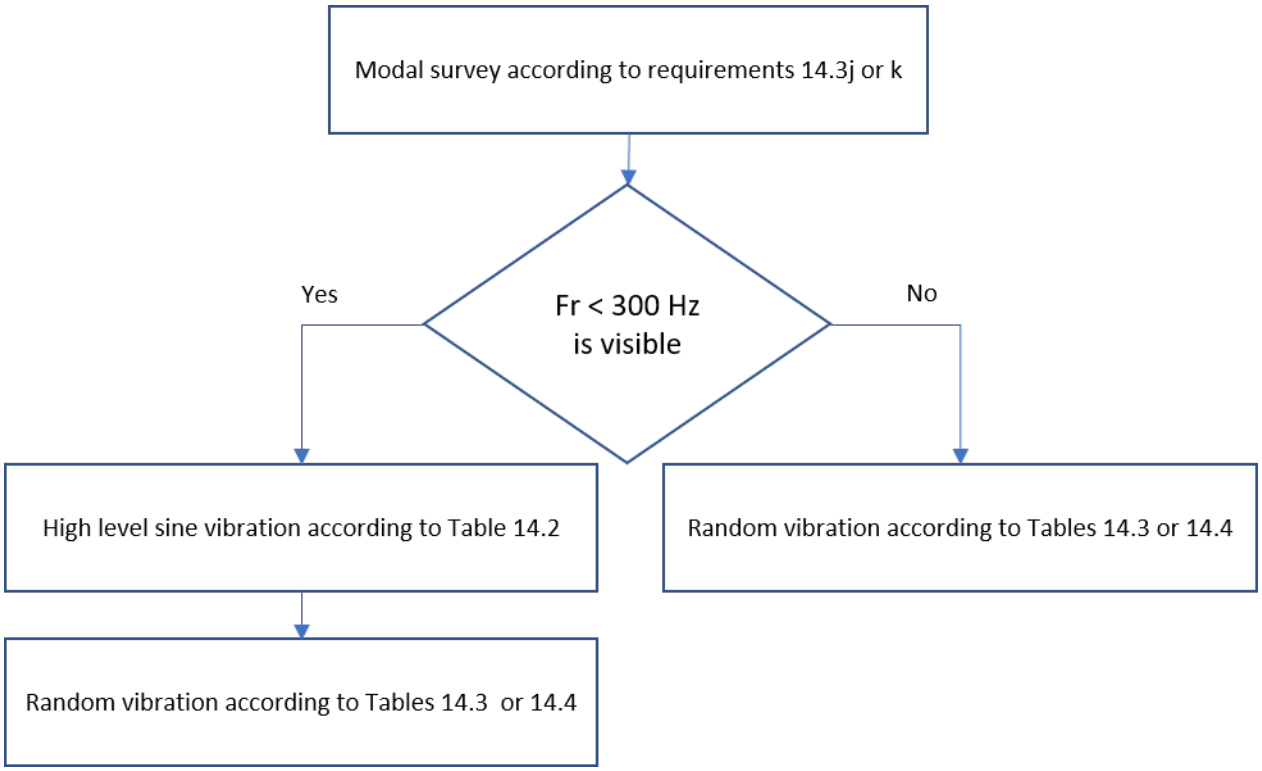


Figure 14-1:Vibration test flow chart

b. The PCB design and mechanical mounting including fittings such as stiffeners, frames or spacers shall be representative of the flight model.

c. The mechanical mounting configuration of the PCB for the vibration tests shall be identified.

d. In order to take into account test samples imperfections, notching may be used to reduce non-representative mechanical overstresses providing that requirements 14.3e and 14.3f are fulfilled.

e. Notching shall be justified to the Approval Authority.

f. Internal notching shall be identified in the vibration test report.

g. The levels and duration of the vibration shall be provided.

h. Verification levels covered by the vibration tests shall be in compliance with Table 14-1, Table 14-2, Table 14-3, and Table 14-4 and project requirements.

i. A modal survey shall be performed in order to detect any primary resonant frequency f_r.

NOTE 1 Modal survey can be done with sine or random vibration

NOTE 2 It is a good practice, for generic applications, that the verification board exhibits a primary resonant frequency in the range of 500 Hz - 800 Hz.

j. The modal survey conditions shall be compliant to level values, as defined in Table 14-1a for sine survey.

k. The modal survey conditions shall be compliant to level values, as defined in Table 14-1b for random survey.

l. Transfer function shall be issued from modal survey and presented to customer.

m. Input vibration levels shall be measured at the interface between the vibration plate and the PCB.

n. The response acceleration of the assembled PCB shall be monitored and recorded during testing.

o. The accelerometers shall be placed on the PCB as well as on the base plate in order to determine the acceleration of the PCB.

NOTE It is a good practice to mount the accelerometers on the PCB area of largest deflection.

p. Vibration testing shall be performed in the three orthogonal axes: one out-of-plane and two in-plane.

q. The severity of the vibration test shall not be less than that shown in Table 14-2, Table 14-3 and Table 14-4.

Table 14-1: Modal survey conditions

a - Sine survey		**b - Random survey**	
Amplitude	0,5 g 0 to peak	Range (Hz)	Level
Frequency range	10 Hz to 2000 Hz	10 Hz- 2000 Hz	$5{,}10^{-4}$ g^2/Hz
Sweep rate	2 octaves/minute	Global levels: 1 g r.m.s.	
Direction	X, Y and Z axis	X, Y and Z axes	1 min/axis
		Frequency sampling = 2 Hz	

Table 14-2: Minimum severity for sine vibration testing

Range (Hz)	**PSD Level** (0 to peak)	**Sweep rate** (Oct/min)
Spacecraft		
25 to 100	20 g	1
100 to 200	15 g	
Duration: 1 cycle up from 25 Hz to 200 Hz		
Launchers		
10 to 16	10 mm	1/3
16 to 60	10 g	1/3
60 to 70	22,5 g	1/3
70 to 200	22,5 g	2
200 to 2000	10 g	2
Duration: 1 cycle up from 10 Hz to 2000 Hz		

Table 14-3: Minimum severity for random vibration testing for all applications except launchers

Perpendicular to PCB		Parallel to PCB	
Range (Hz)	PSD Level	Range (Hz)	PSD Level
20 to 100 100 to 500 500 to 2000	+ 6 dB/oct. 1,0 g^2/Hz - 6 dB/oct.	20 to 100 100 to 800 800 to 2000	+ 6 dB/oct. 0,5 g^2/Hz - 3 dB/oct.
Global: 28,5 g r.m.s.		Global: 27,1 g r.m.s.	
Duration: 5 minutes per axis			

Table 14-4: Minimum severity for random vibration testing for launcher

Frequency (Hz)	PSD
20 to 60 60 to 1000 1000 to 2000	+ 3dB/oct. 0,27 g^2/Hz - 6 dB/oct.
Global: 20 g r.m.s.	
Duration: 5 minutes per axis	

14.4 Mechanical shock

a. Where assembly of a component is sensitive to mechanical shock, shock testing shall be performed.

NOTE Examples of mechanical shock sensitive components can be found in Table 17-1 of ECSS-E-HB-32-25.

b. When mechanical shock testing is required as defined in 14.4a then the shock levels shall be set to meet the intended mission with margin.

NOTE It is the responsibility of the supplier to verify that the levels applied are sufficient to cover the mission.

c. The levels and duration of the shock shall be provided in the verification report.

d. For area array components, the mechanical shock levels shall be set to meet the intended mission with margin, except the case specified in the requirement 14.4e.

e. For area array components, mechanical shock may be omitted when the mechanical design can demonstrate robust margin.

NOTE The use of dedicated mechanical stiffener is an example of such design.

14.5 Damp heat test

a. Damp heat test conditions shall be (93 ± 3) % at (40 ± 3) °C for 240 hours in compliance with the annex C of ECSS-Q-ST-70-14.

14.6 Temperature cycling test

a. The test specimen shall be temperature cycled in an air circulating or inert gas purged oven.

b. Before the start of the temperature cycling, the test specimen shall be baked out to remove the internal humidity according to clause 7.7.

c. The bake-out may be part of the first temperature cycle.

d. The temperature cycle shall be between –55 (-5/+0) °C and +100 (-0/+5) °C.

e. The first temperature cycle shall be hot.

f. The rate of temperature change during the temperature cycle shall not exceed 10 °C per minute.

g. The soak time at each temperature extreme shall be a minimum of 15 minutes.

h. The monitoring thermocouple shall be attached to the surface of the printed circuit board.

i. The total number of temperature cycles shall be 500, except for area array components and components verified by electrical monitoring.

j. The total number of temperature cycles shall be 1500 for area array components and components verified by electrical monitoring.

k. Compliance from -55 °C to +85 °C for mission shall be stated.

14.7 Final tests

14.7.1 Visual inspection

a. Visual inspection of each verification sample shall be made using the list of nonconformance criteria of clause 12.3.

b. Any identified nonconformance during the visual inspection specified in 14.7.1a, before any aging test, shall lead to rejection of the verification sample.

c. Any identified nonconformance during the visual inspection specified in 14.7.1a, after any aging test, shall be recorded in the traveller sheet of the verification sample.

d. In the case of visual failures, an analysis shall be performed to identify if the failure results from the component or the assembly process.

e. The identified nonconformances of 14.7.1c should be classified in acceptable or unacceptable depending on performed test flow.

NOTE After the environmental campaign, some defects are acceptable. Example: granular and disturbed solder joints are typical after verification programme.

f. The nonconformances identified in 14.7.1b and 14.7.1c shall be notified to the Approval Authority within one week.

14.7.2 Electrical measurements

a. Electrical continuity measurements shall be performed for multilayer boards which are monitored throughout a further 10 thermal cycles.

b. Electrical continuity measurements for multilayer boards with positive changes greater than 10 % shall be recorded as failed in the verification report.

14.8 Microsection

14.8.1 Microsection facilities

a. The Approval Authority should make available the list of laboratories to perform microsection.

NOTE The list of available laboratories is on ESCIES website.

b. Microsections shall be performed by a laboratory specified in 14.8.1a except the case specified in the requirement 14.8.1c.

c. When in-house or other non-listed microsection facilities are used, the company shall demonstrate the following:

1. the laboratory capability on a representative sample including conformal coating is provided,
2. a report with associated microsections is sent to the Approval Authority for review and assessment of quality of microsectioning,
3. representative samples include chip components, LCCs and FPs.

14.8.2 Microsections location and acceptance criteria definitions

a. At least one microsection shall be made per assembly configuration after environmental testing on each type of component, size and assembly processes and soldering processes.

NOTE Successive polishing planes can be performed.

b. The microsection shall be done on the component having the worst solder joint appearance as identified at MIP2.

c. The microsections of the component shall be done as specified in Table 14-5.

d. The microsection shall be inspected with a magnification of 50 to 200 times except the case specified in the requirement 14.8.2e.

e. The microsection for components with small stand-off should be inspected with magnification up to 500 times.

NOTE Examples of small stand-off components are LCCs, chip resistors.

f. In case the microsection shows a crack more than 75 % of acceptable crack, the component type shall be classified as sensitive.

g. When requirement 14.8.2f. occurs, all remaining components from verification boards shall be microsectioned in order to confirm that acceptance criteria are still fulfilled.

NOTE For a first verification of a new component not identified as assembly sensitive, 3 components are sufficient.

h. For assembly sensitive components, 5 (five) components shall be microsectioned per assembly configuration.

i. Additional microsections may be requested in case of cracks or other features detected during the first microsection sample or by request from the Approval Authority.

j. The integrity of the assembly shall be assessed by microsectioning.

NOTE Integrity covers PCB, solder joints, adhesives, packages.

k. Adhesive for thermal or mechanical purpose underneath a component shall be microsectioned.

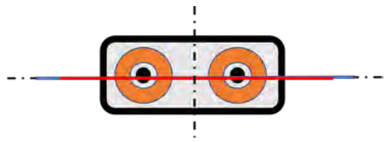
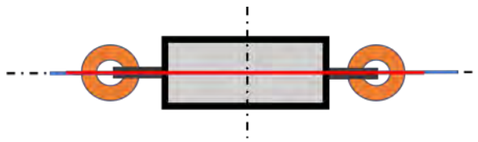
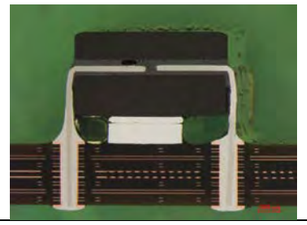
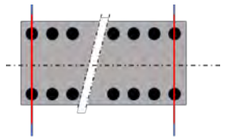
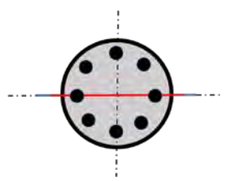
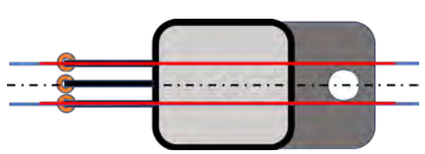
l. The Approval Authority shall have access to the moulded microsection and pictures.

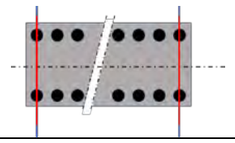
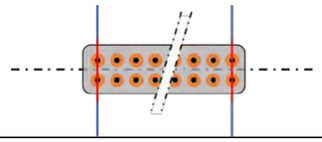
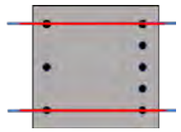
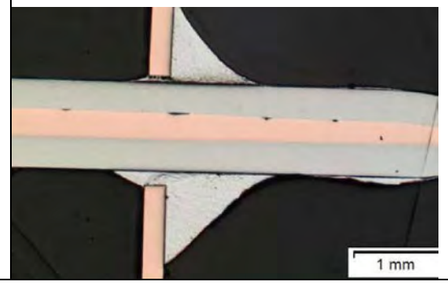
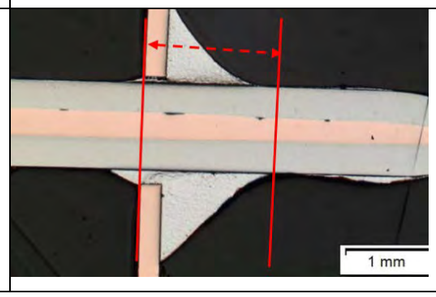
m. The verification board and associated microsections shall be stored for a period of at least ten years.

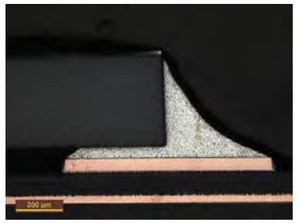
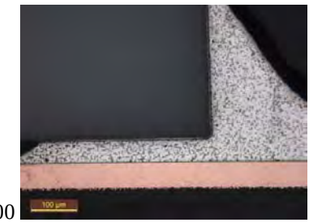
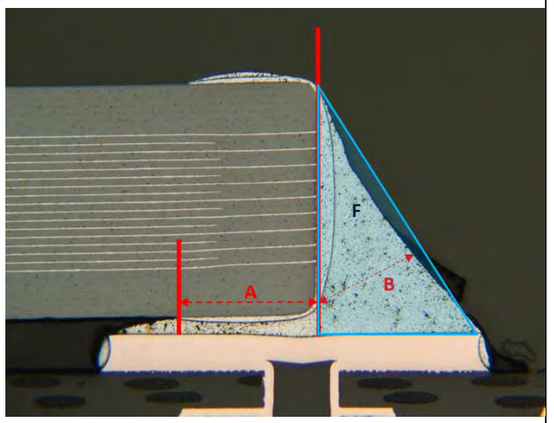
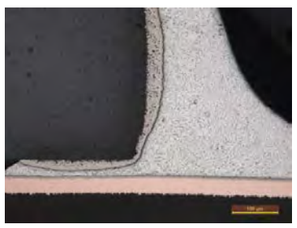
NOTE 1 It is good practice to store the boards until end of mission.

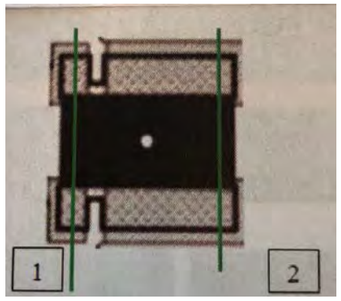
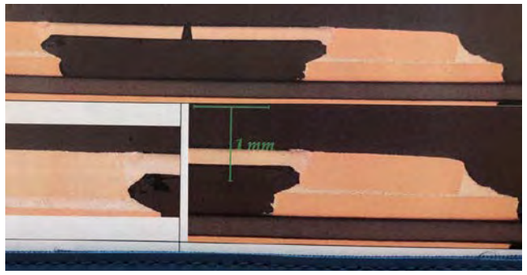
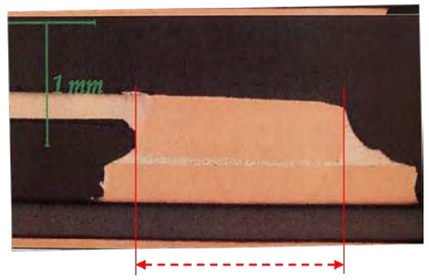
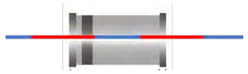
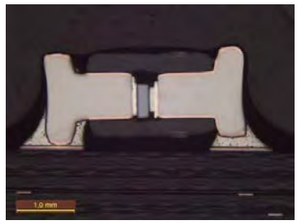
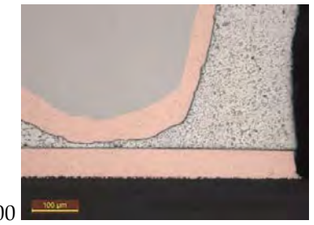
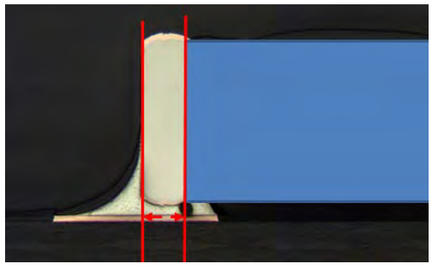
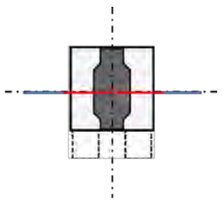
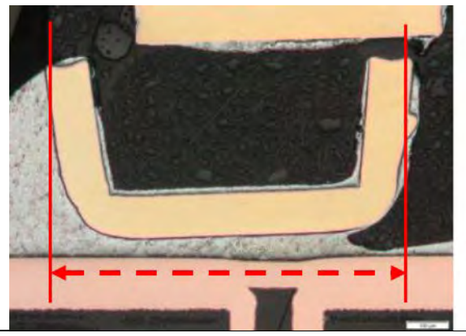
NOTE 2 Boards can assist the analysis of in-orbit failures.

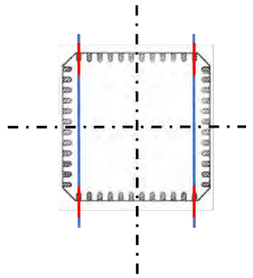
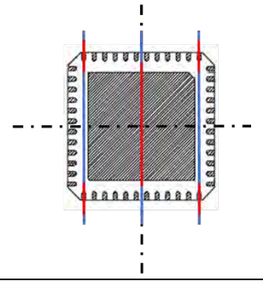
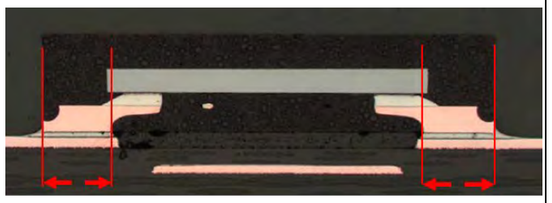
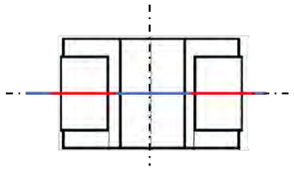
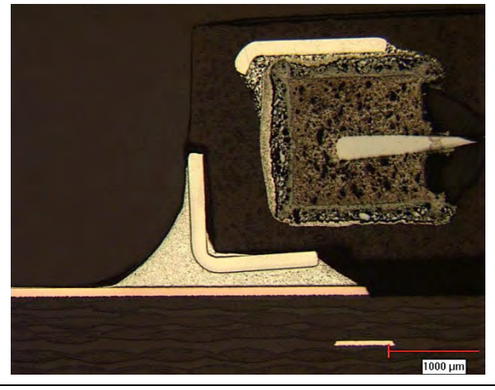
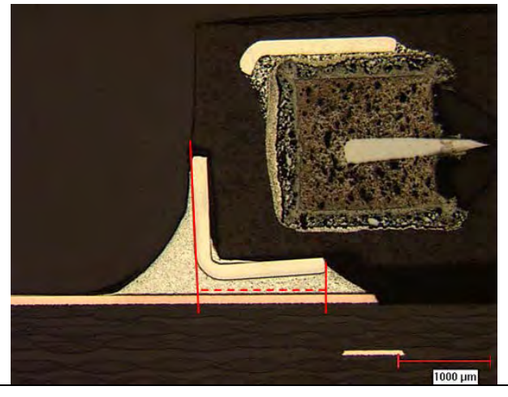
Table 14-5: Component microsection location and acceptance criteria

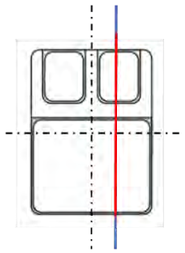
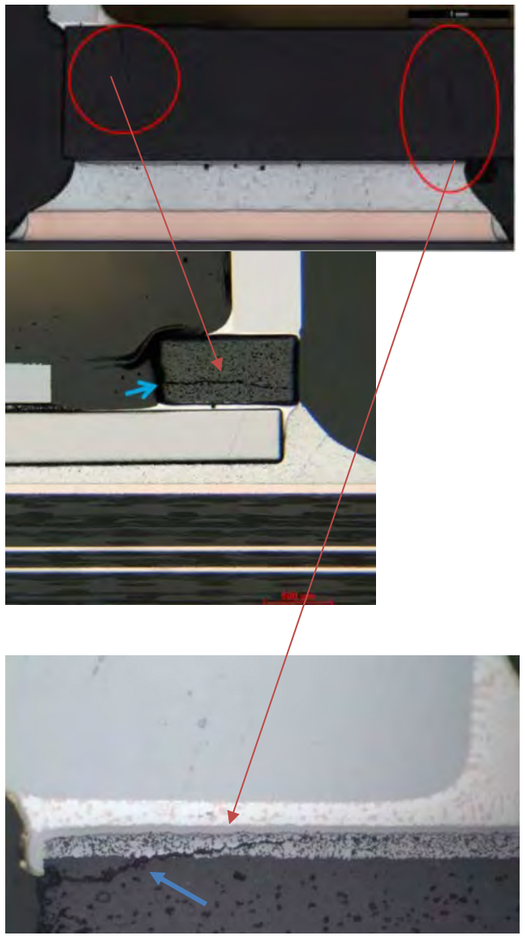
Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
Radial component	CKR capacitors				
Axial components	CH capacitors CNC capacitors RWR resistors				
Stacked capacitors				Not applicable	25% of PCB thickness (laminate)
T0 package component	TO-39-	 Microsection in the largest distance between two leads			
T0 package component with metal tab	TO254				

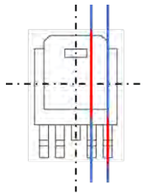
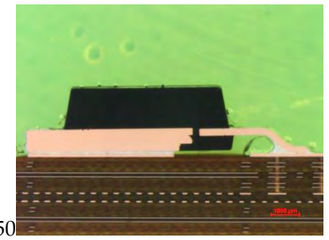
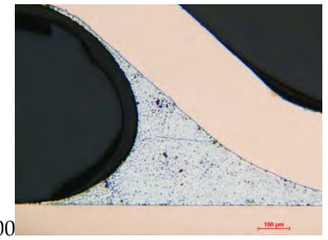
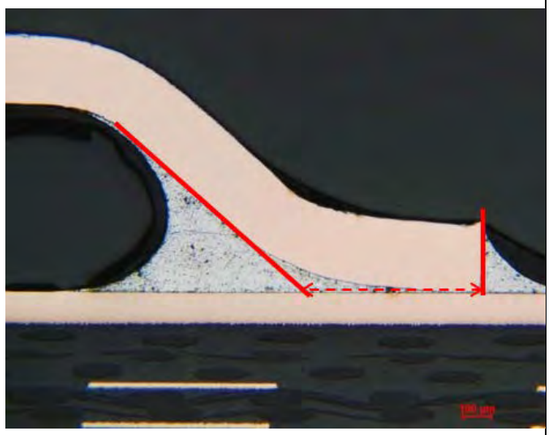
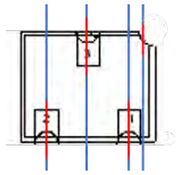
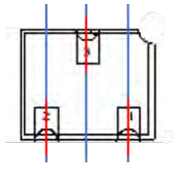
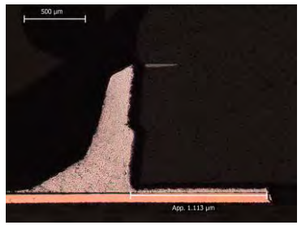
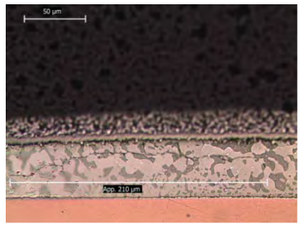
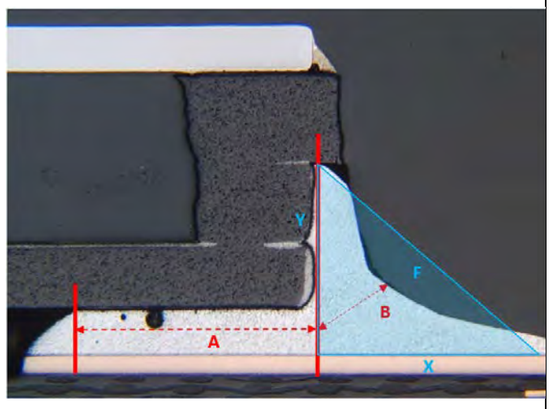
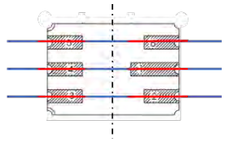
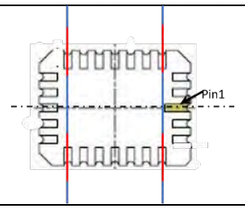
Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition		Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane			red-dotted line indicates critical zone	
Dual in Line Package (DIL or DIP)	Side brazed DIP>24 pins			Not applicable		25% of PCB thickness (laminate)
Connectors						
Radial magnetics	1553 transformers					
Sculptured flexible						a. No crack in the solder fillet on the solder side at completion of the test. b. Crack in the hole of the PTH acceptable less than 25% of critical zone

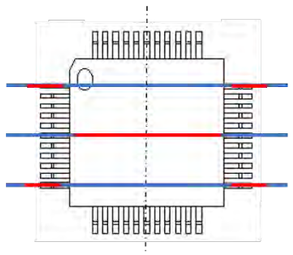
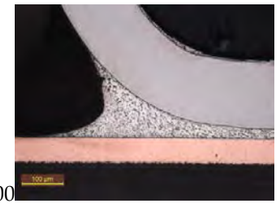
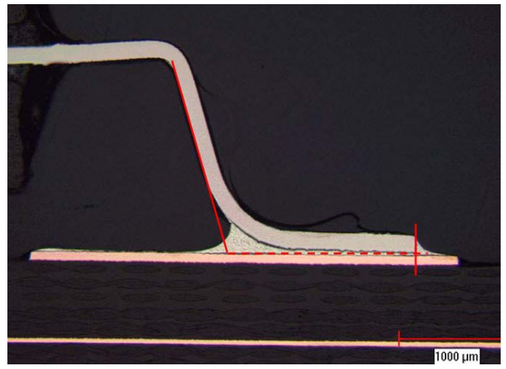
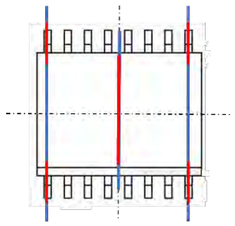
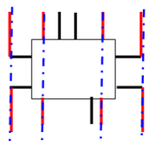
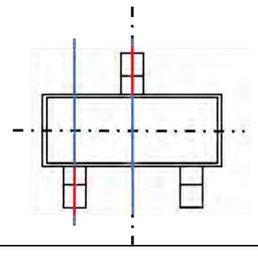
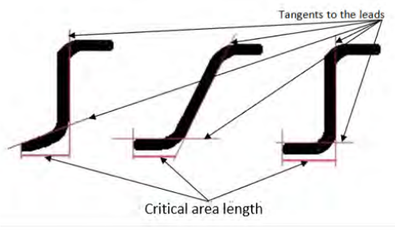
Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition		Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane			red-dotted line indicates critical zone	
Rectangular and square end-capped or end-metallized component with rectangular body	Chip resistors		x50  x200 			Crack length less than 60% of A+B, and no crack in fillet area F The vertical limit to the fillet area F shall be the outermost ceramic edge
	Chip capacitors		X50  X200 			
	Resistor array					

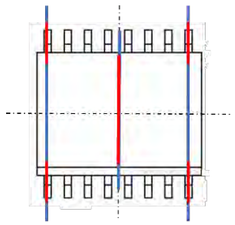
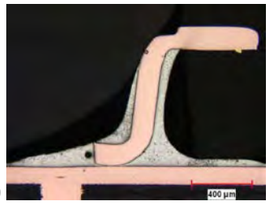
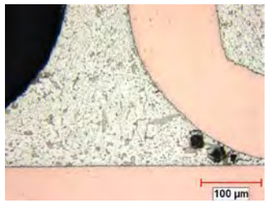
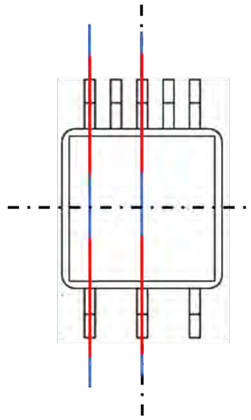
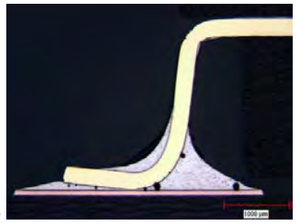
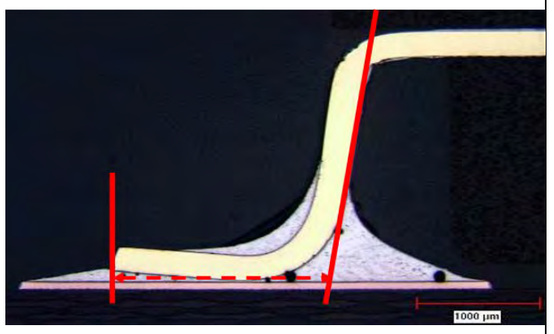
Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition		Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane			red-dotted line indicates critical zone	
Rectangular and square end-capped or end-metallized metallic component with rectangular body, leadless chip	CSM					No crack longer than 33% of lap connection
Cylindrical and square end-capped components with cylindrical body	MELF		X 50   X200	 		No crack longer than 33% of critical zone length
Bottom terminated chip component Bottom terminated chip component	Coil					No crack longer than 33% of lap connection

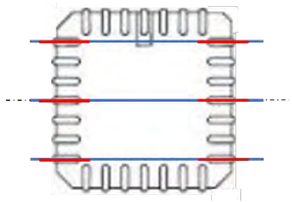
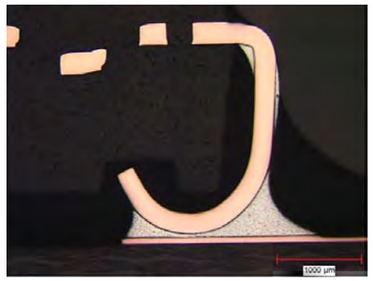
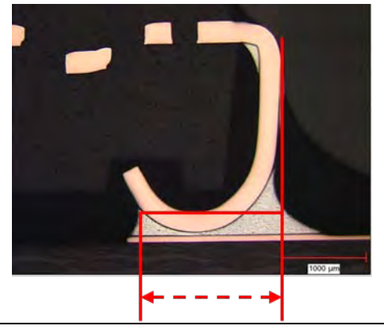
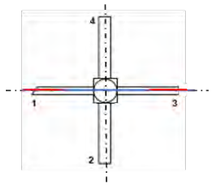
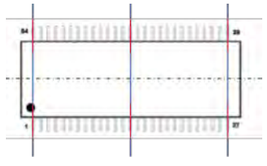
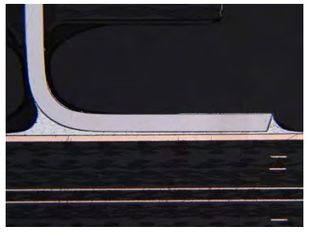
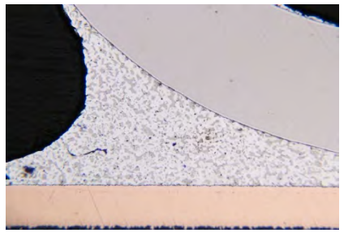
Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition		Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane			red-dotted line indicates critical zone	
	No lead Quad Flat Pack QFN	 When thermal plane is present, the third microsection is in the middle axis: 	 			No crack longer than 33% of lap connection
Component with Inward formed L-shaped leads	Tantalum chip capacitor					No crack longer than 33% of critical zone length

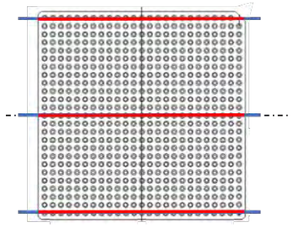
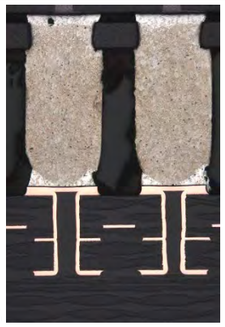
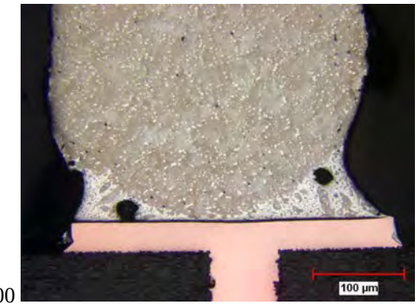
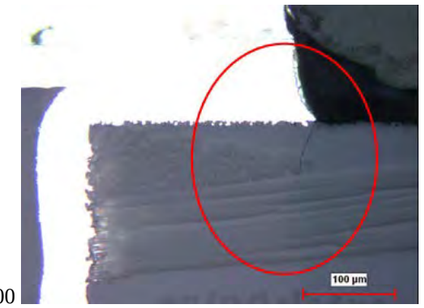
Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition		Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane			red-dotted line indicates critical zone	
Leadless component with plane termination	SMD0.5, SMD1, SMD2, SMD0.2	 + X-ray	Absence of cracks in the ceramic to be checked by visual inspection prior to microsectioning X50 			No crack longer than 33% of lap connection No cracks in the ceramic to be checked by visual inspection prior to microsectioning

Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition		Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane			red-dotted line indicates critical zone	
Leaded component with plane termination	DPAK/TO252 D2 PAK SOT 223	 X-ray+ micro section (lead + plane) Microsection plane in one edge. Additional microsection depending on lead configuration (different dimensions or shape)	 X50  X200			For lead, no crack longer than 33% of critical zone length For plane termination, X-ray criteria in accordance with clause 14.2.2.
Castellated chip carrier component The main component of this type is leadless ceramic chip carrier (LCCC)	LCC3	 With ground connection (microsection to be done in the middle of castellation)  Without ground connection	 x100  x500			Crack length less than 70% of A+B and no crack in fillet area F (blue area) OR Crack length less than 100% of A providing the following: - no crack in fillet area F - convex solder joint - wetting height (Y) 100% of castellation - solder wetting length on the solder footprint X shall be more than the wetting height Y The vertical limit to the fillet area F shall be the outermost ceramic edge in the castellation
	LCC with terminations on 2 faces	 all terminals to be microsectioned				
	LCC with termination on 4 faces					

<table>
<tr><th>Component type</th><th>Example component</th><th>Cross section planes</th><th>Example of views at min and max magnification</th><th colspan="2">Critical Zone definition</th><th>Acceptance criteria</th></tr>
<tr><td colspan="2">  </td><td>Terminal to cross section
Symmetry axis
Cross section plane</td><td></td><td></td><td>red-dotted line indicates critical zone</td><td></td></tr>
<tr><td rowspan="3">Flat pack and Gull-wing leaded component with round, rectangular, ribbon leads, Moulded magnetics</td><td>CQFP + MQFP</td><td> 
Centre micro-section to be done only when component is bonded.x100</td><td>x50 
x200 
Similar magnification to be applied for the assessment of the bonding lines.</td><td colspan="2" rowspan="3">  </td><td rowspan="3">No crack longer than 33% of critical zone length</td></tr>
<tr><td>FP, SO, SOIC</td><td> 
Centre micro-section to be done only when component is bonded.</td><td>x50 
x200  </td></tr>
<tr><td>FP with spider leads</td><td>  </td></tr>
<tr><td>SOT 23</td><td>  </td><td></td><td colspan="2">  </td><td>No crack longer than 10% of critical one length</td></tr>
</table>

Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition		Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane			red-dotted line indicates critical zone	
Flat pack and Gull-wing leaded component with round, rectangular, ribbon leads, Moulded magnetics	TSOP		x50  x200 			No crack longer than 10% of critical one length
	1553 interface transformers or specific transformers	 Microsection plane in one edge. Additional microsection depending on lead configuration (different dimensions or shape)	x25  x200 			No crack longer than 33% of critical zone length

Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
"J" leaded component	ceramic leaded chip carriers (CLCC) and plastic leaded chip carriers (PLCC).				No crack longer than 33% of critical zone length
Components with ribbon terminals without stress relief (flat lug leads)					No crack longer than 33% of critical zone length
Stacked modules components with leads protruding vertically from bottom		 Can be reduced when package is less than 50 leads	x25  x200 		No crack longer than 33% of critical zone length OR No crack longer than 50% of critical zone length, providing leads >3 mm and 5 micro-sectioned components

Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition		Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane			red-dotted line indicates critical zone	
Area Array components (Capability Phase only)	CCGA		x25  x100  x200  Presence of cracks in the laminate under investigation	Not applicable		See 13.3.2Visual inspection for capability samples only

14.8.3 Verification acceptance and rejection criteria

a. Prior to microsectioning, the components shall be in conformance with the assembly requirements of clause 9 and 10.5.

b. After microsectioning, cracks in solder joints shall be in compliance with requirements of Table 14-5.

c. Cracks present outside the critical zone shall be considered acceptable.

d. Cracks in the mechanical bonding shall not be accepted unless the criteria defined in Table 14-5 are met.

e. Cracks in the thermal bonding may be accepted at the completion of the verification testing, when they are perpendicular to PCB surface plane.

f. Any damage to the component beyond the ones acceptable by the component datasheet shall be identified as a verification failure.

g. The presence of AuSn intermetallic on the top of LCC package shall not lead to a rejection.

14.9 Anomalies in PCB and sculptured flex during verification

a. After verification testing the acceptance criteria of ECSS-Q-ST-70-60 clause 10.3 and 10.5 shall apply, except for the case specified in requirements 14.9b and 14.9c.

NOTE ECSS-Q-ST-70-60 includes acceptance criteria for cracks in dielectrics for PTH.

b. Anomalies outside the conditions specified in requirement 14.9a may be accepted providing that at least one of the following conditions is met:

1. Presence of anomaly also during PCB procurement, either on the PCB coupons or in certificate
2. Presence of anomaly also on a spare non-assembled nor tested PCB.
3. Presence of anomaly also on a spare footprint, included on the verification board, showing that the defect was not caused by the assembly processes.

NOTE It is good practice to include additional footprints on the verification board, which are not populated, to assist failure investigations.

c. Cracks in the dielectrics under SMT footprints, outside the conditions specified in requirement 14.9a, may be accepted providing that:

1. the dielectric crack does not propagate more than 80 µm and
2. the remaining insulation distance of the flight PCBs is in conformance with the PCB definition dossier.

d. Cracks in the Printed Circuit Board that have not been identified in the clause 10 of ECSS-Q-ST-70-60 shall be unacceptable.

e. Defects, such as footprint lifting, cracks in laminate, cracks in via, cracks of tracks, PCB delamination shall be recorded as a nonconformance and analysed.

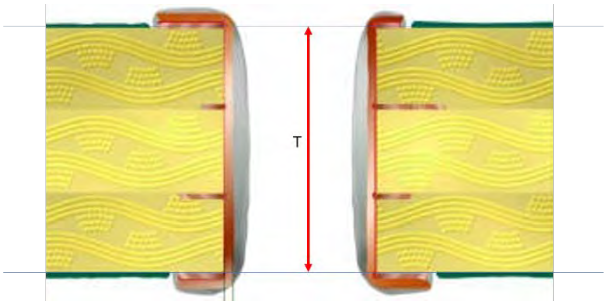


Figure 14-2 Measurement of PCB thickness

14.10 Soldering log

a. A soldering log shall be put in place for all soldering processes involved in a board manufacturing during verification programme.

b. The soldering log shall contain as a minimum the following data:

1. Board identification
2. Board technology description: materials, build up, ground planes
3. Soldering process identification
4. Main parameters for the soldering process
5. List of identified defects
6. Calculation of percentage of defects
7. Inspectors observations
8. Any miscellaneous remark of interest.

NOTE An example of a soldering log for a wave process soldering is given in Figure 14-3.

c. The soldering log shall be made available to the Approval Authority.

Part identification **Wave soldering parameters** **Assembly: _____ PCB P/N: _____ Preheat temp: _____ Solder temp: _____ Conveyor Speed: _____ Wave height: _____**																				
Description					**Insufficient**						**Excess**					**Miscellaneous**				
MLB ❑ No. of thru holes: _____ ❑ No. of layers: _____ Ground plane estimated area: Topside: _____% Botside: _____%																				
Acceptable rework level: ___% total	Date	Inspector	Insptn. S/N	T: component side; B: bottom side	Lead poor wetting	Pad poor wetting	Large voids	Small bottomless voids	Insufficient solder flow-thru	Depressed solder	Bridging	Icicling	Accumulations	Excess solder (lead obscured)	Stress-relief bends filled	Raised component	Other solder discrepancies (specify)	Subtotals	% for rework
Inspector's observations:				T															
				B															
				T															
				B															
Totals:																			

Figure 14-3: Example of soldering log for joints discrepancy log

15 Outsourcing

15.1 General

a. The supplier that performs assembly for the customer may be assigned as "outsourcing" providing that the following conditions are met

1. "Outsourcing" activities are limited to degolding and pretinning, lead forming, hand soldering, bonding, staking and conformal coating.
2. The manufacturing at the supplier site is performed with the same materials as the one used by the customer.
3. The manufacturing at the supplier site is performed in compliance with the manufacturing procedures of the customer PID.
4. In case the "outsourcing" includes lead forming activities, the demonstration that lead geometry is identical are provided to the customer.
5. The customer is responsible for-the assembly of the supplier,
6. The supplier fills in the manufacturing log sheet of the customer.
7. In case the supplier is not equipped to fill in the manufacturing log sheet of the customer, he can use his own manufacturing log sheet providing that it has been reviewed and accepted by the customer.
8. All operators and inspectors working at the supplier site are trained and certified according to clause 17.8a and being active in their certification status.
9. All operators and inspectors working at the supplier site for the customer as outsourcing are trained on customer applicable PID procedures and certified by the instructor of the customer.

NOTE For the requirement 15.1a.2 Ideally those materials are provided in the kitting.

b. The operators and inspectors shall work only on one set of specified process procedures at a time at the supplier site.

c. The customer shall issue and maintain a certification matrix of the certification status of the supplier's operators and inspectors including the name of the instructor and the supplier assembly contact point name.

d. The manufacturing dossier of the boards and unit shall identify the operations performed by the supplier.

e. The customer shall appoint a person in charge of NCRs issued by customer and supplier.

f. The supplier shall be informed about assembly NCRs in the customer assembly line.

g. The customer shall conduct an audit at supplier according to clause 13.1.3 in order to verify the compliance of the assembly line.

h. The customer shall provide to the Approval Authority the audit report.

i. In case of modification in the procedures, the supplier operators and inspectors shall be informed, trained and certified according to requirement 15.1a.9.

j. KIPs shall be performed by the customer inspector,

k. The customer shall have a storage and transportation procedure for the hardware manufactured at supplier assembly line,

l. Incoming inspections of the assembly shall be performed by the customer to verify absence of damage due to the storage and transportation,

m. Every 4 years the customer shall invite the Approval Authority to participate the audit of the supplier assembly line, in compliance with requirement 13.1.3f.

n. The customer shall list in its PID the supplier as “outsourcing” to manufacture hardware.

o. The customer PID shall identify the certification matrix with the associated names of the supplier involved personnel.

16
Process identification document (PID)

16.1 General

16.1.1 Overview

The purpose of the PID is to establish a precise reference for the assembly processes approved in accordance with this Standard.

The PID provides a standard reference against which any anomalies occurring after the approval can be examined and resolved.

16.1.2 Document preparation

a. Prior to any start of verification, the supplier shall provide a draft PID to the Approval Authority, in conformance with the DRD in Annex C.

b. The PID may supersede the requirements from this standard in case supplier can demonstrate that any deviation recorded in the PID is approved on the basis of tests results.

16.1.3 Approval

a. The PID shall be submitted to the Approval Authority

b. The Approval Authority shall approve the PID.

NOTE The approval can be achieved by PID signature or minutes of meeting being signed by the Approval Authority.

16.1.4 Contact person

a. The supplier shall appoint a contact person for assembly topics.

16.2 Process identification document update

a. A PID shall represent the verified manufacturing processes and production controls.

b. Any proposed change to the PID shall be agreed by the Approval Authority.

c. At least every two years the supplier shall perform a review of the PID, the summary table and the relevant applicable documents for agreement by the Approval Authority.

d. The PID shall be managed in accordance with configuration control requirements of ECSS-M-ST-40.

17
Quality assurance

17.1 General

a. Requirements from clause 5 from ECSS-Q-ST-20 shall apply for "Quality assurance".

17.2 Data

a. Quality records shall be retained for at least ten years, or in accordance with the project contract.

NOTE Example of quality records are travellers log, work orders.

b. Quality records shall be gathered in the Verification report in conformance with the DRD in Annex B.

17.3 Nonconformance

a. The requirements from clauses 5 and 6 from ECSS-Q-ST-10-09 shall apply for "Nonconformance".

17.4 Calibration

a. Equipment and tools, degolding and pretinning bathes, soldering equipment, and measuring equipment shall be calibrated within a period of one year.

b. A suspected or confirmed tool or equipment failure shall be recorded as a project nonconformance.

NOTE The records can aid early detection of a trend towards nonconformance.

c. Defective or out of calibration date equipment or tools shall be labelled or removed from work areas.

d. The Approval Authority shall be notified of the nonconformance.

17.5 Traceability

a. The requirements from clause 5.2.5 of ECSS-Q-ST-20 shall apply for traceability.

17.6 Workmanship standards

a. The supplier shall prepare in-house visual workmanship standards to be made available to each operator and inspector.

NOTE 1 Examples are: Satisfactory work samples or visual aids which illustrate the quality characteristics of all types of soldered connection involved in the task.

NOTE 2 The illustrations presented in Annex F and Annex E this standard can be included as part of the examples.

17.7 Inspection points operation

a. During all stages of the process, the inspection points defined in the manufacturing flow chart shall be carried out.

b. The inspection shall be performed in conformance with clause 12

17.8 Operators, inspectors and instructors training and certification

a. Operators, inspectors and instructors shall be trained and certified at a school in compliance with ESA STR-258 or in-house training authorised by the Approval Authority.

NOTE The supplier company is responsible, in particular, for checking the constant visual acuity of its workers

b. Trained and certified personnel shall be employed for soldering operations and inspections.

c. A training programme shall be developed, maintained and implemented by the supplier to provide excellence of workmanship and personnel skills in manual and SMT soldering

NOTE Records of training, testing and certification status of the operators are maintained for at least 10 years.

d. The training programme shall include procedures for the training, certification, maintenance of certified status, recertification and revocation of certified status for soldering and inspection personnel.

e. Certification shall be based on objective evidence of soldering quality, resulting from test and inspection of soldered joints.

f. Personnel shall be retrained or re-assessed in the following circumstances:

1. Repeated quality non-conformance.
2. Change in soldering techniques.
3. Change in soldering parameters.
4. Additional process skills

g. The operators performing X-ray inspection shall be trained and in-house certified to perform and assess X-ray results.

17.9 Quality records

a. The following documents, as a minimum, shall be made available to supplier

1. PID.
2. Audit report established by the Approval Authority.
3. Verification report.

Annex A (normative)
Verification programme - DRD

A.1 DRD identification

A.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-61, requirement 13.1.4a.

A.1.2 Purpose and objective

The purpose of the Verification programme DRD is to detail the requirements for the documentation of the verification programme.

A.2 Expected response

A.2.1 Scope and content

a. The verification programme documentation shall contain as a minimum the following:
   1. Indication of process of the assembly:
      (a) soldering process
      (b) repair process.
   2. Substrate information:
      (a) PCB material and manufacturer
      (b) PCB footprint surface finish
      (c) Number of layers
      (d) Thickness
      (e) Built up with identification of signal and full copper plane
      (f) Connection of the footprints to the internal layer representative of the FM
      (g) Location of the components on the PCB
      (h) For through hole component, ratio of hole to lead diameter
      (i) Location of the mechanical fixation or stiffeners if any
      (j) Number of PCB used for the verification programme.

3. Materials used
   (a) Solder paste and wire designation, commercial trade mark, and composition with associated flux class
   (b) Flux class used for pretinning and soldering
   (c) Conformal coating
   (d) Adhesive, potting, underfill and encapsulants used for mechanical and for thermal purpose
   (e) Solvent
   (f) Others.
4. List of components with their materials leads and finish
5. Environmental test conditions and facility
6. Electrical continuity test specification, procedure
7. Verification method Microsection or Electrical monitoring
   (a) Microsection laboratory.
8. PID and Manufacturing document process references
9. Verification workflow
10. Verification by similarity
11. Certification status of the operators and inspectors
12. Compliance status of the operators and inspectors
13. Compliance of the manufacturing room
14. Additional information.

b. The content of Verification programme specified in requirement A.2.1a may be tailored for companies already having an approved PID in accordance with this standard.

A.2.2 Special remarks

None.

Annex B (normative)
Verification report - DRD

B.1 DRD identification

B.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-61, requirement 13.1.6a.

B.1.2 Purpose and objective

The purpose of the Verification report DRD is to summarize all the verification test specifications, procedures and test results which are relevant for the approval of the assembly component verifications.

B.2 Expected response

B.2.1 Scope and content

a. The verification documentation shall contain as a minimum the following:
   1. Indication of process of the assembly:
      (a) soldering process
      (b) repair process.
   2. PCB information:
      (a) PCB material and manufacturer
      (b) PCB footprint surface finish
      (c) Number of layers
      (d) Thickness
      (e) Built up with identification of signal and full copper plane
      (f) Connection of the footprints to the internal layer representative of the FM
      (g) Location of the components on the PCB
      (h) For through hole component, ratio of hole to lead diameter
      (i) Location of the mechanical fixation or stiffeners if any
      (j) Number of PCB used for the verification programme.

3. Materials used
   (a) Solder paste and wire designation, commercial trade mark, and composition with associated flux class
   (b) Flux class used for pretinning and soldering
   (c) Conformal coating
   (d) Adhesive for mechanical, and for thermal
   (e) Solvent
   (f) Others.
4. List of components with their materials leads and finish (including traceability)
5. Environmental test conditions and facility
6. Visual inspection report established in conformance with the requirements of clause 12
7. Summary of cleanliness test results in conformance with clause 11.1.3 of ECSS-Q-ST-70-61 or equivalent process
8. Tests results concerning the warp (bow) and twist of circuit board in conformance when applicable
9. Electrical continuity test report for multilayer boards
10. Verification method Microsection or Electrical monitoring
    (a) Microsection laboratory
11. PID and Manufacturing document process references
12. Verification workflow
13. Verification by similarity
14. NCRs
15. Certification status of the operators and inspectors
16. Compliance status of the operators and inspectors
17. Compliance of the manufacturing room
18. Additional information.

b. The verification report shall contain the results of all tests performed according to clauses 12 and 14.

c. The verification report shall contain photographic evidences of the tested assembled boards where possible.

d. The verification report shall contain the manufacturing soldering log according to clause 14.9.

e. The verification report shall contain the list of all NCRs referring to assembly and test of verification boards and associated reports.

B.2.2 Special remarks

None.

Annex C (normative) Process Identification Documentation (PID) - DRD

C.1 DRD identification

C.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-61 requirement 16.1.2a.

C.1.2 Purpose and objective

The purpose of the PID is to consolidate the overall management, process and facilities utilised during the manufacturing and verification of the assembly.

C.2 Expected response

C.2.1 Scope and content

<1> SECTION 1: Document Format

a. The PID shall contain the following information about the Document Format:
   1. Cover page: document title, document reference, revision number and date, page numbering, signing of Production and Quality representatives,
   2. Follow-up of PID updates: registration of PID updates indicating the nature of the update and the sections and pages updated,
   3. Purpose and scope of the document,
   4. Table of contents.

<2> SECTION 2: Manufacturing control

a. The PID shall contain the Manufacturing control flow chart of the verified assembly.

NOTE 1 This illustrates the various stages of procurement, manufacturing and inspection operations specific to this technology in a flow chart format.

NOTE 2 It can be used to identify, among others:

- the operation,
- the body responsible for its implementation,
- related documents: (only their reference),
- procurement specifications (for materials),
- acceptance inspection procedures (for materials and components),
- manufacturing procedures,
- manufacturing and quality control procedures during and at the end of production.

<3> SECTION 3: Specifications

a. The PID shall contain the following information about Specifications:

1. List of procurement specifications, assembly procedures and inspection procedures concerning the technology dealt within the PID, including the precise title, the reference or number, the revision number and date of each document
2. Printed circuit design rules in compliance with requirements from ECSS-Q-ST-70-60.
3. General Quality Assurance documents relating to the technology.

<4> SECTION 4: Organisation

a. The PID shall contain the following information about Organisation:

1. Represented as a flow chart: organization of the company, organization of production department and organization of the quality Department.
2. Focal point and PID responsible,
3. Operators and inspectors' certification methodology.

<5> SECTION 5: Manufacturing traveller or log file

a. The PID shall contain as a minimum the following information about the Manufacturing traveller or log file:

1. The sequencing of the various operations in their logical order of execution,
2. The references of the documents referred to and used during these operations,
3. The references of the Quality documents to trace the various batches of material used (record reference), together with the work stations and tools employed,
4. The signatures of the various actors with the date on which the task was completed.

<6> Section 6: List of verified technologies

a. The PID shall contain as a minimum the following information about the list of verified technology:

1. List of materials,

2. Temperature and time profiles for the soldering machines used in the verification,
3. List of verified components per assembly configuration,
4. List of assembly sensitive components,
5. List of components with limited project verification,
6. For limited project verification, non-compliance with clause 13 shall be clearly identified.

<7> SECTION 7: Description of production line

a. The PID shall contain as a minimum the following about the Description of production line:
   1. Layout of premises with associated surface area, with indication of location of production machines and quality inspection,
   2. Working environment; cleanliness class, ambient temperature limits, humidity and positive pressure limits for each type of activities.

<8> SECTION 8: List of equipment

a. The PID shall contain a list of all machines and tools utilised during the manufacturing activity.

<9> SECTION 9: List of laboratory services

a. The PID shall contain range and capability of supporting laboratory services.

<10> SECTION 10: Project assembly heritage

a. The PID shall contain a list of assembled board with associated assembly process by year manufactured in accordance with the PID.

C.2.2 Special remarks

None.

Annex D (normative)
Assembly Summary Table – DRD

D.1 DRD identification

D.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-61, requirement 13.1.7d.

D.1.2 Purpose and objective

The purpose of the assembly summary table is to consolidate the approval status of the boundary conditions for the verification activity.

An assembly summary table is issued for each assembly process.

D.2 Expected response

D.2.1 Scope and content

a. The assembly summary table shall include the following data:
   1. Assembly processes
   2. PID reference with issue
   3. Solder type for machine reflow and for hand assembly
   4. Conformal coating
   5. Substrate type
   6. Component data.

NOTE An example of a component type preparation and mounting configuration table is given in Figure D-1.

D.2.2 Special remarks

None.

Component family	Package	Manufacturer	Package dimensions	Bonding material (under component)	Staking material (edge or corner)	Termination material	Lead finish	Pitch (mm)	Nominal Termination thickness (mm)/ Nominal width	In-House degolding / pretinning	In-house lead forming Yes/No/NA	Artificial stand-off Yes/No	Final report
Ceramic chip	C0603 Type I		Length, width	NA	NA		Sn/Pb	NA	NA	No	N/A	No	
Ceramic	C0603 Type II										N/A		
Ceramic resistor	R0805			NA	NA		Sn/Pb	NA	NA	No	N/A	No	
Diode	D5-B										N/A		
Tantalum capacitors													
IC	FP10 Bottom brazed			yes	One the side	Alloy42	Gold	1,27	0,25	yes	yes	NA	
CQFP	CQFP196 top brazed					Kovar					No		

Figure D-1: Example of component type preparation and mounting configuration

Annex E (normative)
Visual workmanship standards for through hole component

E.1 Soldered clinched terminals

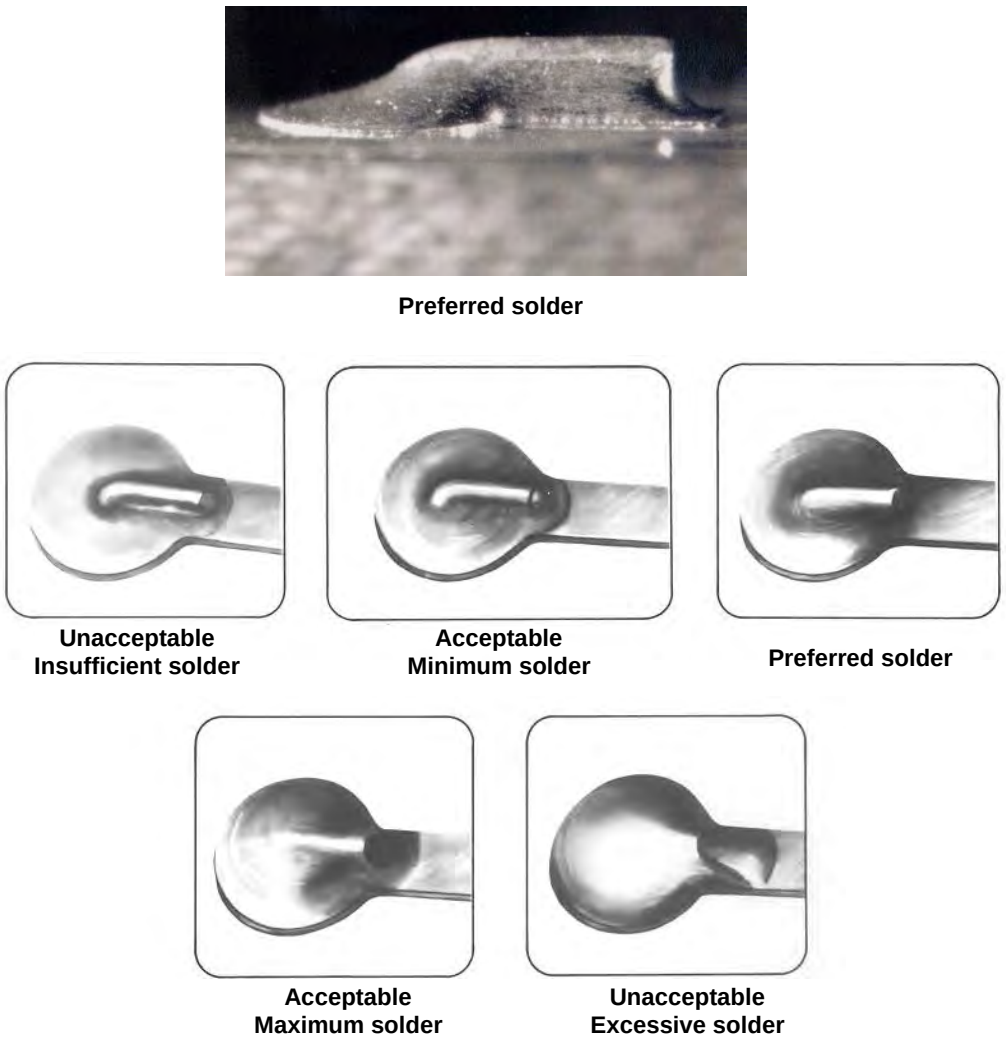


Figure E-1: Soldered clinched terminals

E.2 Soldered stud terminals

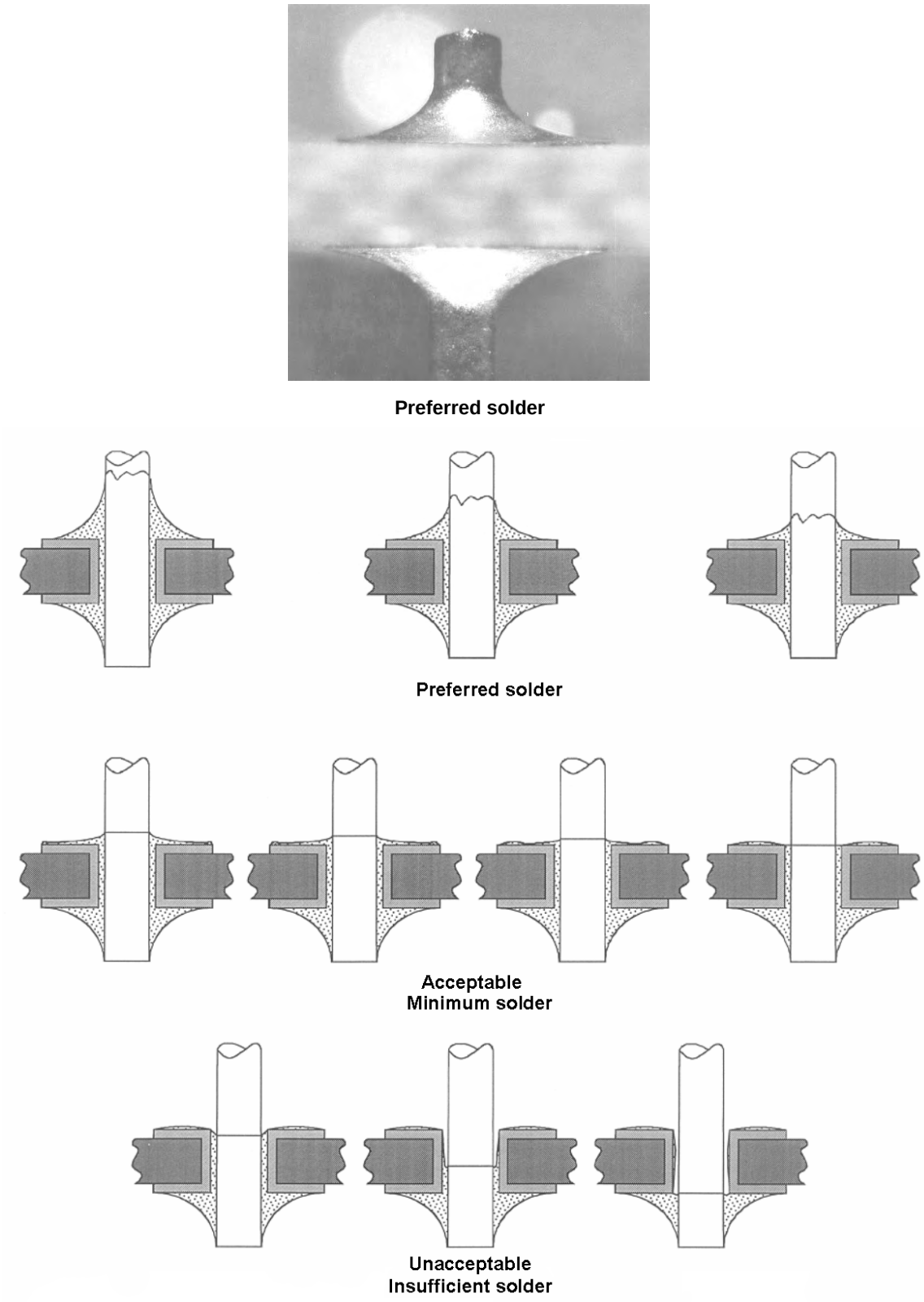


Figure E-2 : Soldered stud terminals

E.3 Soldered turret terminals

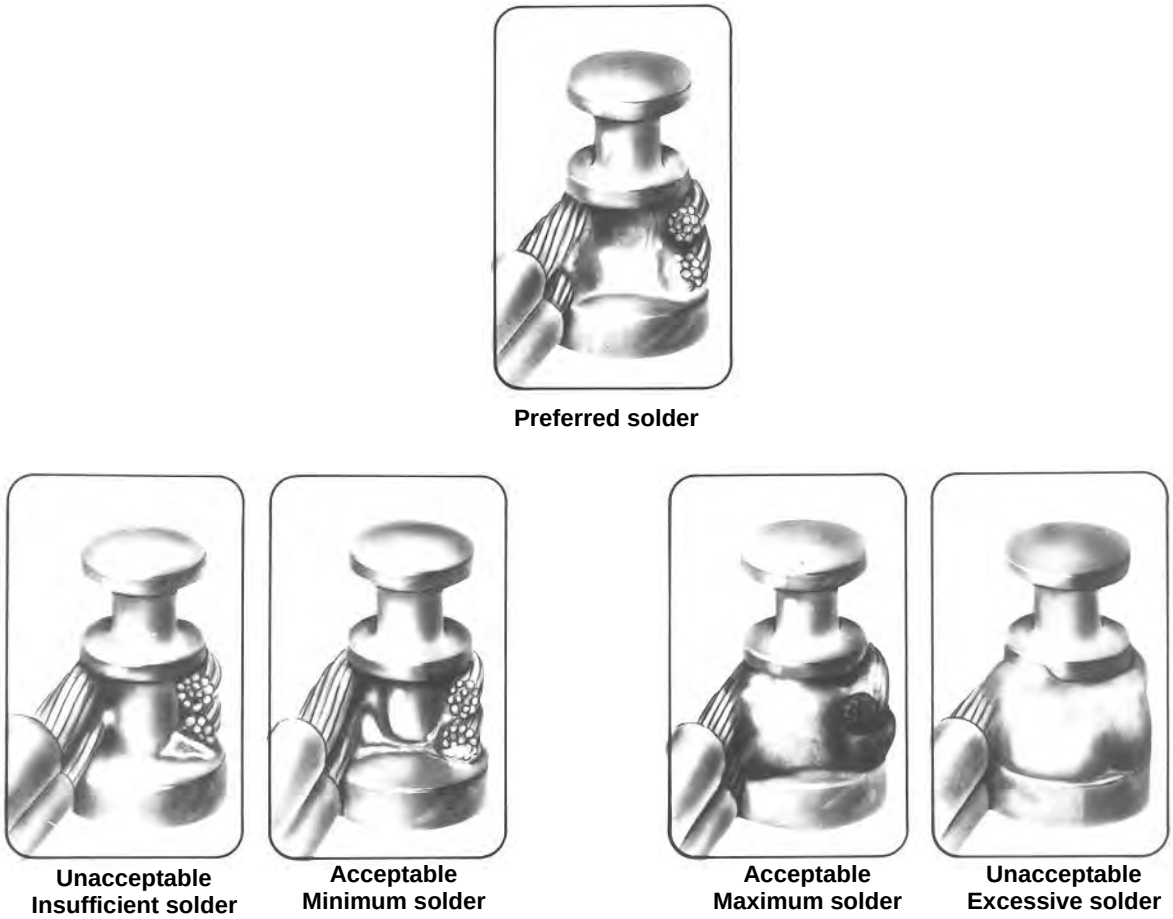


Figure E-3: Soldered turret terminals with twin conductors

E.4 Solder turret terminals

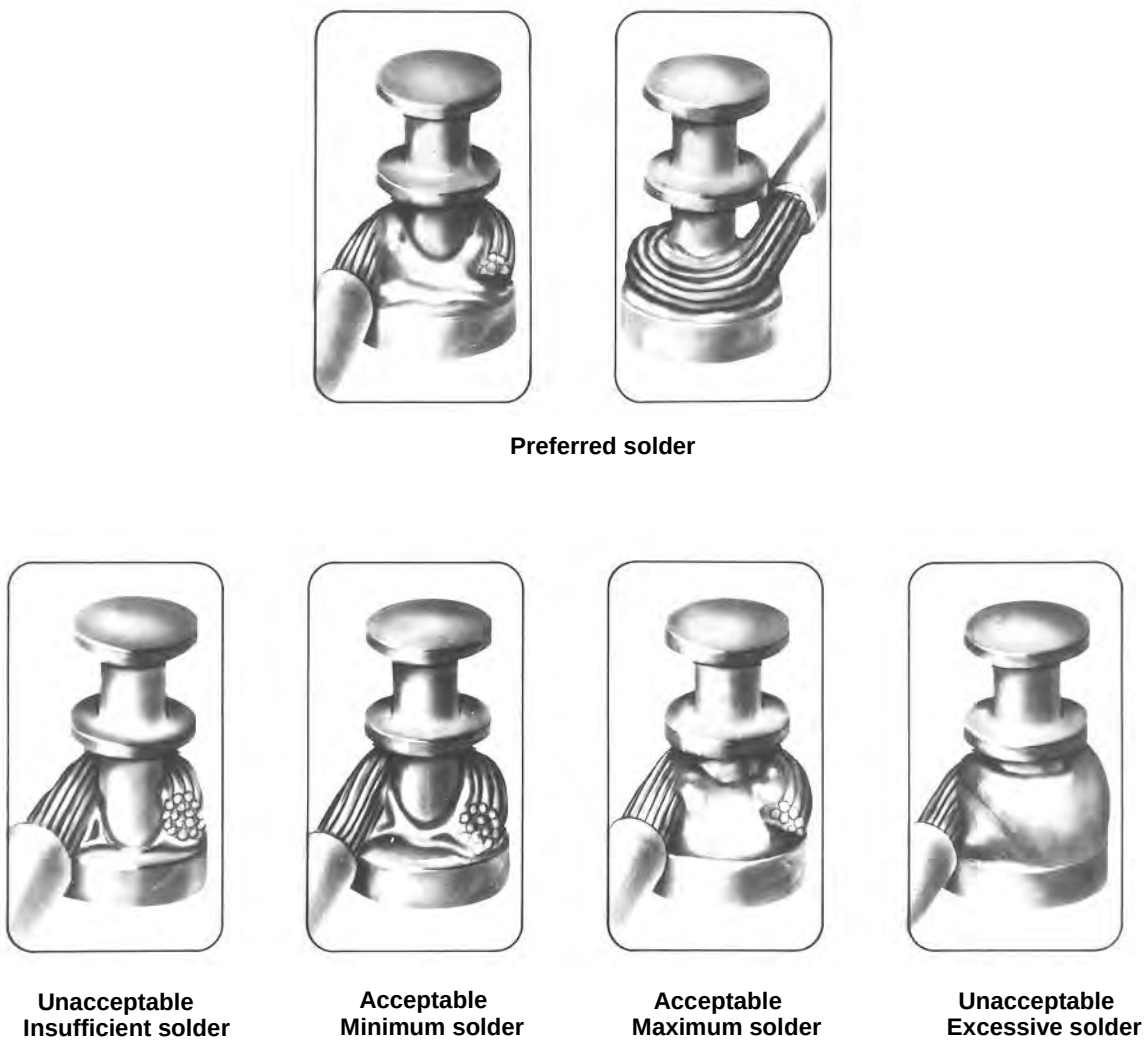


Figure E-4: Soldered turret terminals with single conductors

E.5 Soldered bifurcated terminals

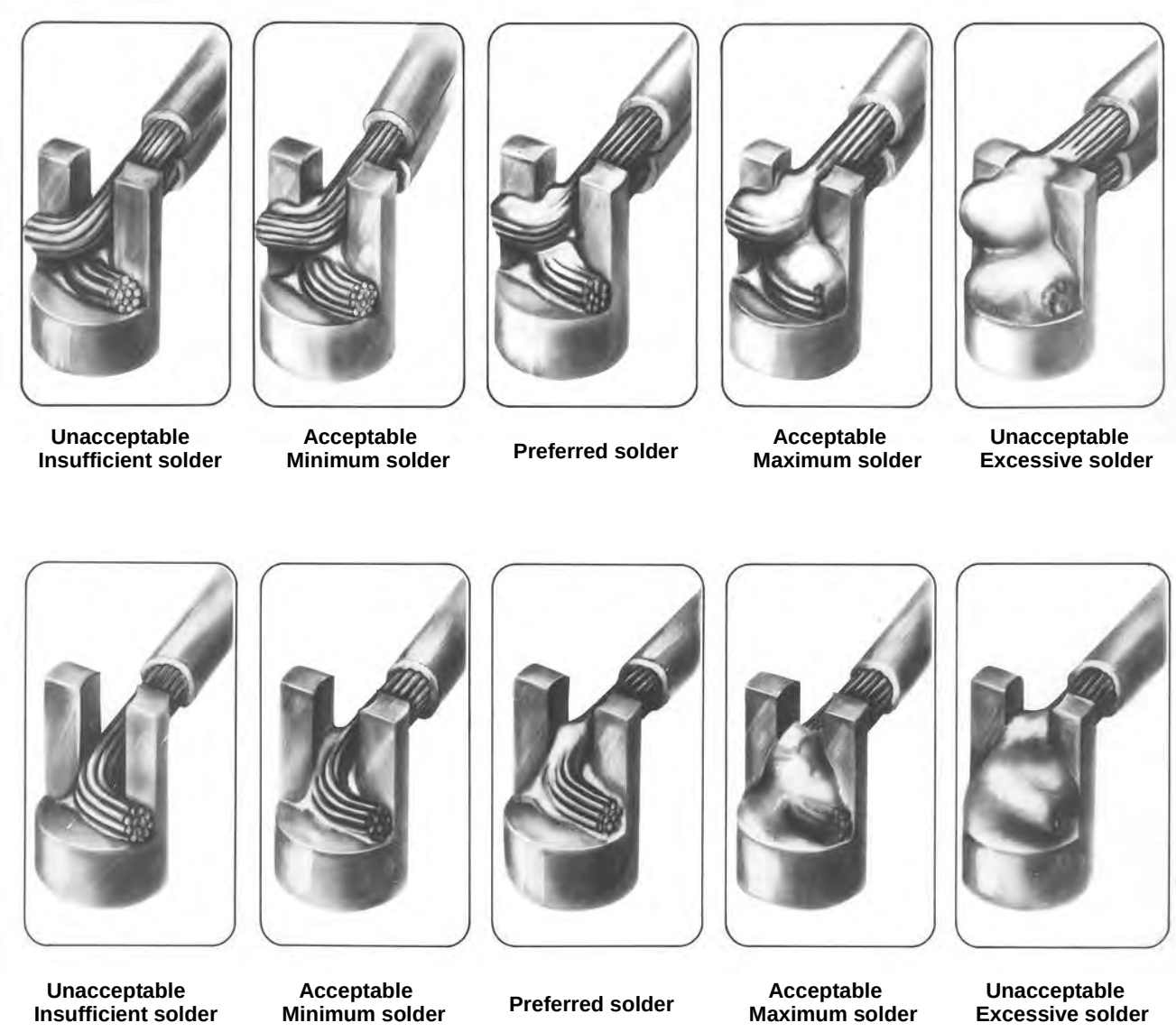


Figure E-5: Soldered bifurcated terminals

E.6 Soldered hook terminals

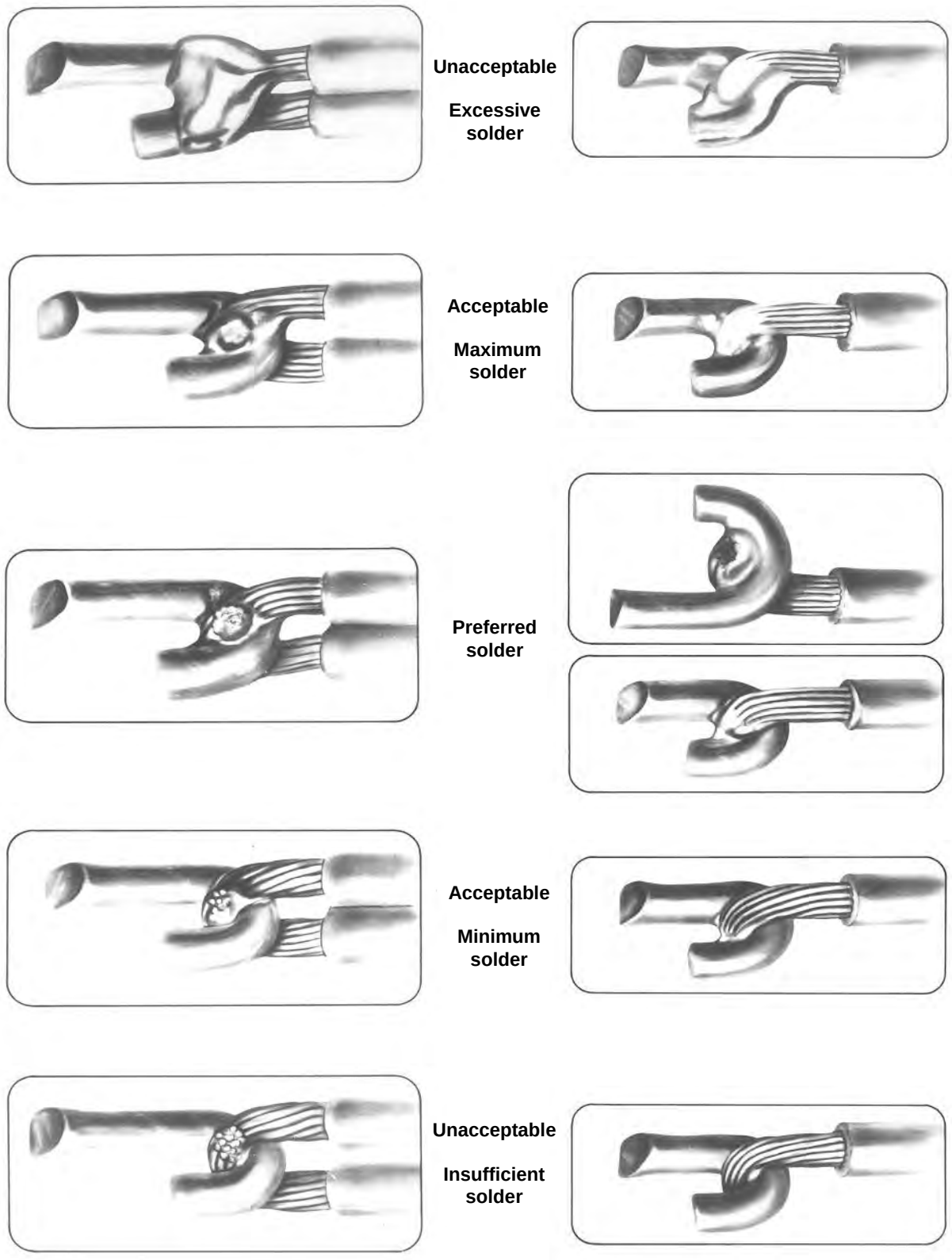
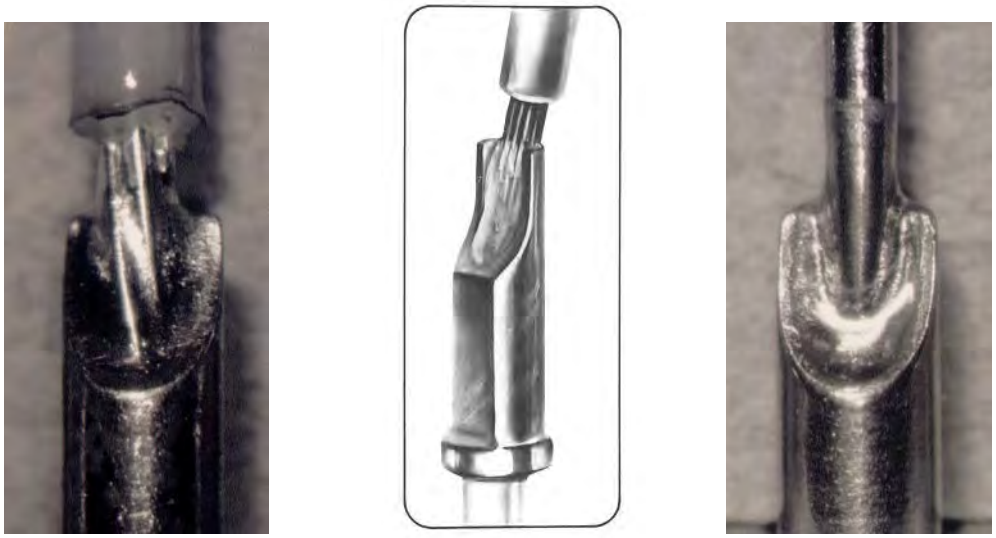
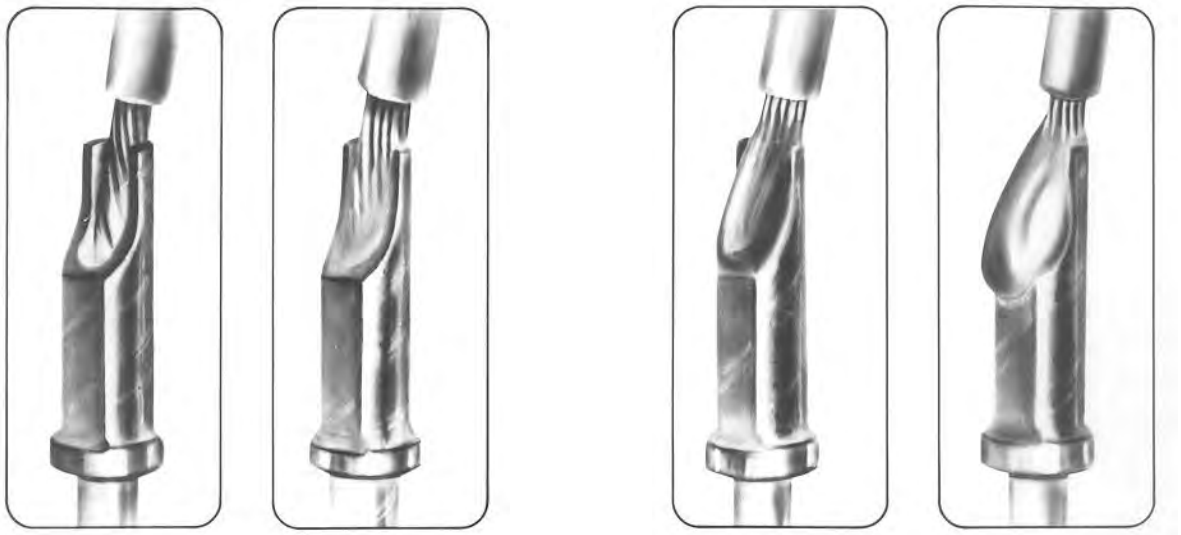


Figure E-6: Soldered hook terminals

E.7 Soldered cup terminals



Preferred solder



Unacceptable
Insufficient solder

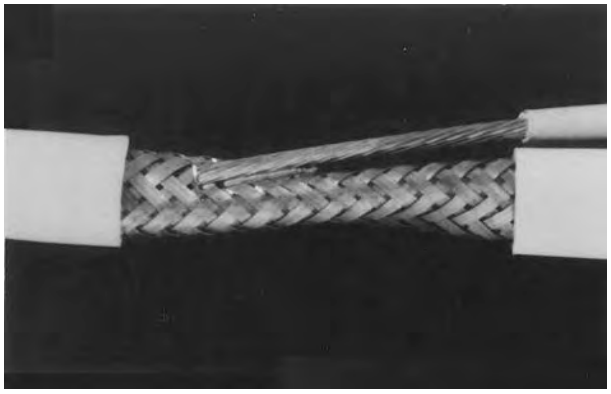
Acceptable
Minimum solder

Acceptable
Maximum solder

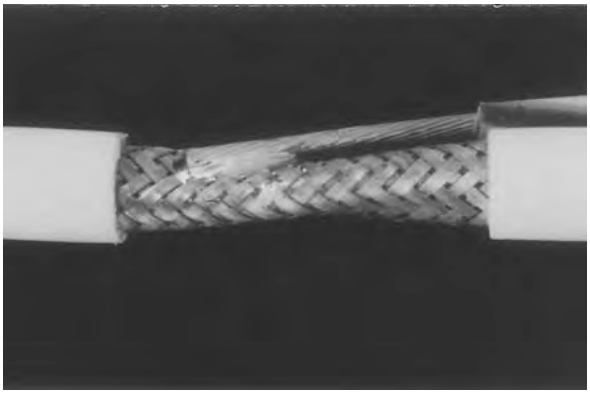
Unacceptable
Excessive solder

Figure E-7: Soldered cup terminals

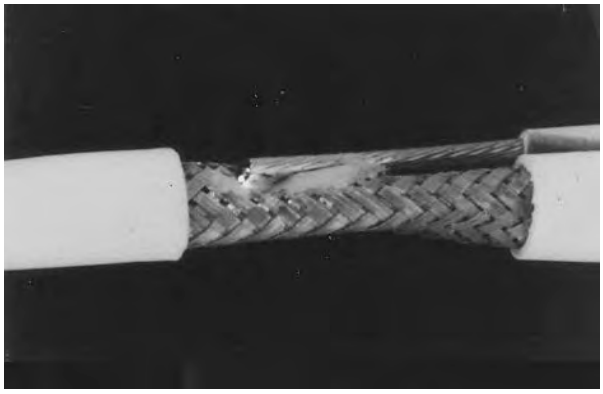
E.8 Soldered wire to shielded cable interconnections



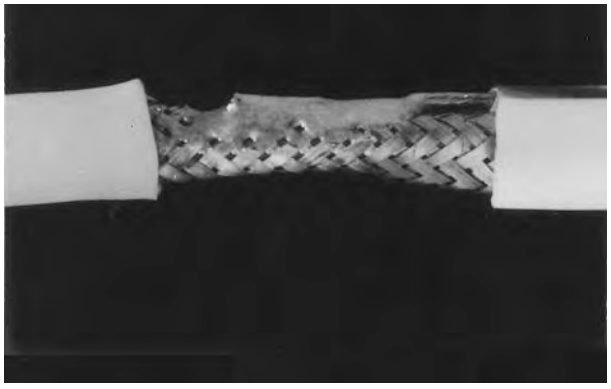
Unacceptable
Insufficient solder



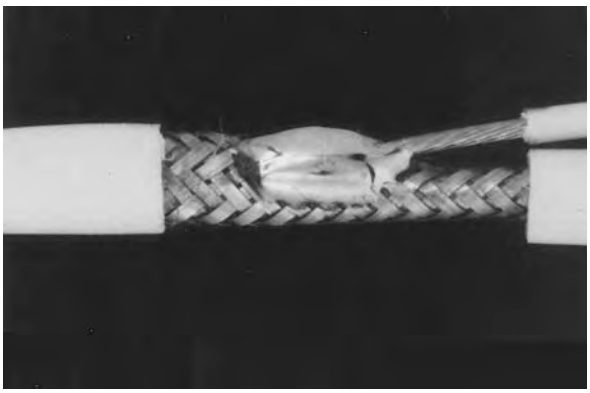
Acceptable
Minimum solder



Preferred solder

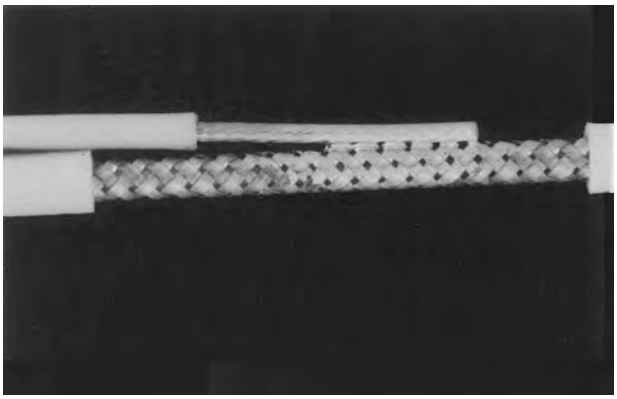


Acceptable
Maximum solder

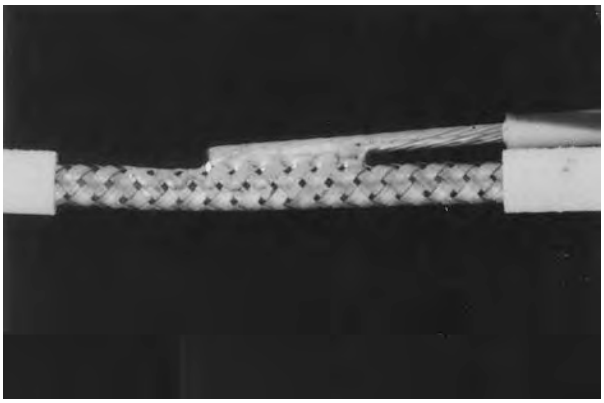


Unacceptable
Excessive solder

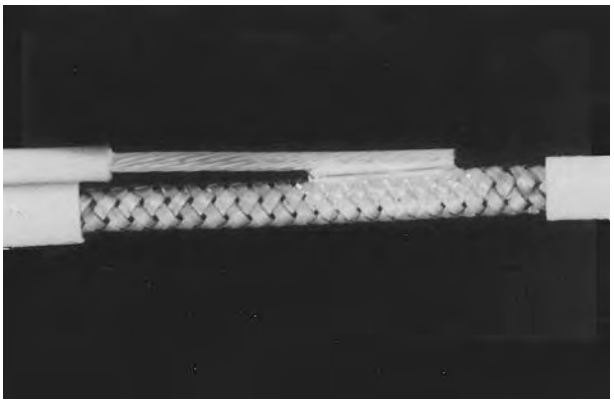
Figure E-8: Hand-soldered wire to shielded cable interconnections



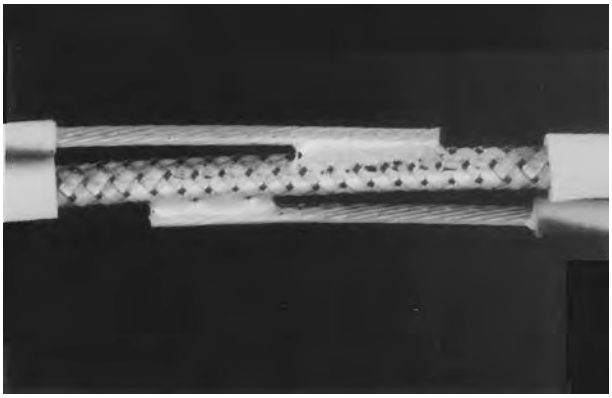
Unacceptable
Insufficient solder
Insulation overlap too great



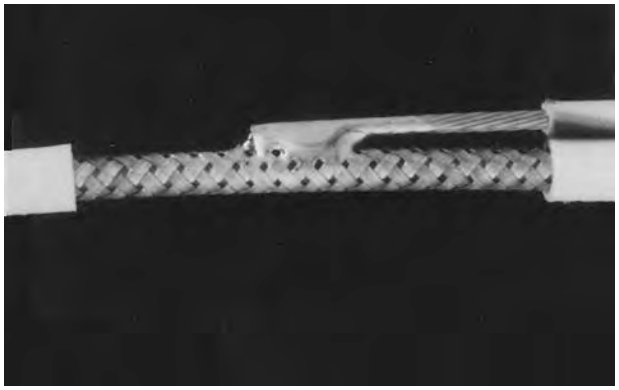
Acceptable
Minimum solder
Maximum overlap



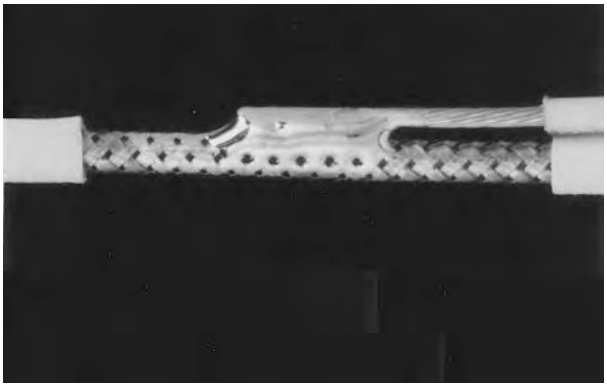
Preferred solder



Preferred solder

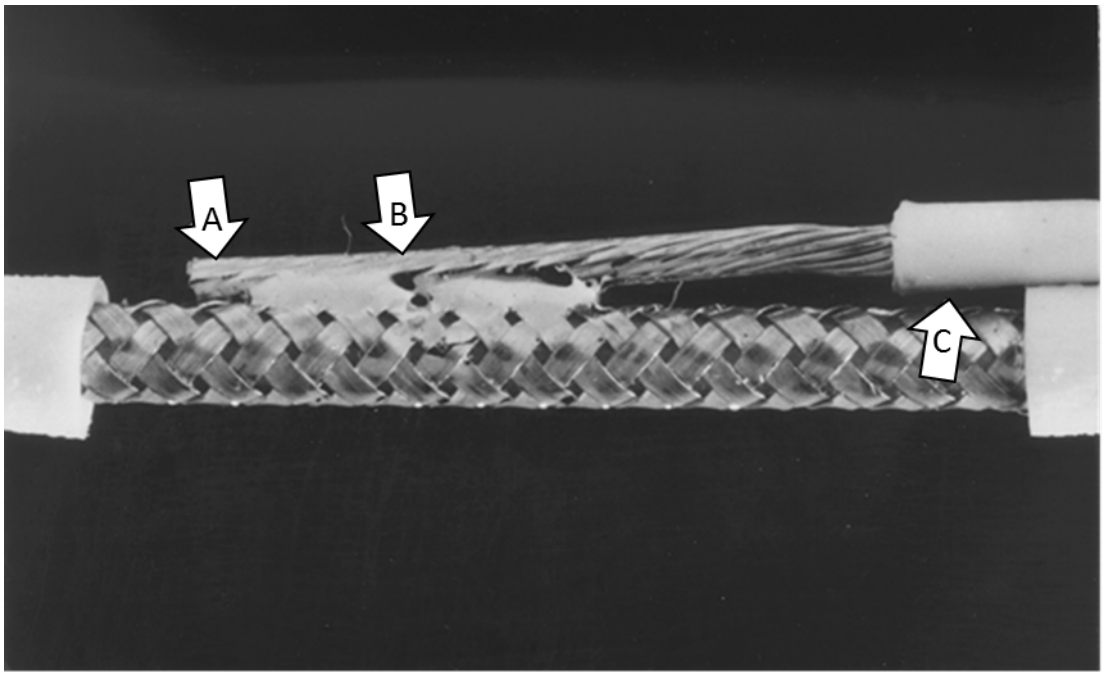


Acceptable
Maximum solder

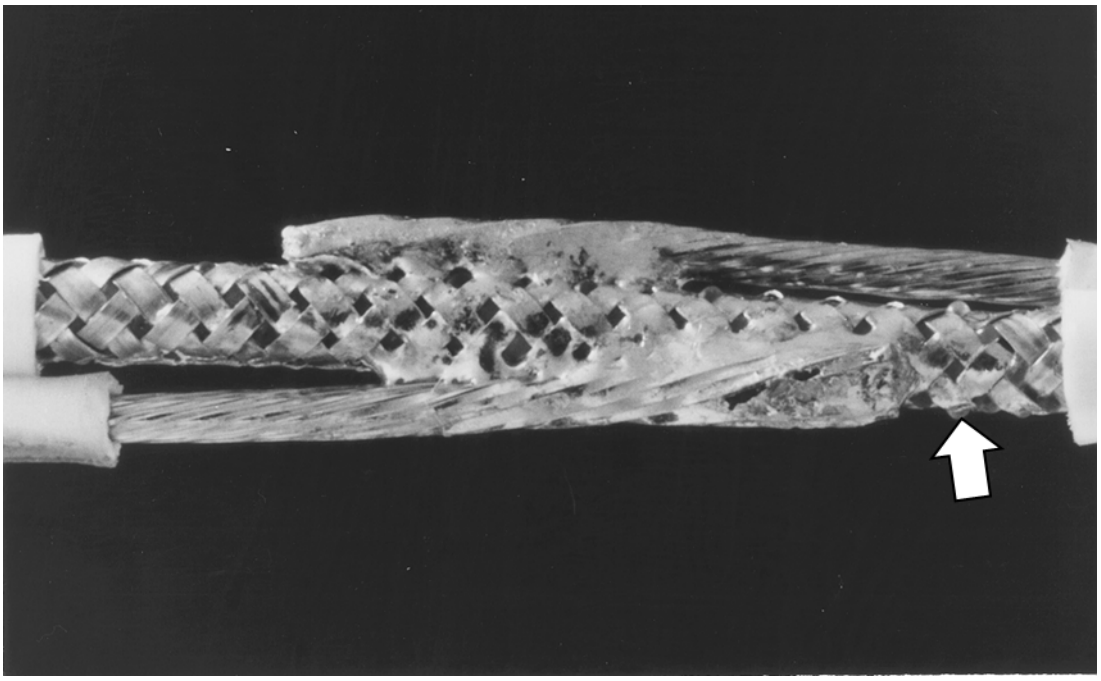


Unacceptable
Excessive solder

Figure E-9: Hand-soldered wire to shielded wire interconnections



A = Acceptable maximum insulation overlap
B = Acceptable pit in solder fillet caused by weave of shield material
C = Unacceptable lack of solder between conductors



Unacceptable
Unacceptable molten dielectric insulation
Unclean connection (flux)

Figure E-10: Hand-soldered wire interconnections - details of defects

Annex F (informative)
Visual and X-ray workmanship standards for SMDs

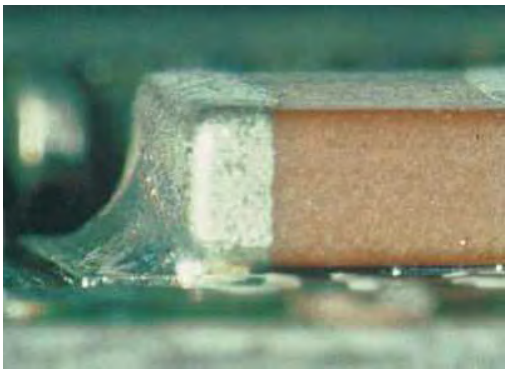
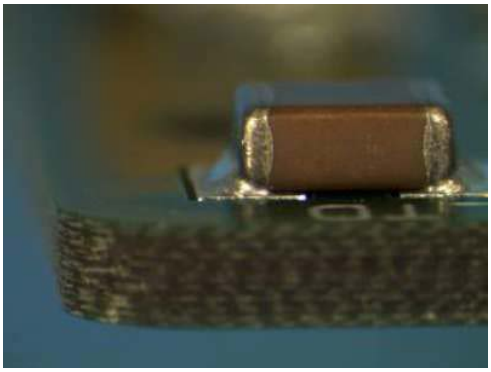
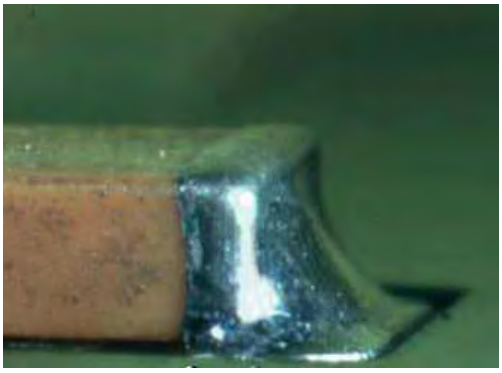
F.1 Workmanship illustrations for standard SMDs

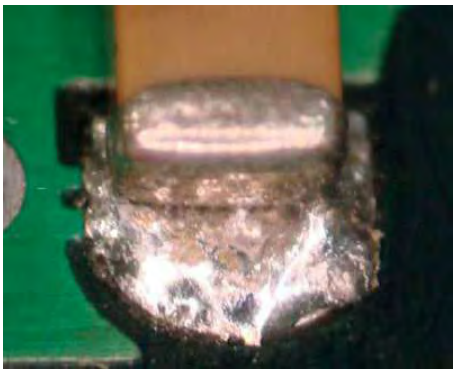
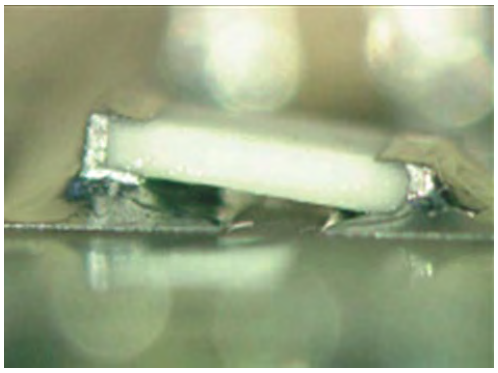
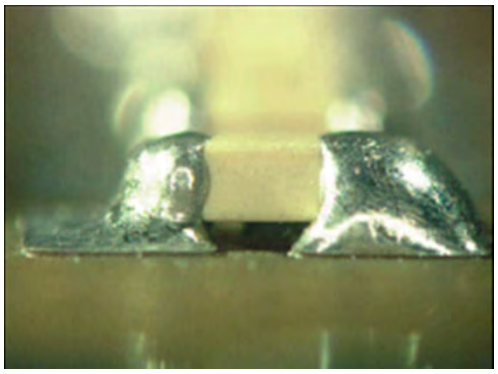
F.1.1 SMD Component type classification

Component type	Classification
Rectangular and square end-capped or end-metallized component with rectangular body	Leadless chip
Cylindrical and square end-capped components with cylindrical body	Leadless chip
Bottom terminated chip component	Leadless
Castellated chip carrier component	Leadless
Flat pack and Gull-wing leaded component with round, rectangular, ribbon leads	Leaded
Moulded magnetics	Leaded
"J" leaded component	Leaded
Area array components	AAD
Components with ribbon terminals without stress relief (flat lug leads)	Leaded
Component with Inward formed L-shaped leads	Leaded
Stacked modules components with leads protruding vertically from bottom	Leaded
Leaded component with plane termination	Leaded

F.1.2 Rectangular and square end-capped or end-metallized component with rectangular body

The following photos are provided as support material to the figures given in clause 10.5.2.1.

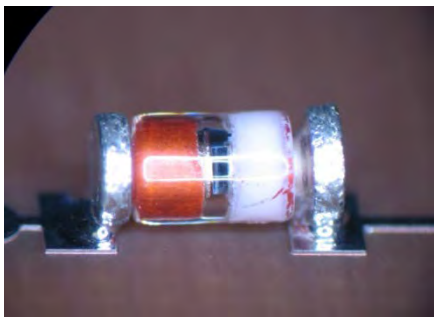
Criteria	Component	Picture
Preferred	Chip capacitor	
Acceptable (min)	Chip capacitor	
Acceptable (max)	Chip capacitor	

Criteria	Component	Picture	Comment
Unacceptable	Chip capacitor		Poor wetting
	Chip resistor		Excessive tilt
	Chip capacitor		Tombstone effect
	Chip capacitor		Excessive solder joint

F.1.3 Cylindrical and square end-capped components with cylindrical body

The following photos are provided as support material to the figures given in clause 10.5.3.

Criteria	Component	Picture
Preferred	MELF	
Acceptable (min)	MELF	No photo available at this time
Acceptable (max)	MELF	

Criteria	Component	Picture	Comment
Unacceptable	MELF		Insufficient solder joint
	MELF		Excessive overhang

F.1.4 Bottom terminated chip component

The following photos are provided as support material to the figures given in clause 10.5.4.

Criteria	Component	Picture
Preferred		No photo available at this time
Acceptable (min)		No photo available at this time
Acceptable (max)		No photo available at this time

Criteria	Component	Picture	Comment
Unacceptable		No photo available at this time	
		No photo available at this time	
		No photo available at this time	
		No photo available at this time	

F.1.5 Component with Inward formed L-shaped leads

The following photos are provided as support material to the figures given in clause 10.5.5.

Criteria	Component	Picture
Preferred	Tantalum capacitor	
Acceptable (min)		No photo available at this time
Acceptable (max)		No photo available at this time

Criteria	Component	Picture	Comment
Unacceptable		No photo available at this time	
		No photo available at this time	
		No photo available at this time	
		No photo available at this time	

F.1.6 Leadless component with plane termination

The following photos are provided as support material to the figures given in clause 10.5.6.

Criteria	Component	Picture
Preferred		No photo available at this time
Acceptable (min)		No photo available at this time
Acceptable (max)		No photo available at this time

Criteria	Component	Picture	Comment
Unacceptable		No photo available at this time	
		No photo available at this time	
		No photo available at this time	
		No photo available at this time	

F.1.7 Leaded component with plane termination

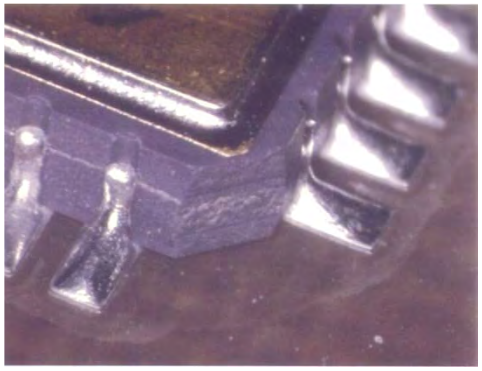
The following photos are provided as support material to the figures given in clause 10.5.7.

Criteria	Component	Picture
Preferred		No photo available at this time
Acceptable (min)		No photo available at this time
Acceptable (max)		No photo available at this time

Criteria	Component	Picture	Comment
Unacceptable		No photo available at this time	
		No photo available at this time	
		No photo available at this time	
		No photo available at this time	

F.1.8 Castellated chip carrier component

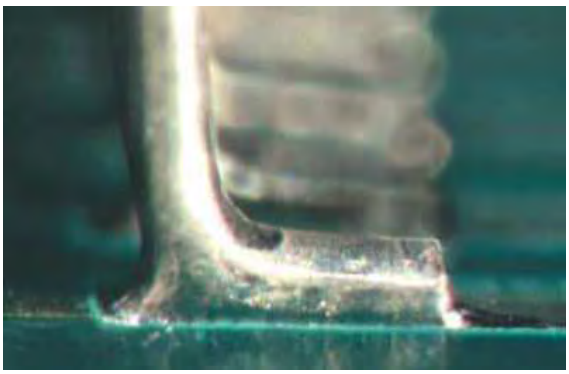
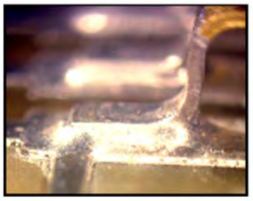
The following photos are provided as support material to the figures given in clause 10.5.8.

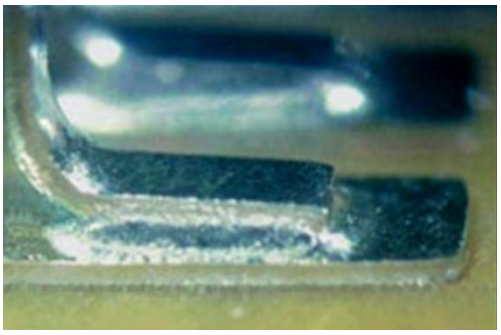
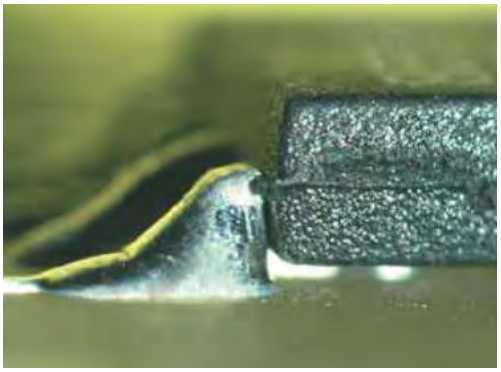
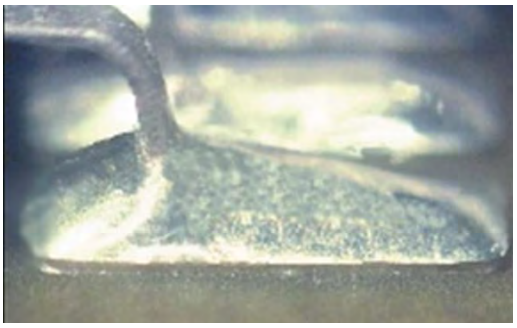
Criteria	Component	Picture
Preferred		No photo available at this time
Acceptable (min)		No photo available at this time
Acceptable (max)		

Criteria	Component	Picture	Comment
Unacceptable		No photo available at this time	
		No photo available at this time	
		No photo available at this time	
		No photo available at this time	

F.1.9 Flat pack and Gull-wing leaded component with round, rectangular, ribbon leads

The following photos are provided as support material to the figures given in clause 10.5.9.

Criteria	Component	Picture
Preferred		
Acceptable (min)	SO?	
Acceptable (max)		 

Criteria	Component	Picture	Comment
Unacceptable	SO?		Insufficient heel fillet
	SO		Excessive solder
	SO		Excessive solder

F.1.10 Moulded magnetics

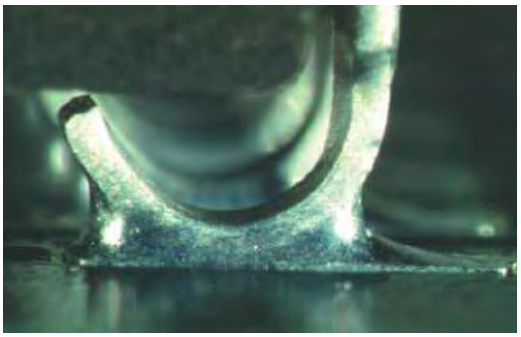
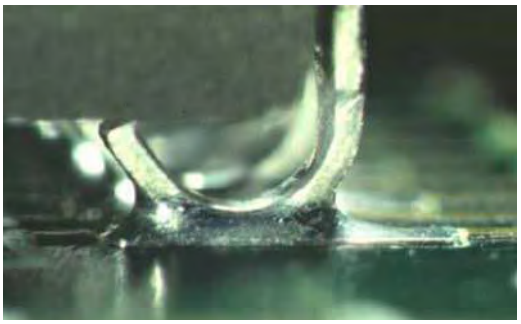
The following photos are provided as support material to the figures given in clause 10.5.9.

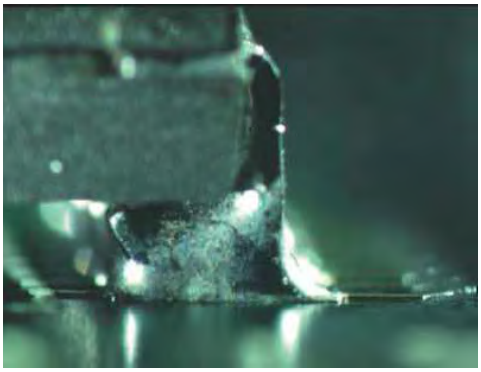
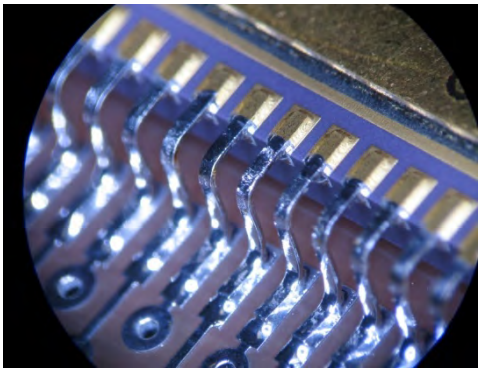
Criteria	Component	Picture
Preferred		No photo available at this time
Acceptable (min)		No photo available at this time
Acceptable (max)		No photo available at this time

Criteria	Component	Picture	Comment
		No photo available at this time	
		No photo available at this time	
		No photo available at this time	

F.1.11 "J" leaded component

The following photos are provided as support material to the figures given in clause 10.5.10.

Criteria	Component	Picture
Preferred		
Acceptable (min)		
Acceptable (max)		

Criteria	Component	Picture	Comment
Unacceptable			Excessive solder joint
			Excessive degolding

F.1.12 Components with ribbon terminals without stress relief (flat lug leads)

The following photos are provided as support material to the figures given in clause 10.5.11.

Criteria	Component	Picture
Preferred		No photo available at this time
Acceptable (min)		No photo available at this time
Acceptable (max)		No photo available at this time

Criteria	Component	Picture	Comment
Unacceptable		No photo available at this time	
		No photo available at this time	
		No photo available at this time	
		No photo available at this time	

F.1.13 Stacked modules components with leads protruding vertically from bottom

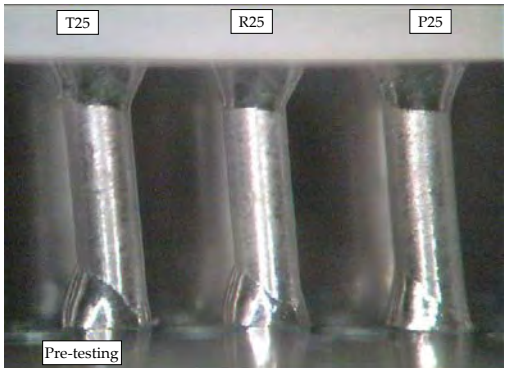
The following photos are provided as support material to the figures given in clause 10.5.12.

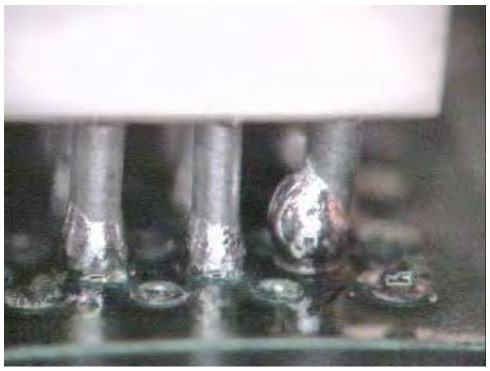
Criteria	Component	Picture
Preferred		No photo available at this time
Acceptable (min)		No photo available at this time
Acceptable (max)		No photo available at this time

Criteria	Component	Picture	Comment
Unacceptable		No photo available at this time	
		No photo available at this time	
		No photo available at this time	
		No photo available at this time	

F.1.14 Area array components

The following photos are provided as support material to the figures given in clause 10.5.13.

Criteria	Component	Picture
Preferred		No photo available at this time
Acceptable (min)		No photo available at this time
Acceptable (max)		

Criteria	Component	Picture	Comment
Unacceptable			Bent column
			

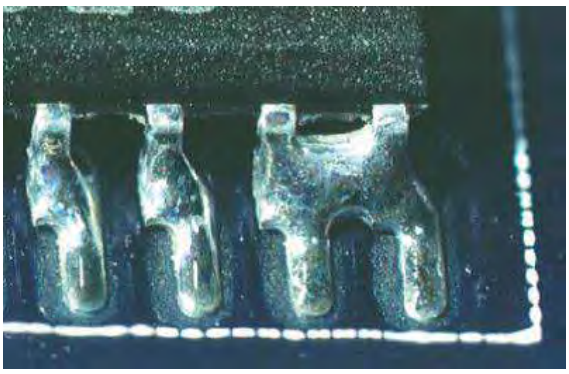
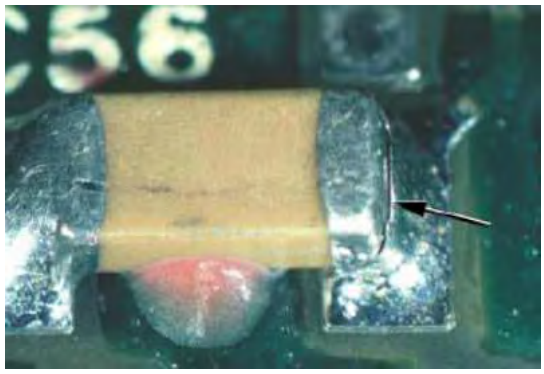
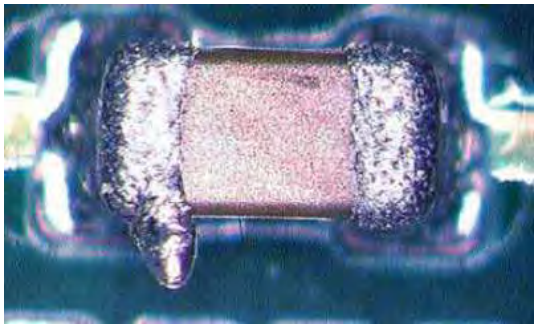
F.1.15 Leaded component with plane termination

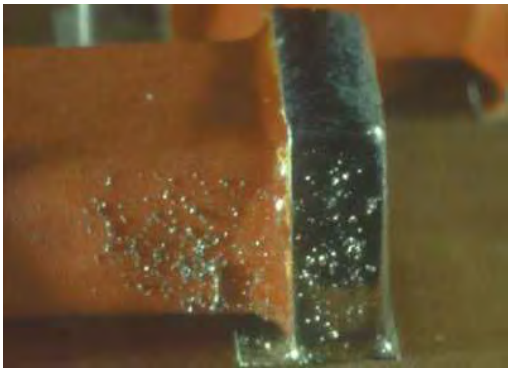
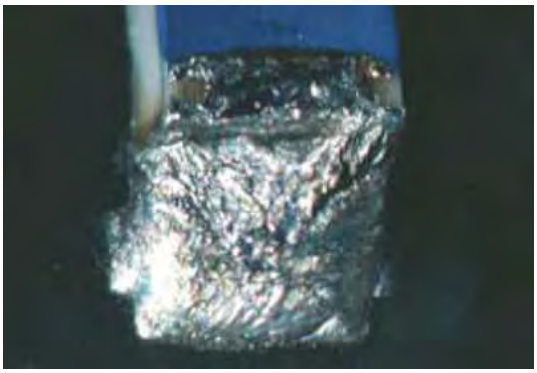
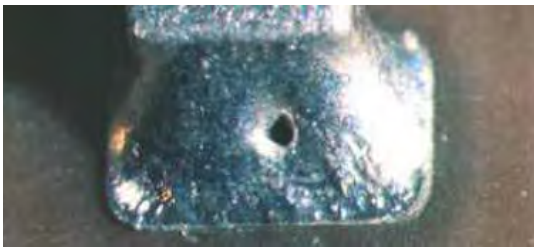
The following photos are provided as support material to the figures given in clause 10.4.

Criteria	Component	Picture
Preferred		No photo available at this time
Acceptable (min)		No photo available at this time
Acceptable (max)		No photo available at this time

Criteria	Component	Picture	Comment
Unacceptable		No photo available at this time	
		No photo available at this time	
		No photo available at this time	
		No photo available at this time	

F.1.16 Miscellaneous soldering defects

Criteria	Picture	Comment
Unacceptable		Solder bridge between terminals
		Device misplacement and solder bridge
		Misplacement and fractured solder joint
		Icicle

		Solder microballs
		Cold wetting
		Void bottom not visible

F.2 X Ray Workmanship illustrations for ball grid array devices

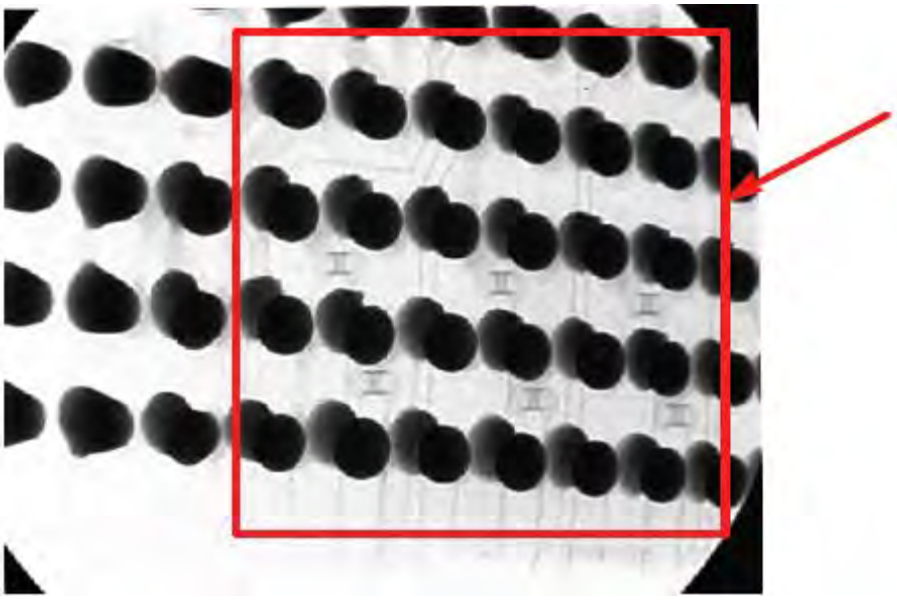
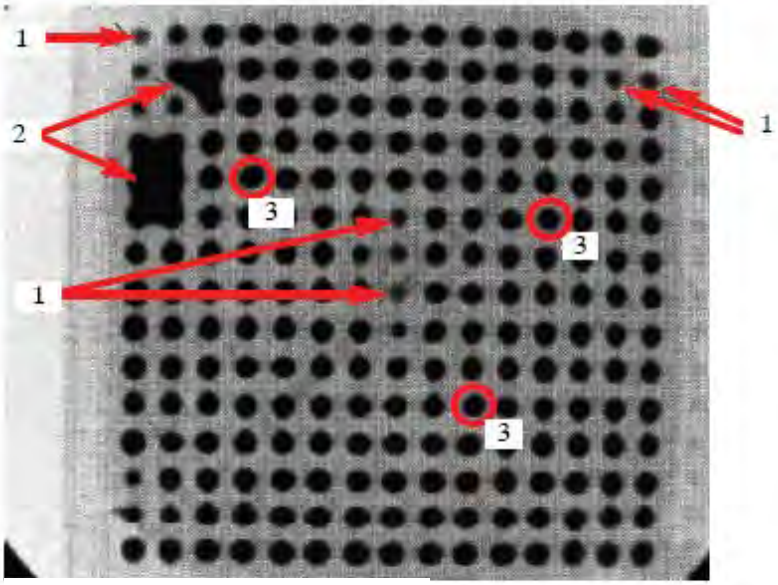
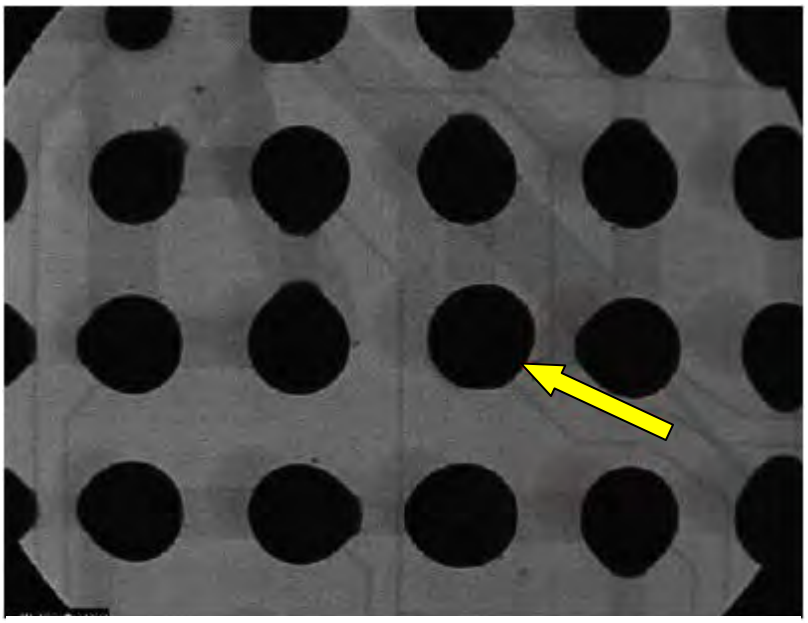


Figure F-1: Angled-transmission X-radiograph showing solder paste shadow due to partial reflow: Reject



1. missing balls: Reject
2. bridges: Reject
3. non-wetted pads: Reject

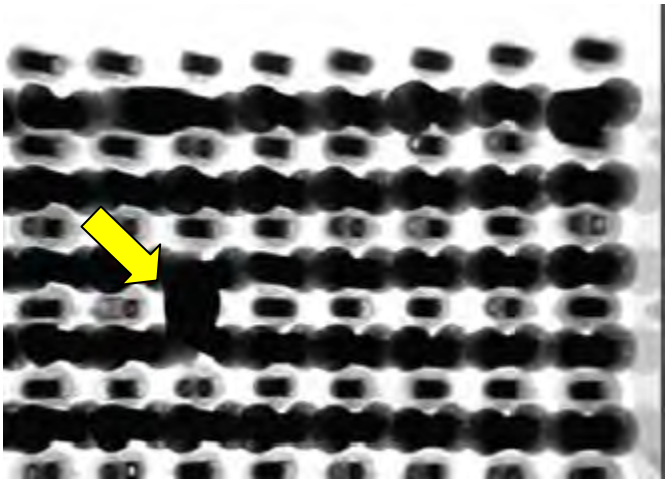
Figure F-2: Perpendicular transmission X-radiograph showing unacceptable defects



Solder has not flowed to extent of teardrop pad: Reject

Figure F-3: Perpendicular transmission X-radiograph showing non-wetted footprint

F.3 Workmanship illustrations for column grid array devices



:

Figure F-4: X-radiograph of CGA mounted on PCB showing solder bridge: Reject

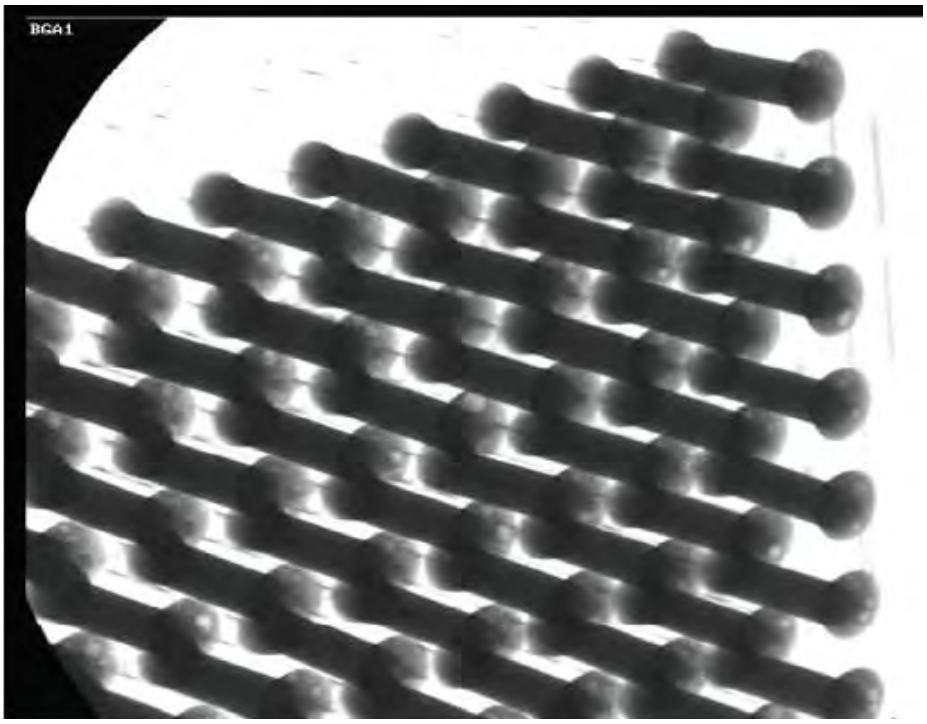


Figure F-5: X-radiograph of CGA showing solder fillets at base of columns: acceptable

Annex G (informative)
Solder Alloys melting temperatures and choice

G.1 Melting temperatures and choice

Table G-1: Guide for choice of solder type

Solder type	Melting range (°C)		Uses
	Solidus	Liquidus	
63 tin solder (eutectic)	183	183	Soldering printed circuit boards where temperature limitations are critical and in applications with an extremely short melting range. Preferred solder for surface mount components.
62 tin silver loaded	179	190	Soldering of terminations having silver metallization. This solder composition decreases the scavenging of silver surfaces.
60 tin solder	183	188	Soldering electrical wire/cable harnesses or terminal connections and for coating or pretinning metals.
96 tin silver (eutectic)	221	221	Can be used for special applications, such as soldering terminal posts.
75 indium lead	145	162	Special solder used for low temperature soldering process when soldering gold and gold-plated finishes. Can be used for cryogenic applications.
70 indium lead	165	175	For use when soldering gold and gold-plated finishes when impractical to degold.
50 indium lead	184	210	This solder has low gold leaching characteristic.

Annex H (informative)
Cross-references matrices

NOTE: The Cross-reference matrices of this standards w.r.t. H.3 ECSS-Q-ST-70-08C, ECSS-Q-ST-70-08C and ECSS-E-ST-70-38C Rev.1 will be updated before publication. They are not part of the Public Review.

H.1 ECSS-Q-ST-70-38C Rev.1 vs ECSS-Q-ST-70-61C

ECSS-Q-ST-70-38C Rev.1 (16 Sept 2017)	ECSS-Q-ST-70-61C
Change log	Change log
Introduction	Introduction
1 Scope	**1 Scope**
2 Normative references	**2 Normative references**
3 Terms, definitions and abbreviated terms	**3 Terms, definitions and abbreviated terms**
3.1 Terms from other standards	3.1 Terms from other standards
3.2 Terms specific to the present standard	3.2 Terms specific to the present standard
3.3 Abbreviated terms	3.3 Abbreviated terms
3.4 Nomenclature	3.4 Nomenclature
4 Principles of reliable soldered connections	**4.Principles of reliable soldered connections**
5 Process identification document (PID)	**16 Process identification document (PID)**
5.1 General	16.1 General
5.3 Process identification document updating	15.2 Process identification document updating
6 Preparatory conditions	**5. Preparatory conditions**
6.1 Calibration	5.1 Calibration
6.2 Facility cleanliness	5.2 Facility cleanliness
6.3 Environmental conditions	5.3 Environmental conditions
6.4 Precautions against static charges	5.5 Precautions against static discharges
6.5 Lighting requirements	5.4 Lighting requirements
6.6 Equipment and tools	5.6 Equipment and tools
6.7 Soldering machines and equipment	5.7 Soldering machines and equipment
6.8 Ancillary equipment	5.8 Ancillary equipment
7 Material selection	**6 Material selection**
7.1 General	6.1 General
7.2 Solder	6.2 Solder
7.3 Flux	6.3 Flux
7.4 Solvents	6.4 Solvents
7.5 Flexible insulation materials	6.5 Flexible insulation materials

ECSS-Q-ST-70-38C Rev.1 (16 Sept 2017)	ECSS-Q-ST-70-61C
7.6 Terminals	6.6 Terminals
7.7 Wires	6.7 Wires
7.8 Printed circuit substrates	6.9 PCBs
7.9 Components	6.10 Components
7.10 Adhesives, encapsulants and conformal coatings	11.2 Staking and bonding
	11.3 Conformal coating, potting and underfill
8 Preparation for soldering	**7 Preparations prior to mounting and soldering**
8.1 Preparation of components and terminals	7.2 Preparation of components, wires, terminals and solder cups
8.2 Preparation of solder tip	7.5 Preparation of the soldering tip
8.3 Handling	7.6 General handling
8.4 Storage	7.8 Storage
8.5 Baking of PCBs and moisture assembly sensitive components	7.7 Baking of PCB
	7.8 Baking and storage of moisture assembly sensitive components
9 Mounting of components prior to soldering	**8 Components mounting requirements prior to soldering**
9.1 General requirements	8.1 General requirements
9.2 Lead bending and cutting requirements	8.2.9 PTH Lead bending requirements
9.3 Mounting of terminals to PCBs	8.2.10 Mounting of terminals to PCBs
9.4 Lead attachment to through holes	8.2.11 Lead attachment to PCBs
9.5 Mounting of components to terminals	8.2.12 Mounting of components to terminals
9.6 Mounting of through hole connectors to PCBs	8.2.13 Mounting of through hole connectors to PCBs
9.7 Surface mount requirements	8.3 Mounting of surface mount components
10. Attachment of conductors to terminals, solder cups and cables	**9. Attachment of conductors to terminals, solder cups and cables**
11. Soldering to printed circuit boards	**10 Assembly to terminals and to PCBs**
11.1 General	10.2 General
11.5 Soldering of SMDs	10.5 Soldering of Surface Mount Components
12 Cleaning of PCB assemblies	**11.1 Cleaning of PCB assemblies**
12.1 General	11.1.1 General
12.2 Ultrasonic cleaning	11.1.2 Ultrasonic cleaning
12.3 Monitoring for cleanliness	11.1.3 Monitoring for cleanliness
13 Final inspection	**12 Final inspection**
13.1 General	12.1 General
13.2 Acceptance criteria	12.2 Acceptance criteria
13.3 Visual rejection criteria	12.3 Visual rejection criteria
13.4 X-ray rejection criterion	12.4 X-ray rejection criterion
13.5 Warp and twist of populated boards	12.5 Warp and twist of populated boards
13.6 Inspection records	12.6 Inspection records
14 Verification procedure	**13 Verification procedure**
14.1General	13.1 General
14.2 Verification by similarity	13.7 Verification by similarity
14.3 Verification programme	13.2 Verification programme
14.4 Electrical testing of components	13.4 Component verification with electrical testing procedure
14.5 Vibration and shock	14.3 Vibrations
	14.4 Mechanical shock
14.6 Temperature cycling test	14.7 Temperature cycling test
14.7 Microsection	14.9 Microsection
14.9 Special verification testing for hermetic ceramic area array packages	13.3 Special verification testing for hermetic ceramic area array packages
14.10 Verification acceptance and rejection criteria	14.9.3Verification acceptance and rejection criteria

ECSS-Q-ST-70-38C Rev.1 (16 Sept 2017)	ECSS-Q-ST-70-61C
14.11 Approval of verification	13.1.7 Approval of assembly line
14.12 Withdrawal of approval status	13.1.8 Withdrawal of approval status
14.13 Conditions for delta verification	13.6 Conditions for delta verification
14.14 Verification of cleanliness	14.2.3 Cleanliness test
15 Quality assurance	**17 Quality assurance**
15.1 General	17.1 General
15.2 Data	17.2 Data
15.3 Non-conformance	17.3 Non-conformance
15.4 Calibration	17.4 Calibration
15.5 Traceability	17.5 Traceability
15.6 Workmanship standards	17.6 Workmanship standards
15.7 Inspection	17.7 Inspection points operation
15.8 Operator and inspector training and certification	17.8 Operator and inspector training and certification
15.9 Quality records	17.9Quality records
Annex F (normative) Process Identification Document (PID) - DRD	Annex C (normative) Process Identification Documentation (PID) - DRD
Annex G (normative) Verification programme report - DRD	Annex B (normative) Verification report-DRD
Annex H (normative) SMT summary table - DRD	Annex D (normative) SMT Summary table –DRD
Annex I (informative) Visual and X-ray workmanship standards	Annex E (informative) Visual and X-ray workmanship standards for SMDs
Bibliography	Bibliography

H.2 ECSS-Q-ST-70-08C vs ECSS-Q-ST-70-61C

ECSS Q ST-70-08C (6 March 2009)	ECSS-Q-ST-70-61C
Change log	Change log
Introduction	Introduction
1 Scope	**1 Scope**
2 Normative references	**2 Normative references**
3 Terms, definitions and abbreviated terms	**3 Terms, definitions and abbreviated terms**
3.1 Terms from other standards	3.1 Terms from other standards
3.2 Terms specific to the present standard	3.2 Terms specific to the present standard
3.3 Abbreviated terms	3.3sAbbreviated terms
4 Principles of reliable soldered connections	**4 Principles of reliable soldered connections**
5 Preparatory conditions	**5. Preparatory conditions**
5.1 Calibration	5.1 Calibration
5.2 Facility cleanliness	5.2 Facility cleanliness
5.3 Environmental conditions	5.3 Environmental conditions
5.4 Lighting requirements	5.4 Lighting requirements
5.5 Precautions against static discharges	5.5 Precautions against static discharges
5.6 Equipment and tools	5.6 Equipment and tools
6 Materials selection	**6 Material selection**
6.1 General	6.1 General
6.2 Solder	6.2 Solder
6.3 Flux	6.3 Flux
6.4 Solvents	6.4 Solvents
6.5 Flexible insulation materials	6.5 Flexible insulation materials
6.6 Terminals	6.6 Terminals

ECSS Q ST-70-08C (6 March 2009)	ECSS-Q-ST-70-61C
6.7 Wires	6.7 Wires
6.8 PCBs	6.9 PCBs
6.9 Component lead finishes	6.10.2 Components lead finishes
6.10 Adhesives (staking compounds and heat sinking), encapsulants and conformal coatings	6.11 Adhesives, pottings and conformal coatings
7 Preparation for soldering	**7 Preparations prior to mounting and soldering**
7.1 General	7.1 General
7.2 Preparation of conductors, terminals and solder cups	7.2 Preparation of components, wires, terminals and solder cups
7.3 Preparation of the soldering tip	7.5 Preparation of the soldering tip
7.4 Maintenance of resistance-type soldering electrodes	7.6 Maintenance of resistance-type soldering electrodes
7.5 Handling (work station)	7.7 General handling
7.6 Storage (work station)	7.8 Storage
7.7 Preparation of PCBs for soldering	
8 Mounting of components	**8 Components mounting requirements prior to soldering**
8.1 General requirements	8.1 General requirements
8.2 Lead bending requirements	8.2.14 Lead bending requirements
8.3 Mounting of terminals to PCBs	8.2.15 Mounting of terminals to PCBs
8.4 Lead attachment to PCBs	8.2.16 Lead attachment to PCBs
8.6 Mounting of connectors to PCBs	8.2.18 Mounting of through hole connectors to PCBs
9 Attachment of conductors to terminals, solder cups and cables	**9 Attachment of conductors to terminals, solder cups and cables**
9.1 General	9.1 General
9.2 Wire termination	9.2 Wire termination
9.3 Turret and straight-pin terminals	9.3 Turret and straight-pin terminals
9.4 Bifurcated terminals	9.4 Bifurcated terminals
9.5 Hook terminals	9.5 Hook terminals
9.6 Pierced terminals	9.6 Pierced terminals
9.7 Solder cups (connector type)	9.7 Solder cups (connector type)
9.8 Insulation sleeving	9.8 Insulation sleeving
9.9 Wire and cable interconnections	9.9 Wire and cable interconnections
9.10 Connection of stranded wires to PCBs	9.10 Connection of stranded wires to PCBs
10 Soldering to terminals and PCBs	**10 Soldering to terminals and PCBs**
10.1 General	10.1 General
10.2 Solder application to terminals	10.2.1 Solder applications to terminals
10.3 Solder application to PCBs	10.2.4 Solder application to PCBs
10.4 Wicking	10.2.5 Wicking
10.5 Solder rework	10.2.6 Solder rework
10.6 Repair and modification	10.2.7 Repair and modification
11 Cleaning of PCB assemblies	**11 Cleaning of PCB assemblies**
11.1 General	11.1 General
11.2 Ultrasonic cleaning	11.2 Ultrasonic cleaning
11.3 Monitoring for cleanliness	11.3 Monitoring for cleanliness
12 Final inspection	**12 Final inspection**
12.1 General	12.1 General

ECSS Q ST-70-08C (6 March 2009)	ECSS-Q-ST-70-61C
12.2 Acceptance criteria	12.2 Acceptance criteria
12.3 Visual rejection criteria	12.3 Visual rejection criteria
13 Verification procedure	**13 Verification procedure**
13.1 General	13.1 General
13.2 Vibration	
13.3 Temperature cycling	
13.4 Microsection	
14 Quality assurance	**15 Quality assurance**
14.1 General	15.1 General
14.2 Data	15.2 Data
14.3 Nonconformance	15.3 Nonconformance
14.4 Calibration	15.4 Calibration
14.5 Traceability	15.5 Traceability
14.6 Workmanship standards	15.6 Workmanship standards
14.7 Inspection	15.7 Inspection
14.8 Operator and inspector training and certification	15.8 Operator and inspector training and certification
15 Workmanship standards	**Annex E (informative) Visual workmanship standards for manual soldering**
15.1 Soldered clinched terminals	
15.2 Soldered stud terminals	
15.3 Soldered turret terminals	
15.4 Solder turret terminals	
15.5 Soldered bifurcated terminals	
15.6 Soldered hook terminals	
15.7 Soldered cup terminals	
15.8 Soldered wire to shielded cable interconnections	
Annex A (normative) Report on manual soldering of high-reliability electrical connections - DRD	Annex A (normative) Verification programme report-DRD
Annex B (informative) Solder melting temperatures and choice	Annex G (informative) Solder alloys melting temperatures and choice
Bibliography	Bibliography

H.3 ECSS-Q-ST-70-07C vs ECSS-Q-ST-70-61

ECSS-Q-ST-70-07C (16 April 2010)	ECSS-Q-ST-70-61C
Change log	Change log
Introduction	Introduction
1 Scope	**1 Scope**
2 Normative references	**2 Normative references**
3 Terms, definitions and abbreviated terms	**3 Terms, definitions and abbreviated terms**
3.1 Terms from other standards	3.1 Terms from other standards
3.2 Terms specific to the present standard	3.2 Terms specific to the present standard
3.3 Abbreviated terms	3.3 Abbreviated terms

ECSS-Q-ST-70-07C (16 April 2010)	ECSS-Q-ST-70-61C
4 Principles	**4 Principles of reliable soldered connections**
5 Requirements	13.2.3 Additional verification for wave soldering
5.1 General	
5.1.1 PCB design constraints	
5.1.2 Rework	
5.2 Request for verification of the automatic wave soldering process	13.1.1 Request for verification
5.2.1 General	
5.2.2 Technology samples	13.1.2 Technology sample
5.2.3 Examination	13.1.2.2Evaluation of technology sample
5.3 Line audit	13.1.3 Audit of assembly line
5.4 Verification	13.2 Verification programme
5.4.1 Planning, management and finance	deleted
5.4.2 Description of samples	13.1.2.1 Description off technology sample
5.4.3 Initial tests	14.2 Initial tests
5.4.4 Environmental exposure	14.3 Vibration
	14.4 Mechanical shock
	14.7 Temperature cycling test
5.4.5 Final tests	14.8 Final tests
5.4.6 Final verification report	Annex B (normative) Verification report
5.5 Approval	13.1.7 Approval of assembly line
5.5.1 Notification	
5.5.2 Renewal of approval	
5.5.3 Withdrawal of approval	13.1.8 Withdrawal of approval
5.5.4 Approval for future project	13.1.7 Approval of assembly line
5.6 Process requirements for wave soldering of printed circuit boards	5.5 Precaution against static discharges
	5.6.12 Dynamic wave-solder machines
	6 Material selection
Annex A (normative) Solder joint discrepancy log – DRD	Superseded by 14.11 Soldering log
Annex B (normative) Request for verification of the automatic wave soldering process - DRD	Annex A(normative) Verification programme - DRD
Annex C (normative) Automatic wave soldering process verification report – DRD	Annex B (normative) Verification programme report-DRD
Annex D (normative) Machine-soldering logbook – DRD	Superseded by 14.11 Soldering log
Annex E (normative) Wave soldering process identification document (PID) – DRD	Annex C (normative) Process Identification Documentation (PID) - DRD
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ECSS-E-HB-32-25	Space engineering - Mechanical shock design and verification handbook
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EN-IEC 61190-1-2	Attachment materials for electronic assembly - Part 1-2: Requirements for soldering pastes for high-quality interconnects in electronics assembly
EN-IEC 61190-1-3	Attachment materials for electronic assembly - Part 1-3: Requirements for electronic grade solder alloys and fluxed and non-fluxed solid solders for electronic soldering applications
EN-IEC 61340-5-2	Electrostatics - Part 5-2: Protection of electronic devices from electrostatic phenomena – User guide
ESA STM-275	Evaluation of cleanliness test methods for spacecraft PCB assemblies
MIL-PRF-28861	FILTERS: Filters, Radio Interference/Electromagnetic Interference Suppression
MIL-PRF-39003	CAPACITORS: Fixed, Tantalum, Electrolytic (Solid Electrolyte), Polarized, Established Reliability
MIL-PRF-39010	COILS: Coils, Fixed, Radio Frequency, Established Reliability
MIL-PRF-49470	CAPACITORS: Fixed, Ceramic Dielectric, Switch Mode Power Supply
MIL-PRF-83421	CAPACITORS: Fixed, Metallized, Plastic Film Dielectric, Hermetically Sealed, Established Reliability