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# Capability approval programme for hermetic thin-film hybrid microcircuits

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# ABSTRACT

This specification defines the general requirements for capability approval of a manufacturing line for hermetic thin-film hybrid microcircuits.

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# SECTION 1: SCOPE

This specification defines the general requirements for capability approval of a manufacturing line for hermetic thin-film hybrid microcircuits. For procurement requirements, see ESA PSS-01-608. ESA approval mandate will be exercised upon conclusion of the evaluation phase and at the end of the programme. Before the evaluation phase can commence, the manufacturer shall define the capability approval domain by specifying the processes, materials and techniques involved in the technology for which approval is sought.

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# SECTION 2: GENERAL

## 2.1 INTRODUCTION

The manufacturer shall have and implement a quality and reliability programme compatible with this specification. The review of this programme by ESA is part of the capability approval. The manufacturer shall be responsible for the performance of tests and inspections required by this specification. All of these tests and inspections shall be performed at the plant of the manufacturer and be approved by the manufacturer's quality assurance organisation. The use of external facilities and/or services is subject to prior ESA approval.

ESA, or its designated representative, reserves the right to participate in, or execute, surveys, audits, reviews and source inspections as well as to witness any tests and to have resident or temporary personnel at the manufacturer's plant during the programme period. Participation by ESA, or its designated representative, in any approval activities shall never be considered as substitution for, or release from, the manufacturer's responsibilities. The manufacturer shall grant personnel of ESA, and/or of its designated representative, free access to any documentation, hardware and facilities listed in the Process Identification Document (PID).

## 2.2 Applicable Documents

The following documents are applicable to the extent specified herein.

### 2.2.1 ESA

| | |
|---|---|
| ESA PSS-01-60 | Component selection, procurement and control for ESA space systems |
| ESA PSS-01-70 | Materials and process selection and quality control for ESA space systems |
| ESA PSS-01-201 | Contamination and cleanliness control |
| ESA PSS-01-608 | Generic specification for hybrid microcircuits |
| ESA PSS-01-702 | A thermal vacuum test for the screening of space materials |
| ESA PSS-01-708 | The manual soldering of high-reliability electrical connections |

| | |
|---|---|
| ESA PSS-01-722 | The control of limited life materials |

### 2.2.2 Others

| | |
|---|---|
| FED-STD-209 | Clean room and workstation requirements,controlled environment |
| MIL-STD-202 | Test methods for electronic and electrical component parts |
| MIL-STD-883 | Test methods and procedures for microelectronics |
| MIL-STD-38510 | Microcircuits, general specification for |
| QRC-05C | Checklist for thin-film hybrid microcircuit manufacturers and line survey |

## 2.3 REFERENCE DOCUMENTS

Not applicable.

## 2.4 DEFINITIONS

The definitions listed in the Annex shall apply.

## 2.5 ACCESS TO MANUFACTURING FACILITIES

To enable the survey team of ESA, or its delegated representative, to carry out the capability survey and line survey, the manufacturer shall grant free access to the facilities concerned. He shall also enable the team to witness any development, engineering, production and quality assurance operations involved in the processes for which approval is sought.

### 2.5.1 Checklist

To facilitate the evaluation procedure, ESA will apply Checklist ESA QRC-05C.

## 2.6 CAPABILITY SURVEY

The purpose of this survey is to assess the following aspects of the manufacturer's organisation:

(a) General organisation and management;
(b) Quality and reliability assurance organisation, including definition of authority and effectiveness;
(c) Facilities and capabilities of the plant in which the thin-film hybrid microcircuits will be manufactured and tested;
(d) Nonconformance control.

Before and/or during the actual survey, the manufacturer shall provide ESA with any documentation which may assist the survey team in the execution of its tasks. As a minimum, this documentation shall include:

- An organigram delineating authority, responsibility and interrelationship between Engineering, Production, Quality and Reliability Assurance, Procurement and Management;
- Expertise of all key personnel employed in the Production and Product Assurance Departments;
- A list of contracts with ESA and/or national space agencies for component evaluation and qualification;
- The name(s) and location(s) of any other plant(s) of the manufacturer where electronic parts are produced according to the same technology (or a similar one) as that applied to the hybrid microcircuits for which qualification is sought;
- A flow-chart and any available procedures relative to the processes and controls applied in the production of the devices to be evaluated and approved.

### 2.6.1 Organisation and Management

The manufacturer shall clearly define his policy on:

- Authority and responsibility of quality and reliability management vis-à-vis general management;
- Support requested by the research and development department from engineering and/or quality assurance personnel;
- Employee motivation (bonus scheme, incentives, operator training and certification etc.).

### 2.6.2 Assessment of Design Rules

For assessment of the design of the hermetic thin-film hybrid microcircuits, the manufacturer shall provide ESA with the design rules he proposes to apply. General design guidelines are under consideration.

## 2.7 PRODUCT ASSURANCE REQUIREMENTS

### 2.7.1 Organisation and Responsibilities

The manufacturer shall have an effective quality and reliability organisation, suitable facilities and competent product assurance personnel with a sufficient degree of independence from the company's design and manufacturing functions to deal objectively with the product assurance aspects of the hybrid microcircuits in compliance with the applicable ESA documents.

The quality and reliability organisation shall have direct and unimpeded access to higher management, to which it shall report regularly on the status and adequacy of the programme.

The quality assurance organisation shall be responsible for the implementation of all requirements of this specification and the execution of this programme to the satisfaction of the customer. He shall present to the consumer only those items/documents which he determines to be in full compliance with those requirements of this and all applicable specifications listed that concern the customer.

### 2.7.2 Quality and Reliability Requirements

The manufacturer shall establish and implement a quality and reliability programme that fully complies with all the applicable ESA PSS specifications. Special attention shall be paid to:

- Training of operators/inspectors;
- Definition of workmanship standards;
- Reliability engineering activities;
- Configuration control;
- Quality asurance activities according to PSS-01-20;
- Materials and process selection according to PSS-01-70 and PSS-01-716.

## 2.8 LAY-OUT OF FACILITIES

The manufacturer shall provide ESA with the lay-out of the facilities to be surveyed, showing the location of each production area, the cleanliness standards and dust count frequency applicable to each area and operation, and including a list of equipment, specifying its accuracy and calibration frequency.

## 2.9 LINE SURVEY

During this survey, which will comprise all aspects of the production line, special attention will be paid to those processes, process steps, materials, piece parts and controls that are involved in the manufacture of the devices concerned. The manufacturer shall demonstrate to ESA the methods evolved on the basis of in-house experience for investigation and optimisation of all processes for which approval is sought.

For the purpose of this survey, the subject test structures will be divided according to the major processes performed in the three main production areas of a hybrid microcircuit manufacturing facility, viz.:

**(a) Thin Film Network**
The pure thin-film circuit requires basically the film deposition and the etching technique, resistor trimming, without additions or encapsulation.

**(b) Thin Film Hybrid Assembly**
This involves the adding-on of chips or other circuits and their connection to the substrate.

**(c) Encapsulation or Mounting of Microcircuit**
This involves the encapsulation of the substrate or its mounting onto a base-plate or similar structure.

NOTE: In certain cases, mounting may be considered as part of assembly (b).

### 2.9.1 Production Documents

All documents related to the processes for which capability approval is sought shall be made available to ESA. Any proprietary documents shall be included, but shall be marked as such.

### 2.9.2 Process Flow-chart

This chart shall show the sequence of production and inspection steps. Inspections shall include each measurement, test or visual examination performed. The flow-chart shall also show:

- number, issue and revision date of the specification applicable to each production and inspection step;
- department, division or section responsible for each operation involved in the processing, production and quality control;
- point at which statistical control records are applied. The issue and revision date of the above-mentioned documents may be listed separately.

### 2.9.3 Travelling Documents

The manufacturer shall prepare and use a travelling document for each lot. This document shall show as a minimum:

- a lot identification;
- operation;
- date of each operation;
- number in/out at each operation;
- operator identification;
- nonconformance references.

### 2.9.4 Process Control Chart

The process control chart shall show as a minimum:

- title of relevant process;
- name or code number of station at which it is used;
- lot identification;
- dates recorded;
- number of items inspected;
- identification of equipment adjustment;
- percentage of defective devices;
- average nominal values;
- average limits.

### 2.9.5 Process Documentation

The manufacturer shall prepare and maintain documents for incoming inspection, production, quality assurance and process control such as specifications and procedures establishing:

- materials and piece parts;
- operations;
- equipment;
- calibration methods;
- measurements;
- tests;
- inspections;
- tolerances.

These documents and any revisions thereof shall be available at all times to operating personnel and, upon request, shown to the evaluating and qualifying authority.

### 2.9.6 Traceability

The manufacturer shall record the manufacturing data and material history of all units processed according to this specification and maintain these records for a minimum of five years.

## 2.10 LOCATION OF PROCESSING AREAS

The manufacturer shall specify the location where each of the key processing steps is performed. The evaluating authority shall be notified of any changes in these locations so that he may determine whether re-evaluation is required.

## 2.11 WORK AREAS

### 2.11.1 General Requirements

The subject devices shall be produced in a controlled area. This implies that:

- only authorised personnel shall have access to such an area and that within such an area:
- personnel shall wear protective clothing;
- smoking, drinking and eating shall be prohibited;
- housekeeping shall be according to a written schedule;
- equipment shall be compatible with the cleanliness standard required in the controlled area.

### 2.11.2 Environmental Control

The manufacturer shall specify for each process step:

- relative humidity;
- particle count.

He shall demonstrate the manner in which these conditions are controlled, taking into account the relevant requirements defined in Table 1 and Specification ESA PSS-01-201.

## 2.12 HANDLING OF SUBSTRATES

The manufacturer shall furnish evidence that adequate provisions are in force for the careful handling and storage of substrates throughout the production cycle. Any damage to substrates shall be recorded together with details of the station and/or stage of operation at which the damage occurred.

## 2.13 PURITY OF MATERIALS

The manufacturer shall keep records to verify that the materials used in production are of a consistent purity level and meet the application requirements.

**TABLE 1: ENVIRONMENTAL REQUIREMENTS**

| Process step | Cleanliness class | Humidity (% RH) | Temperature (°C) |
|---|---|---|---|
| Cutting of masters (if used). | 100 000 | 50 ± 5 | To be specified by manufacturer |
| Photoreduction, plotting and manufacture of production masks. | 100 | 50 ± 5 | ditto |
| Photoresist preparation, application, drying, including pattern exposure and development processes. | 100 | 50 ± 5 | ditto |
| Etching and cleaning processes. | 100 | 50 ± 5 | ditto |
| Attachment of encapsulated or unencapsulated passive components and encapsulated semiconductor components. Attachment of substrates to baseframes, plates or structures. Includes flux removal and cleaning processes. | 100 000 | To be specified by manufacturer | ditto |
| Final cleaning attachment of unencapsulated semiconductor components, mounting of substrate into hermetic package and final sealing of package. (Also includes possible burn-in, precap, visual inspection and other control processes before final sealing). | 100 | ditto | ditto |
| Mounting of component equipped structures into non-hermetic packages. Includes cleaning after mounting. | 10 000 | ditto | ditto |
| Packaging of finished product into sealed plastic bag. | 10 000 | 50 ± 5 | ditto |

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# SECTION 3: EVALUATION PHASE

## 3.1 GENERAL

The evaluation phase shall consist of:

**(a) Capability Survey**
This survey is made to assess a manufacturer's general capability in the production of reliable circuits.

**(b) Line Survey**
This survey consists of an analysis of a manufacturer's technology and production line based on applied processes and controls and a detailed study of all available test data for the identification of critical processes and controls.

**(c) Evaluation Testing**
This involves respectively the selection, production and testing of test structures for determination of their stress limits and weaknesses.

**(d) Corrective Actions**
If, as a result of evaluation testing, the test structures show weaknesses or deficiencies, the manufacturer shall take any corrective actions required by ESA.

**(e) ESA Approved Capability Domain**
After all required corrective actions have been implemented to the full satisfaction of ESA, ESA will approve the manufacturer's capability domain as defined in the PID at the end of this phase. This approval will enable the manufacturer to start the next phase of the programme.

## 3.2 EVALUATION TESTING

Evaluation testing shall comprise four sequential steps, viz.:

(a) Selection of techniques, processes and materials to be certified;

(b) Based on the selection specified under (a) above, manufacture of test structures or circuits;

(c) Testing of test structures or circuits;

(d) Evaluation of test results.

### 3.2.1 Selection of Techniques

On the basis of the processes, materials and techniques proposed by the manufacturer for approval, the manufacturer shall propose the main techniques and type of encapsulation, define the test structures and draw up the test plans in accordance with the requirements of this specification.

Tables 2 and 3 show respectively the possible main techniques and encapsulation or mounting methods.

The manufacturer shall be free to choose which of the different subtechniques applicable to a specific main technique he wishes to use. However, the lay-out and content of the corresponding test structure shall be agreed with ESA. The selection shall be made before commencing manufacture of the test structures. Table 5 lists the various subtechniques.

The manufacturer shall draw up a list of processes and select the raw materials, piece parts and added-on or applied materials, and ascertain their conformance to the design, quality and procurement requirements defined in this specification and ESA Specifications PSS-01-60, PSS-01-70 and PSS-01-608, as relevant. Alternatively, he shall prove their suitability for space application by other documentary evidence.

Each process step shall be chosen solely on the basis of the materials, techniques and controls applied at the time of evaluation. A preliminary Process Identification Document (PID) shall be prepared for the processes and procedures to be applied. The PID shall list all constituent materials and piece parts.

The manufacturer shall ensure that all materials and processes for which certification is sought are adequately covered by the programme. Prior to its implementation, this programme shall be submitted to ESA for approval.

**TABLE 2: MAIN TECHNIQUES**

| | |
|---|---|
| A | General-purpose 1-layer resistor and conductors, 0.1 W cm$^{-2}$ or less. Terminal current less than 0.5 A. |
| B | General-purpose 1-layer resistor and conductors, 0.1 W cm$^{-2}$ or less. Terminal current less than 0.5 A. Attached with components |

**TABLE 3: MOUNTING AND ENCAPSULATION**

| | |
|---|---|
| Q | Unencapsulated and unmounted substrates |
| R | Substrates mounted on simple metal-plate structure |
| S | Substrates mounted in hermetically sealed low power metal package |
| T | Substrates mounted in hermetically sealed low power ceramic package |

**TABLE 4: PERMITTED COMBINATIONS OF MAIN TECHNIQUES AND MOUNTING OR ENCAPSULATION METHODS FOR DEFINITION OF TEST STRUCTURES**

| MAIN TECHNIQUE | MOUNTING OR ENCAPSULATION | | | |
|---|---|---|---|---|
| | Q | R | S | T |
| A | QA1 and QA2 | RA1 and RA2 | SA1 and SA2 | TA1 and TA2 |
| B | QB1, QB2 and QB3 | RB1, RB2 and RB3 | SB1, SB2 and SB3 | TB1, TB2 and TB3 |

**Example**

SB1 is a type B1 test substrate (covering general purpose 1-layer thin film resistor and conductors with components attached) mounted in metal package.

Definition of Main Technique: See Table 2.

Definition of Mounting and Encapsulation Methods Q to U: See Table 3.

Definition of Test Substrates A1 to B3: See Table 6.

**TABLE 5: SUBTECHNIQUES**

| | |
|---|---|
| I | 1-layer conductor |
| II | 1-layer conductor and resistor |
| III | Protective covering |
| IV | Cross-over by wire bonding |
| V | Termination with leads |
| VI | Mounting of encapsulated components |
| VII | Mounting of resistor and capacitor chips |
| VIII | Chip and wire bonding |
| IX | Beam lead chip mounting |
| X | Substrate mounting on metal plate |
| XI | Substrate mounting in package |

### 3.2.2 Sequence of Operations for Selection, Manufacture and Testing of Test Structures

(a) The manufacturer shall propose and submit to ESA for approval those processes that he wishes to adopt.
(b) Joint agreement by ESA and the manufacturer on subtechniques (see Table 5).
(c) Joint agreement by ESA and the manufacturer on main techniques and mounting or encapsulation methods.
(d) Preparation by the manufacturer of the applicable documentation and lay-outs of test structures.
(e) Manufacture and testing of test structures; preparation of report.
(f) ESA may require that it monitor certain tests.
(g) Destructive Physical Analysis (DPA) of control devices by ESA or an independent test laboratory.

### 3.2.3 Test Structures for Line Evaluation

The test structures to be manufactured shall:

- be based on the processes selected,
- be such that they are representative of the technology involved,
- be in accordance with the controls, limits and constaints agreed between ESA and the manufacturer,
- meet the requirements of this specification,
- be tested for any weakness, so that restraints of the applied processes and technologies may be determined, and
- take into account any inherent criticalities.

### 3.2.4 Test Structures and Applicable Test Programmes

Table 6 specifies the test substrates to be used in the manufacture of the different test structures and refers to the paragraphs in which details are described.

Table 7 shows type designations and numbers of test structures to be manufactured for evaluation testing together with the applicable test plans set out in Paragraph 3.2.6.

**TABLE 6: TEST SUBSTRATES AND PROCEDURES**

| SUBSTRATE | DESCRIPTION | PARA. |
|---|---|---|
| A1 | Substrate for general-purpose 1-layer thin-film conductors | 3.2.5.1 |
| A2 | Substrate for general-purpose 1-layer thin-film resistors and conductors | 3.2.5.2 |
| B1 | Substrate for 1-layer thin-film resistors and conductors attached with components (chip and wire). Applicable subtechniques to be chosen from Table 5. | 3.2.5.3 |
| B2 | Substrate for 1-layer thin-film resistors and conductors attached (beam-lead) with components. Applicable subtechniques to be chosen from Table 5. | 3.2.5.4 |

**TABLE 7: TYPE DESIGNATIONS AND NUMBERS OF TEST STRUCTURES TO BE MANUFACTURED, AND APPLICABLE TEST PLANS**

<table>
<tr><th>DESCRIPTION</th><th>Test structure</th><th>No. of pcs.to be manuf.</th><th>Test Plan No.</th><th>Example</th></tr>
<tr><td>General-purpose 1-layer thin-film conductors, unencapsulated.</td><td>QA1</td><td>39</td><td>1</td><td rowspan="8">Mounting or package type definition see Table 3<br>↓<br>Q A2<br>↑<br>Substrate type definition see Table 6</td></tr>
<tr><td>General-purpose 1-layer thin-film resistors and conductors, unencapsulated.</td><td>QA2</td><td>39</td><td>1</td></tr>
<tr><td>General-purpose 1-layer thin-film conductors, on metal plate.</td><td>RA1</td><td>39</td><td>1</td></tr>
<tr><td>General-purpose 1-layer thin-film resistors and conductors, on metal plate.</td><td>RA2</td><td>39</td><td>1</td></tr>
<tr><td>General-purpose 1-layer thin-film conductors in metal package.</td><td>SA1</td><td>33</td><td>2</td></tr>
<tr><td>General-purpose 1-layer thin-film resistors and conductors, in metal package.</td><td>SA2</td><td>33</td><td>2</td></tr>
<tr><td>General-purpose 1-layer thin-film conductors, in ceramic package.</td><td>TA1</td><td>33</td><td>2</td></tr>
<tr><td>General-purpose 1-layer thin-film resistors and conductors, in ceramic package.</td><td>TA2</td><td>33</td><td>2</td></tr>
</table>

**TABLE 7: TYPE DESIGNATIONS AND NUMBERS OF TEST STRUCTURES TO BE MANUFACTURED, AND APPLICABLE TEST PLANS (Continued)**

| DESCRIPTION | Test structure | No. of pcs. to be manuf. | Test Plan No. | Example |
|---|---|---|---|---|
| General-purpose 1-layer thin-film resistors and conductors with components attached, unencapsulated. | QB1<br>QB2 | 39 | 1 | |
| General-purpose 1-layer thin-film resistors and conductors with components attached, on metal plate | RB1<br>RB2 | 39 | 1 | |
| General-purpose 1-layer thin-film resistors and conductors with components attached, in metal package. | SB1<br>SB2 | 33 | 2 | |
| General-purpose 1-layer thin-film resistors and conductors with components attached, in ceramic package. | TB1<br>TB2 | 33 | 2 | |

### 3.2.5 Description and Lay-out of Test Substrates

The following paragraphs describe the lay-out of test substrates A and B. As a guideline, the test structures described and illustrated in the following paragraphs have been implemented on 19.05 x 25.40 mm substrates. The manufacturer may however choose different dimensions according to the technology for which capability approval is sought.

Any commercially available added-on parts required for assembly shall be as far as possible equivalent to space-qualified parts. The manufacturer shall adhere to the specified patterns unless the technology involved requires deviation. In such a case, the revised drawing of the pattern shall be submitted to ESA for approval, i.e if, for example, capability approval is sought for arched or angular conductors, the evaluation phase must always include test structure A, designed with the necessary conductor or resistor outline.

#### 3.2.5.1 Test Structure A1 for 1-layer thin-film conductors

The test structure is illustrated in Figure 1 and is designed to evaluate the etching quality of thin-film conductors. The pattern includes the range of 0.02 to 0.3 mm line width and distance. Moreover, a special pattern of very thin line and very narrow distance for evaluation of the etching quality is included. If applicable, cross-over by wire bonding may be used. Depending on the technology, the substrate may be dismounted or mounted on a base-plate or enclosed in a package.

If applicable, solder leads may be used.

#### 3.2.5.2 Test Structure A2 for 1-layer thin-film resistors and conductors

The structure is illustrated in Figure 2 and is designed to evaluate the etching quality of thin-film conductors and resistors. The thin-film resistors on the substrate shall be one with the highest value, one with the lowest value, one with standard value, and one for shunt trimming.

If applicable, cross-over by wire bonding may be used.

If applicable, other resistors may be designed on the substrate, at positions D and E.

Endurance testing of resistors, including load and load cycle, is to be specified by the manufacturer in agreement with ESA. Depending on the technology, the substrate may be dismounted or mounted on a base-plate or enclosed in a package.

If applicable, solder leads may be used.

6 Lines Conductors

Width: 50 µm
Spacing: 5 - 7 - 10 - 20 - 30 - 50 µm

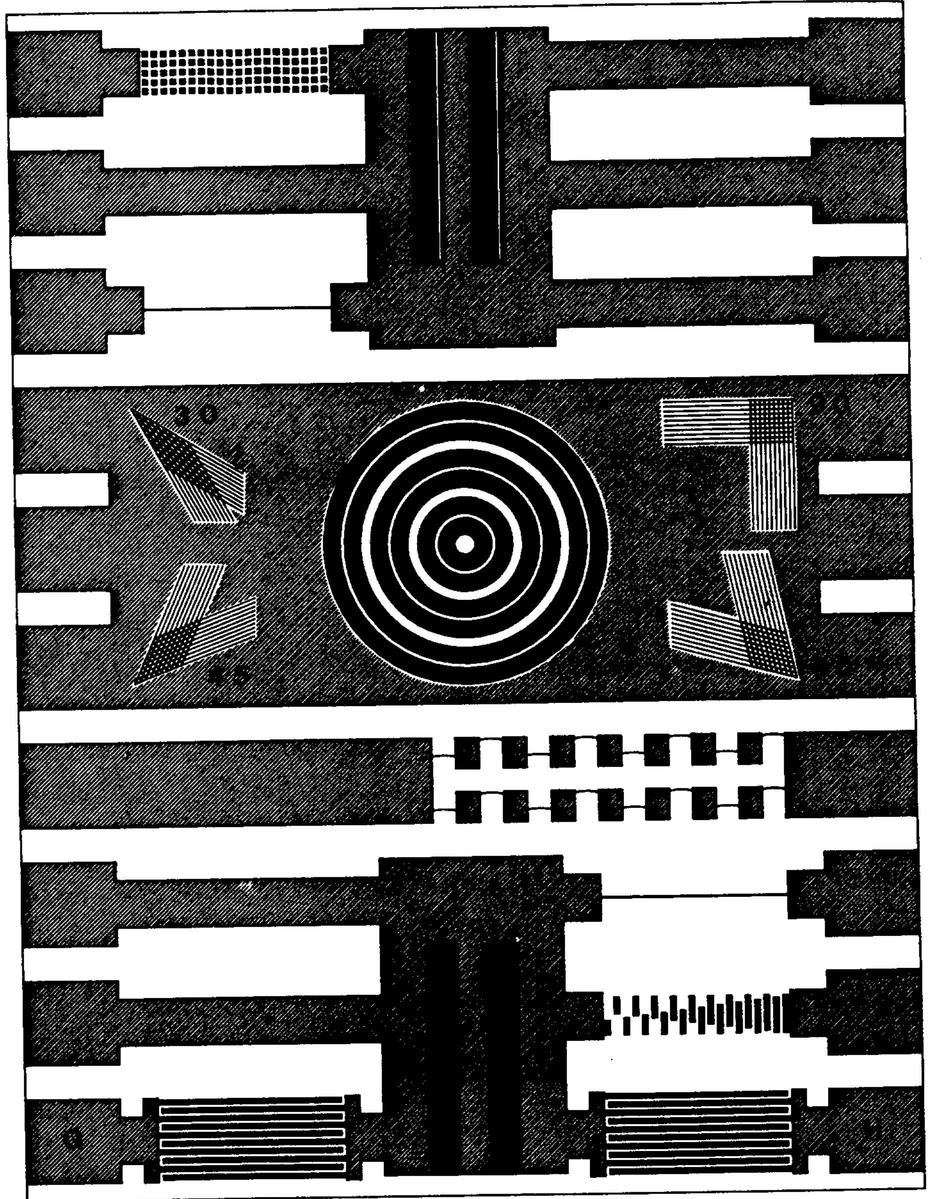
Conductor pattern
50 x 50 µm

20 µm x 40 mm Conductor line

Conductor/Spacing Circle (examples)

Conductor: 20-20-30-50-100-50-30-20-20 µm
Spacing: 50-50-30-40-50-50-40-30-50-50 µm
to be repeated at radius 1 - 2 - 3 mm

Wire Crossover
if applicable



Conductor "Finger"
Pattern Conductor/Spacing

G 100 µm/100 µm
H 50 µm/50 µm or 25 µm/50 µm

7 Lines Conductors

Width: 5 - 7 - 10 - 20 - 30 - 50 - 70 µm
Spacing: 50 µm

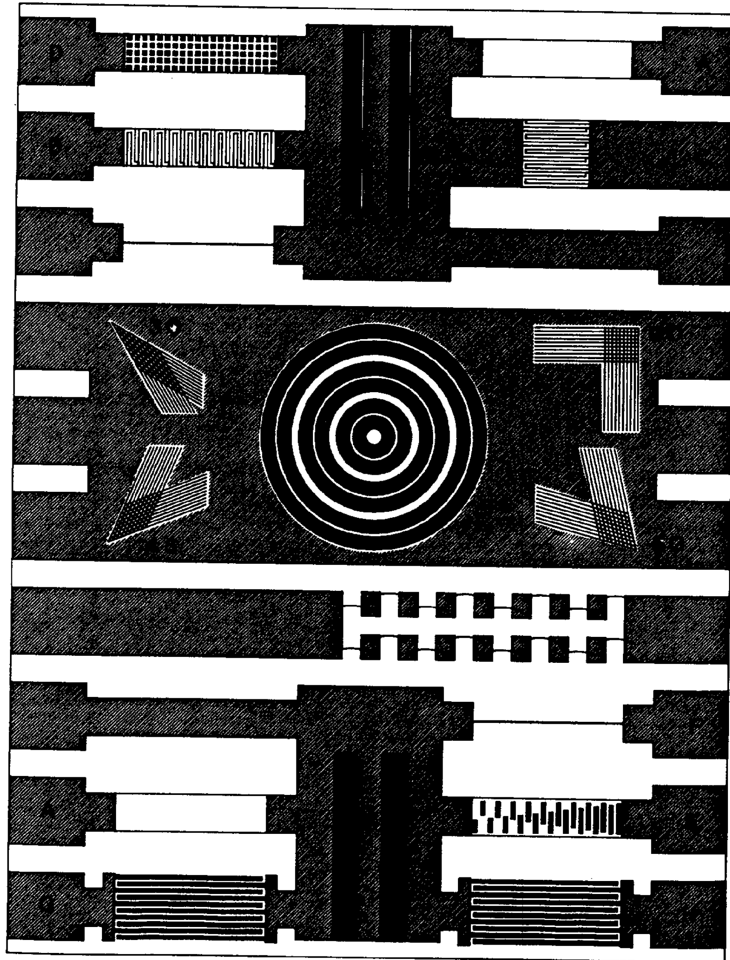
*Figure 1 Test structure A1*

6 Lines Conductors and Resistors

Width: 50 µm
Spacing: 5 - 7 - 10 - 20 - 30 - 50 µm

Resistor Dimensions

A 4 x 1 mm standard value
B 50 µm x 40 mm highest value
C 50 µm x 18 µm lowest value
D Conductor/resistor pattern
50 x 50 µm
E Free position for trimming
shunt resistor, if applicable
F 20 µm x 40 mm resistor line



Conductor/Spacing Circle (examples)

Conductor: 20-20-30-50-100-50-30-20-20 µm
Spacing: 50-50-30-40-50-50-40-30-50-50 µm
to be repeated at radius 1 - 2 - 3 mm

Wire Crossover
if applicable

Conductor "Finger"
Pattern Conductor/Spacing

G 100 µm/100 µm
H 50 µm/50 µm or 25 µm/50 µm

7 Lines Conductors and Resistors

Width: 5 - 7 - 10 - 20 - 30 - 50 - 70 µm
Spacing: 50 µm

*Figure 2 Test structure A2*

### 3.2.5.3 Test Structure B1 for 1-layer thin-film resistors and conductors with components attached

The test structure is illustrated in Figure 3 and specifies thin-film resistors and conductors, a special pattern of very thin lines and small distances for evaluation of the etching quality, positions for attached chip capacitors and active wire-bonded chips. With reference to the subtechniques listed in Table 5, only those sections of the pattern that are required shall be implemented.

**Thin-film resistors**

If applicable, other resistors may be incorporated on the substrate at positions D and E. Endurance testing of resistors, including load and load cycle, is to be specified by the manufacture in agreement with ESA.

**Semiconductors and chip capacitors**

Semiconductors and chip capacitors are not loaded during endurance testing. Depending on the technology, the substrate may be mounted or not, on a base-plate or in a package. If applicable, solder leads may be used.

6 Lines Conductors and Resistors

Width: 50 µm
Spacing: 5 - 7 - 10 - 20 - 30 - 50 µm

Resistor Dimensions

A 4 x 1 mm standard value
B 50 µm x 40 mm highest value
C 50 µm x 18 mm lowest value
D Conductor/resistor pattern 50 x 50 µm
E Free position for trimming shunt resistor, if applicable
F 20 µm x 40 mm resistor line

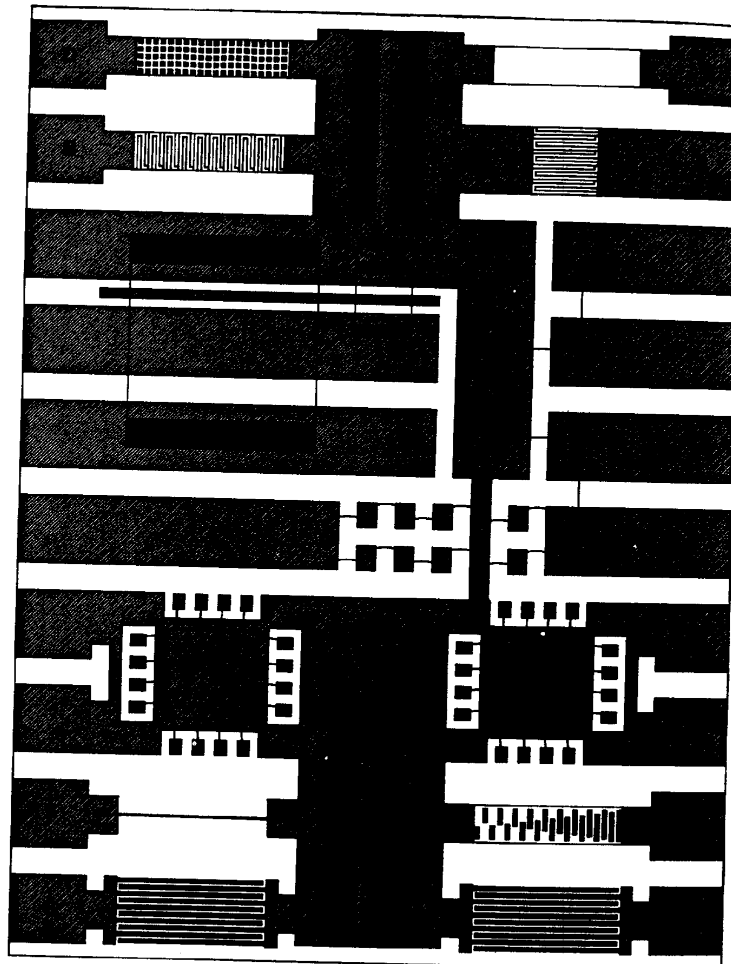
2 Capacitor Chip

1 for the smallest and 1 for the largest size as applicable

Wire Crossover if applicable

Positions for Semiconductor

Attachment (Die mounting and wirebonding) 1 position for the highest and 1 position for the lowest I/O count



Conductor "Finger" Pattern Conductor/Spacing

G 100 µm/100 µm
H 50 µm/50 µm or 25 µm/50 µm

7 Lines Conductors and Resistors

Width: 5 - 7 - 10 - 20 - 30 - 50 - 70 µm
Spacing: 50 µm

*Figure 3 Test structure B1*

### 3.2.5.4 Test Structure B2 for 1-layer thin-film resistors and conductors with components attached

The test structure is illustrated in Figure 4 and specifies thin-film resistors and conductors, a special pattern of very thin lines and small distances for evaluation of the etching quality, positions for attached chip capacitors and active semiconductors mounted by beam lead technique. With reference to the subtechniques listed in Table 5, only those sections of the pattern that are required shall be implemented.

**Thin-film resistors**

If applicable, other resistors may be incorporated on the substrate, e.g. at positions D and E. Endurance testing of resistors, including load and load cycle, is to be specified by the manufacturer in agreement with ESA.

**Semiconductors and chip capacitors**

Semiconductors and chip capacitors are not loaded during endurance testing. Depending on the technology, the substrate may be mounted or not, on a base-plate or in a package. If applicable, solder leads may be used.

6 Lines Conductors and Resistors

Width: 50 µm
Spacing: 5 - 7 - 10 - 20 - 30 - 50 µm

Resistor Dimensions

A 4 x 1 mm standard value
B 50 µm x 40 mm highest value
C 50 µm x 18 mm lowest value
D Conductor/resistor pattern 50 x 50 µm
E Free position for trimming shunt resistor, if applicable
F 20 µm x 40 mm resistor line

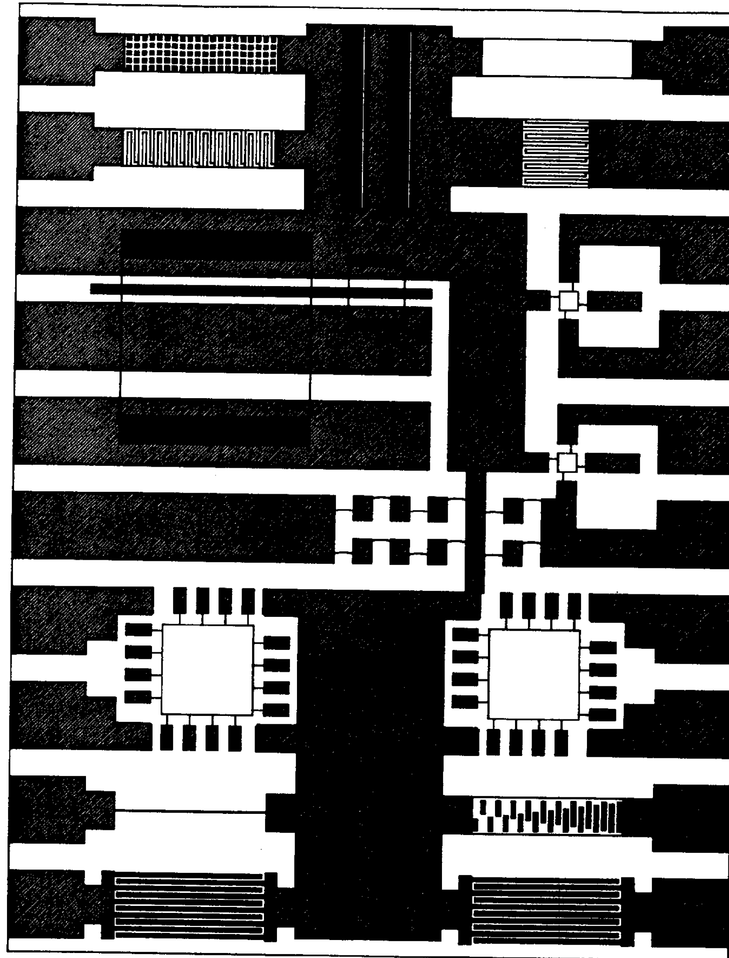
2 Capacitor Chip

1 for the smallest and 1 for the largest size as applicable

Wire Crossover if applicable

Position for Semiconductor

Attachment (beam lead technology)
1 position for the highest and
1 position for the lowest I/O count.



Conductor "Finger"
Pattern Conductor/Spacing

G 100 µm/100 µm
H 50 µm/50 µm or 25 µm/50 µm

7 Lines Conductors and Resistors

Width: 5 - 7 - 10 - 20 - 30 - 50 - 70 µm
Spacing: 50 µm

*Figure 4 Test structure B2*

### 3.2.6 Evaluation Test Plans

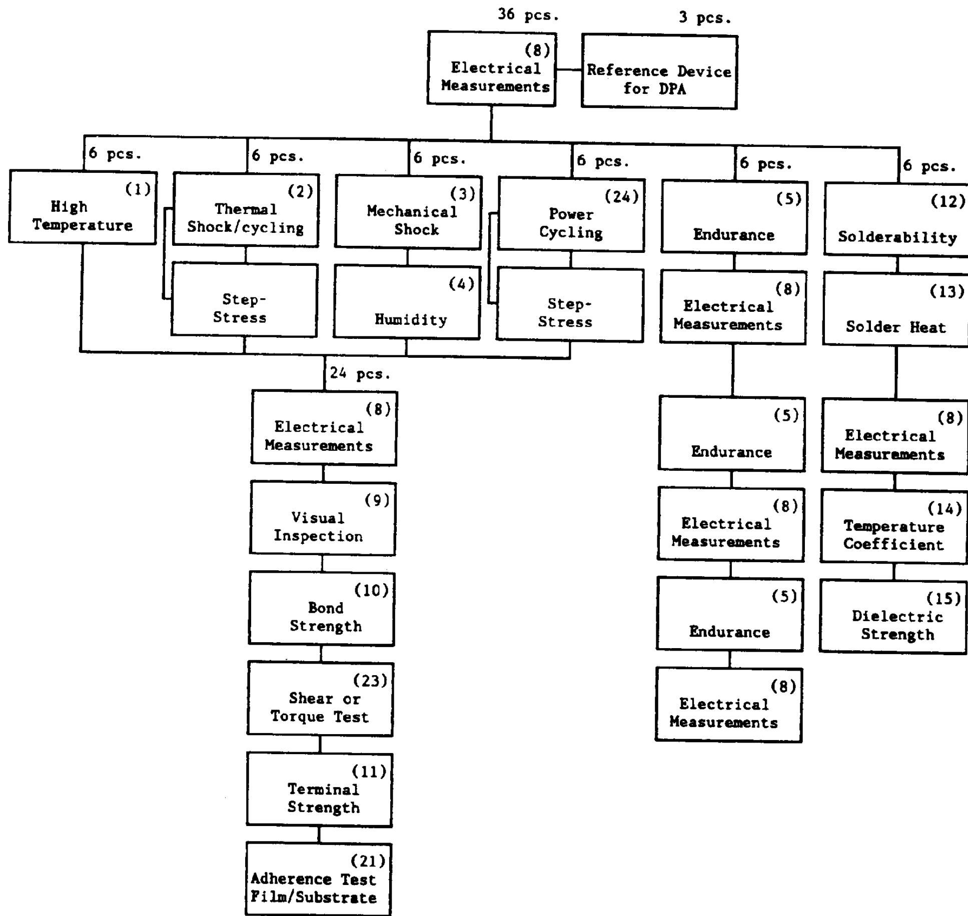
Testing, analysis of test results and presentation of the evaluation test programme shall be in accordance with the test plan and tables specified herein for each test structure. All structures and devices submitted for testing shall be clearly identified by serial numbers.

Upon completion of testing, all devices and all test and inspection results, including a summary of all failure analysis results, shall be submitted to ESA. All measurements shall be recorded.

The reference devices mentioned in the test plan shall serve as control devices enabling the electrical/mechanical characteristics of the test samples to be measured.

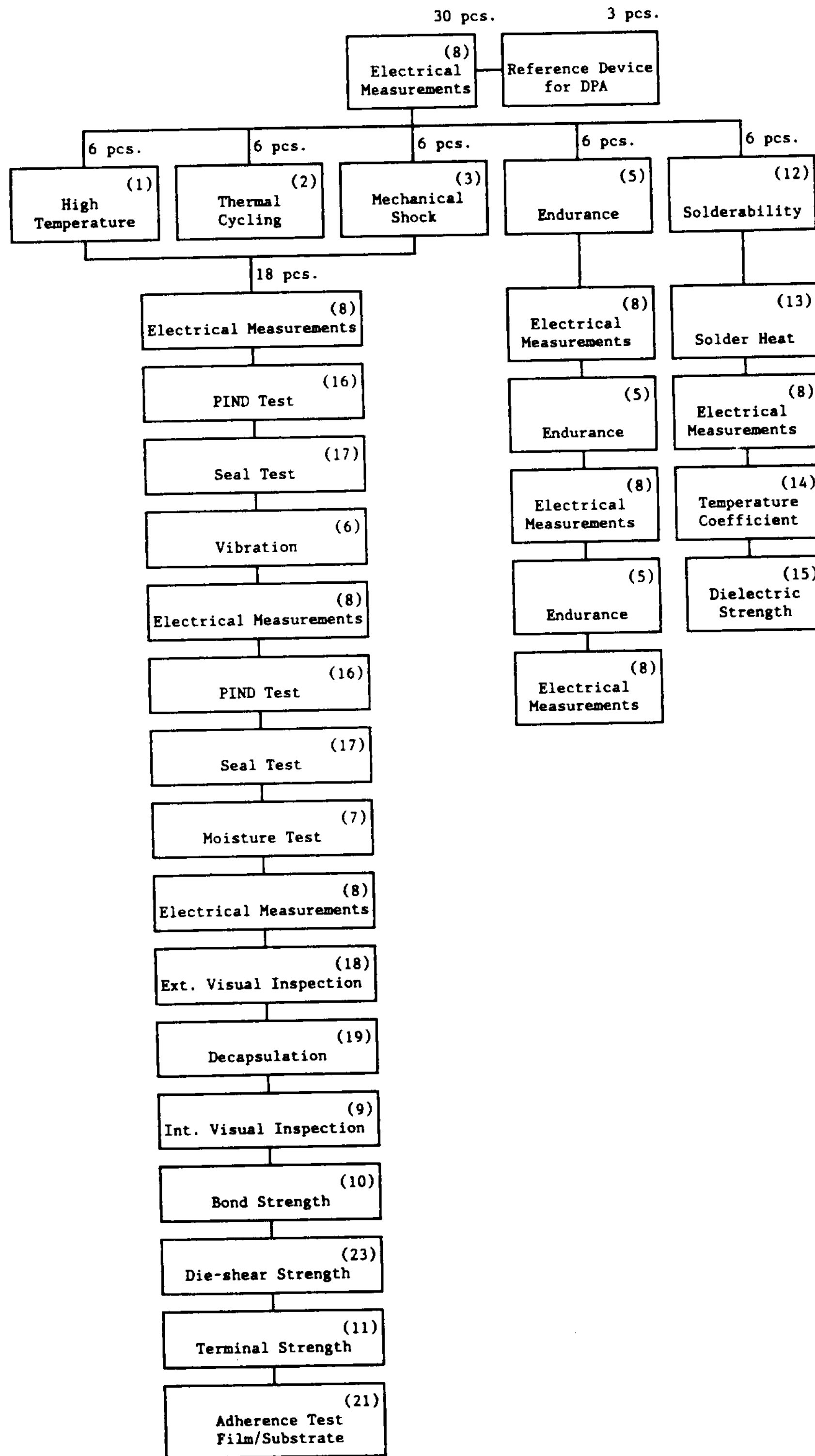
If termination and/or area identification numbers differ from those referenced in this specification, the manufacturer shall provide ESA with a cross-reference table.

The following test plans (Figures 5 and 6) are applicable to the test structures specified in Table 7 and Paragraph 3.2.4.




NOTE: Numbers in parentheses refer to test numbers of Table 8.

*Figure 5 Test plan 1*




NOTE: Numbers in parentheses refer to test numbers of Table 8.

*Figure 6 Test plan 2*

### 3.2.7 Description of Tests

The test procedures pertinent to Test Plans 1 and 2 are listed in Table 8, together with references to the applicable MIL specifications. The number of each test corresponds to that shown in the test plans.

Table 8 shall be used in conjunction with the supplementary test instructions specified for each of the individual test structures listed in Paragraph 3.2.4.

**TABLE 8: TEST PROCEDURES**

| No. | Test | MIL-STD/Method | | Test Conditions and Remarks |
|---|---|---|---|---|
| 1 | High Temperature Storage | 883 | 1008 | Condition 'B': +125°C, 2000 hours |
| 2 | Thermal Cycling | 883 | 1010 | Condition 'B', 100 cycles per step up to 500 cycles or failure |
| 3 | Mechanical Shock | 883 | 2002 | Condition 'C', as per detail spec. |
| 4 | Humidity | 202 | 103B | Duration 2000 hours, no voltage |
| 5 | Endurance | 202 | 108A | Temperature: +125°C, Condition 'F', 2000 hours. Electrical load as specified in Para. 3.4.3.1 |
| 6 | Vibration | 883 | 2007 | Condition 'B', 50 g. Test item shall be glued to the vibration fixture |
| 7 | Moisture Resistance | 883 | 1004 | 10 V DC between all terminals connected together and package; + on terminals |
| 8 | *Electrical Measurements* | 202 | | |
| | — Resistance | | 303 | Test accuracy: ±0.02% thin-film resistors |
| | — Capacitance | | 305 | F = 1 MHz; Test accuracy on C = ±0.1%. Registration of loss factor down to 0.001. Capacitor chips. |
| | — Insulation Resistance | | 302 | Condition 'A', 100 V. The test items are the same as those specified for Test 15, 'Dielectric Strength' |
| | — Semiconductor Components | | | Functional test. Electrical operational conditions shall be normal ones for component concerned. To be specified after joint agreement by ESA and manufacturer. |
| 9 | Internal Visual Inspection | 883 | 2017 | Not applicable to hermetically sealed semiconductor components attached to substrate |
| 10 | Bond Strength | 883 | 2011 | Wire-bonds: Test Condition 'D' |

**TABLE 8: TEST PROCEDURES (Continued)**

| No. | Test | MIL-STD/Method | | Test Conditions and Remarks |
|---|---|---|---|---|
| 11 | Terminal Strength (Ext. termination) | 883 | 2004 | *Flexible leads soldered to Thin Film*<br>Condition 'A'; Force = 30 x Q (Newton); Q = lead ($mm^2$)<br>*Flexible and Semi-flexible Leads in Packages*<br>As above.<br>*Rigid Feed-throughs in Packages*<br>D 1 mm: As above.<br>*Rigid Feed-throughs in Packages*<br>D 1 mm: Condition 'C1';<br>Torque 1.5 N.cm |
| 12 | Solderability (Ext. termination) | 202 | 208 | Three terminals per test item |
| 13 | Soldering Heat (Ext. termination) | 202 | 210 | Condition 'B'. Three terminals per test item. Visual inspection by microscope (magnification x 4) to verify that terminals, glass seals, connection to thin-film substrate or substrate itself are not damaged. |
| 14 | Temperature Coefficient of Resistance (TCR) | 202 | 304 | Maximum temperature: +125°C.<br>Minimum temperature: −55°C. |
| 15 | Dielectric Strength | 202 | 301 | *Test Voltages*<br>Thin-film pattern (all terminals connected together) to plate on reverse side of substrate, to base plate or package: 100 V DC. Between conductors 100 V DC. |
| 16 | Particle Impact Noise Detection (PIND) | 883 | 2020 | Condition 'A' |
| 17 | Seal Test | 883 | 1014 | Step 1: Condition 'A1' or 'A2';<br>Step 2: Packages with lids of 3 cm and less: Condition 'C2'; packages with lids of 3 cm and more: Condition: 'C1' |

**TABLE 8: TEST PROCEDURES (Continued)**

| No. | Test | MIL-STD/Method | | Test Conditions and Remarks |
|---|---|---|---|---|
| 18 | External Visual Inspection | 883 | 2009 | |
| 19 | Decapsulation | Lid shall be removed in such a way that interior of package is not contaminated | | |
| 20 | Radiographic Inspection | 883 | 2012 | |
| 21 | Adherence Test | Under considera-tion | | Under consideration |
| 23 | Die-shear Strength | 883 | 2019 | Shall be performed also on chip capacitors, chip resistors and leadless chip carriers attached to the substrate. Alternatively, torque test may be performed on leadless chip carriers. |
| 24 | Power Cycling | — | — | All components to be powered at nominal power dissipation level. Power shall be switched on and off 500 times (cycles). Lapse time for each cycle shall be 3 × time constant. Power shall be increased in steps up to failure. |

### 3.2.8 Detail Specifications of Test Structures

The manufacturer shall write a detail specification of each test structure to be evaluated. Each specification shall contain tables of the detailed electrical measurements to be performed before and after exposure to environmental tests. The following shall be stated:

(a) **Line-etching quality**
Statement of minimum line width and line distance.

(b) **Thin-film resistors**

| | | |
|---|---|---|
| Manufacturing tolerances | : | ±15% (untrimmed), ±0.1% (trimmed) |
| Maximum change during test | : | ±0.2% |
| Maximum temperature coefficient calculated for any range between two test temperatures | : | As specified by the manufacturer |
| Maximum voltage coefficient | : | As specified by the manufacturer |
| Visual inspection | : | As per MIL-STD-883. |

(c) **Capacitors, attached chips**

| | | |
|---|---|---|
| Maximum loss factor | : | As specified by chip manufacturer |
| Maximum change of loss factor during test | : | 1.5 x initial value |
| Insulation resistance | : | $10^{10}$ Ω minimum |
| Dielectric strength | : | As per MIL-STD-202 |
| Bond strength | : | As per Mil-STD-883 |
| Visual inspection | : | As per MIL-STD-883 |

(d) **Semiconductors, attached**

| | | |
|---|---|---|
| Electrical functional test | : | Test limit to be agreed jointly by manufacturer and ESA |
| Bond strength | : | As per MIL-STD-883 |
| Visual inspection | : | As per MIL-STD-883 |

(e) **Wire cross-overs, internal connections**

| | | |
|---|---|---|
| Bond strength | : | As per MIL-STD-883 |
| Visual inspection | : | As per MIL-STD-883 |

(f) **External connections and leads**

| | | |
|---|---|---|
| Terminal strength | : | As per MIL-STD-883 |
| Visual inspection | : | As per MIL-STD-883 |
| Solderability | : | As per MIL-STD-202 |
| Soldering heat | : | As per MIL-STD-202 |

(g) **Assembly and package**

| | | |
|---|---|---|
| Internal visual inspection | : | As per MIL-STD-883 |
| External visual inspection | : | As per MIL-STD-883 |
| PIND test | : | As per MIL-STD-883 |
| Seal test | : | As per MIL-STD-883 |
| Radiographic inspection | : | As per MIL-STD-883 |

(h) **Structures with base-plate**

| | | |
|---|---|---|
| Visual inspection | : | As per MIL-STD-883 |
| Radiographic inspection (power structures) | : | Area of void(s) under dissipative source shall not be more than 25% of the area of that source. Total void area (sum of all voids at substrate/base-plate interface) shall not exceed 25% of substrate area. |
| Insulation resistance | : | Minimum $10^{10}$ Ω. |

## 3.2.9 Failure analysis

All failed items shall be subjected to failure analysis. The applied procedure shall permit determination of the cause of failure, failure mode and any corrective action required. A detailed test report of all failed items shall be submitted to ESA.

## 3.3 EVALUATION REPORT

The manufacturer shall produce an evaluation report in compliance with this specification and signed on behalf of the company.

### 3.3.1 Analysis of results

At the end of the evaluation phase, ESA will analyse the results of:

- Line survey
- Evaluation testing.

On the basis of the outcome of this review, ESA will decide whether the manufacturer may proceed to the next phase of the programme or whether any corrective actions are required.

### 3.3.2 Corrective actions

ESA may recommend certain modifications to the manufacturer's organisation, the production line and/or processes. If the manufacturer wishes to proceed to the next phase, he shall implement such modifications. If major changes are deemed necessary, ESA may require repetition of certain evaluation tests and/or re-evaluation of test results.

### 3.3.3 Process Identification Document (PID)

The manufacturer shall establish a PID, specifying the agreed procedures for manufacturing control. Details of the contents of the PID are given in Section 4.2 of this specification.

## 3.4 COMPLETION OF EVALUATION PHASE

Upon satisfactory completion of the evaluation phase, ESA will agree the definition of the manufacturer's capabilities and give its consent to proceed to capability approval testing.

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# SECTION 4: CAPABILITY APPROVAL TESTING PHASE

## 4.1 GENERAL

The capability approval testing phase shall cover all tests approved by ESA upon completion of the evaluation phase and consist of:

- the freezing of the processes, process and inspection documents, and materials defined in the Process Identification Document (PID) and
- the manufacture and testing of either test structures or actual circuit types.

## 4.2 PROCESS IDENTIFICATION DOCUMENT (PID)

Before manufacture of the structures to be subjected to testing, the manufacturer shall prepare the PID and agree its contents with ESA. The PID shall be divided into sections according to the following guidelines and reference each process to be applied:

**Section 1**

- Cover page, showing title of PID, issue number and date, and – if applicable – revision letter and date
- Revision list, showing revised pages and dates of revision
- List of contents, showing PID sections.

**Section 2**

Flow chart of manufacture, assembly and testing with reference to the applicable specifications. An example of this flow chart is depicted in Figure 7.

**Section 3**

List of specifications with titles, issue/revision numbers and dates referenced in the flow-chart, and used for the manufacture and control of the devices.

**Section 4**

Organisation of the company, including organigrammes of:

4.1 Management
4.2 Production department
4.3 Quality department

**Section 5**

Processing of hi-rel orders:

5.1 In-house processing flow-chart of hi-rel orders, showing the extent to which each department (Design Engineering, Reliability, Product Assurance, Production, Quality Control, etc.) is responsible for the execution of external orders for hybrid circuits.

5.2 Procurement options, viz variants and testing levels of qualified hybrid microcircuits which the manufacturer can offer.

5.3 Specimen of a hi-rel traveller.

5.4 Points for inspection by orderer.

**Section 6**

List of sub-techniques, materials and rework:

6.1 All subtechniques and associated test structures used shall be listed. This section shall include a colour photograph of the test structure(s) to be tested.

6.2 All materials, such as substrates, films, epoxies (with infrared spectrum), wires, packages etc., shall be listed, together with the manufacture's name, incoming inspection specification and, where applicable, the validation procedure.

6.3 Provisions for rework shall detail how, when, the number of times and according to what procedure, rework is permitted.

**Section 7**

Manufacturing line lay-out:

7.1 Overall line lay-out

7.2 Details of testing area

7.3 Dust, humidity and temperature control of the various areas.

**Section 8**

Equipment list.

**Section 9**

List of failure analysis equipment

Standard failure analysis procedure.

**Section 10**

Records of lots processed according to the subject PID, including number(s) and type(s) of circuits, lot acceptance results and applicable qualification reports. This section shall be updated annually.

The information contained in this section shall be arranged as exemplified in Table 9 and, as a minimum, include the items listed therein.

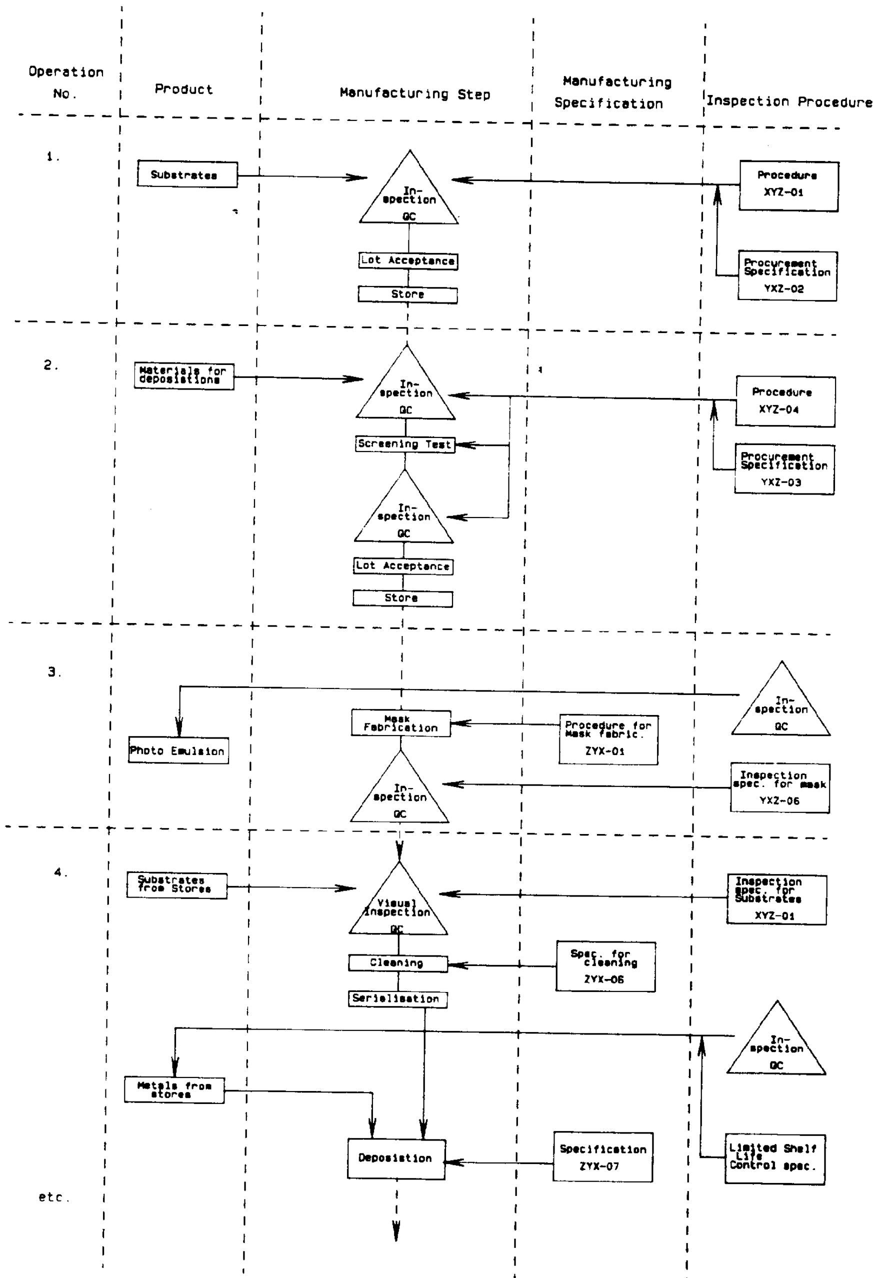



*Figure 7 Example of manufacturing flow chart*

**TABLE 9: EXAMPLE OF INFORMATION TO BE ENTERED IN SECTION 10 OF PID**

| Programme or project | No.of circuits produced | Screening level | Description of circuit | Spec. No. | Lot No. | Lot qual. rep. |
|---|---|---|---|---|---|---|
| Exosat | 20 | B | Control circuit | XYZ-123 | 8230 | ABC-456 |

The established PID shall be called up automatically in any documentation applicable to deliveries according to this specification or ESA Procurement Specification PSS-01-608. Any deviations from the PID shall be subject to prior ESA approval.

The complete PID, comprising all called-up specifications, shall be kept by the manufacturer at the production plant; it shall be made available to ESA or its designated representative for review.

A condensed PID, comprising all basic information, e.g. flowcharts, lists of specifications, materials and processes, but complemented by copies of only the most important specifications, shall be kept by ESA and treated as proprietary information.

The PID shall be made available to the orderer for inspection. The production flow-chart shall always be made available to the orderer upon request.

Travel-logs shall include all processing details, dates and yields of major process steps and any useful comments. They shall be signed or stamped on behalf of the manufacturer's quality assurance department in respect of those operations that are listed as functions of that department. The manufacturer shall keep the travel-logs for a minimum period of three years and, upon request, make them available to ESA, its designated representative, or the orderer.

## 4.3 DETAIL SPECIFICATIONS

Before testing starts, all detail specifications of test structures shall be prepared by the manufacturer and submitted to ESA for approval. They shall be written according to Annex B of ESA PSS-01-608.

## 4.4 MANUFACTURE OF TEST STRUCTURES

Lot manufacture shall be in accordance with the approved PID and all parts thereof shall be selected and screened to level B as set out in specification ESA PSS-01-608. ESA reserves the right to participate in precap visual inspection.

## 4.5 ADDED-ON COMPONENTS

See specification ESA PSS-01-608.

## 4.6 REWORK

Some of the circuits submitted to testing shall have been reworked according to the methods described in the PID.

General rules for rework are as specified in MIL-M-38510 for class 'S' devices.

## 4.7 LOT PRODUCTION REPORTS

The manufacturer shall submit to ESA reports of:

- screening (including burn-in parameter drift values)
- final acceptance test
- failure analysis of parts failed during screening
- in/out figures relevant to the following inspections and tests:
  - visual inspection and final test of thin film network
  - pre-seal acceptance test
  - screening
  - final acceptance test

The in/out figures shall be recorded in terms of the number of parts submitted to a specific test, or group of tests, and the number of rejects. Failure mode data shall be included.

## 4.8 TEST PLAN

The manufacturer shall prepare and submit to ESA for approval a test plan, including a specification of each test structure and a time schedule for production and tests. The time schedule shall show the dates envisaged for performance of the following milestone operations:

- start of manufacture
- start of pre-seal acceptance test
- start of screening and final test
- start of mechanical, environmental and endurance tests
- completion of mechanical, environmental and endurance tests.

The manufacturer shall notify ESA, or its delegated representative, as soon as each of these operations has been completed.

All documents specified herein for review by ESA shall be submitted at least 22 working days before either the due review date or the date on which the manufacturer intends to proceed to the next action in the sequence of operations.

## 4.9 CAPABILITY APPROVAL TESTING

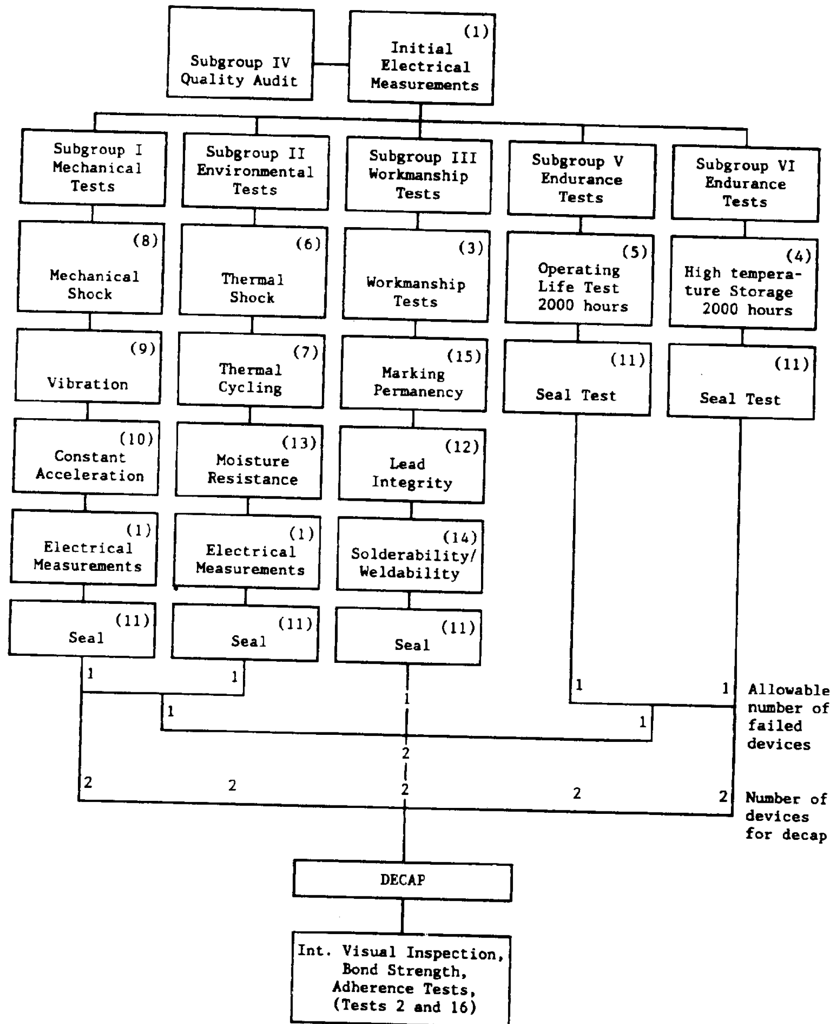
Testing shall be performed in accordance with the test plan shown in Figure 8 for a general-purpose thin-film microcircuit, encapsulated in a package and the requirements defined in the following subparagraphs.

The total number of test structures shall depend on the number of structures/types to be tested. It may be necessary to test more than one type of structure. If so, the number of structures specified in Table 10 shall be applicable. The lay-out of the test structure(s) may be identical to that of any structure specified for the Evaluation Phase or that of a new structure.

Satisfactory test results of reworked test structures shall automatically imply the acceptance of non-reworked test structures. Where the test structures are of several types, they shall be distributed over the various subgroups as shown in Table 10.

**TABLE 10: NUMBER OF TEST STRUCTURES FOR CAPABILITY APPROVAL**

| Number of types of test structure | Number of types required per subgroup | | | | | | Total number per type |
|---|---|---|---|---|---|---|---|
| | I | II | III | IV | V | VI | |
| 1 | 6 | 6 | 3 | 3 | 10 | 6 | 34 |
| 2 | 3 | 3 | 2 | 2 | 6 | 3 | 19 |
| 3 | 2 | 2 | 1 | 1 | 4 | 2 | 12 |




Numbers in parantheses refer to test numbers of Table 11.

*Figure 8 Test plan*

### 4.9.1 Subgroup III, Workmanship

Workmanship shall be assessed as follows:

- Radiographic inspection
- External visual inspection (including marking)
- Physical dimensions and weight
- Internal water vapour content

#### 4.9.1.1 Radiographic Inspection

This inspection shall be performed in accordance with MIL-STD-883, Method 2012.

#### 4.9.1.2 External Visual Inspection (including marking)

This inspection shall be performed according to MIL-STD-883, Method 2009. The marking shall be inspected to ascertain its conformance to the requirements of the applicable test structure detail specification. It shall be legible and unambiguous. Any misalignment of the highest and lowest letters in a row shall not exceed 70% of the letter size. The overlapping of the lowest letters of one row and the highest letters of the next row shall constitute a failure.

#### 4.9.1.3 Physical Dimensions and Weight

All physical dimensions specified in the applicable detail specification shall be measured. Any nonconforming part shall be considered as a failure and contribute towards qualification failure. Two or more non-conforming dimensions of one part shall count as one failure.

All parts shall be weighed and the average weight per part recorded.

#### 4.9.1.4 Internal Water Vapour Content

This shall be determined according to MIL-STD-883C, Method 1018.2, on 1 (one) package.

### 4.9.2 Subgroup IV, Quality Audit

The devices of this subgroup together with the results of the initial electrical test shall be sent to ESA for construction analysis as follows.

The devices of this group will be subjected to the inspections and operations defined in the following subparagraphs. A record will be made of each separate step and all records will be compiled and summerised in one report together with the analysis results.

**(a) Decap**
The parts will be decapped or opened without damage to the functional elements. Any inspection of a decapped device will take place in a controlled atmosphere.

**(b) Description**
Each part type will be described fully and photographed in such a way that the interior of the package and the functional elements are highlighted. Descriptions will include measurement data of physical dimensions and relative location of added parts.

**(c) Internal Visual Inspection**
The parts will be inspected for conformity to the applicable requirements of MIL-STD-883, Method 2017 and Condition 'A' of Method 2010.
Any visual anomalies will be microphotographed and the presence of any foreign matter will be recorded.
The parts will be inspected by a Scanning Electron Microscope (SEM) to verify that bonds, joints, trimming paths, metallisation steps etc. meet the specified requirements. Each of these items will also be photographed.

**(d) Bond Strength/Adherence Group**
The control devices will be submitted to the following tests listed in Table 11:
— Bond Strength (Test 16a)
— Chip adherence (Test 16b)
— Substrate adherence (Test 16c)

All test results, including failure categories, will be recorded.

**(e) Any Other Construction Analysis Tests**
For example: seal test, PIND test, water vapour content, etc.

**TABLE 11: TEST METHODS**

| No. | Test | MIL-STD-883, Method no. | Conditions and/or Remarks |
|---|---|---|---|
| 1 | Electrical measurements | Electrical measurements of all parameters listed in the detail specification shall be performed in accordance with the test methods and conditions specified in that specification. All results shall be recorded and all samples allocated to testing shall be submitted to these electrical tests prior to the start of testing.<br>There shall be no catastrophic electrical failures at this stage. Any such failures shall invalidate the approval.<br>Any devices exhibiting electrical out-of-tolerance parameters shall be replaced. Inspections shall be made during and on completion of the mechanical, environmental and endurance tests. Failures observed during these measurements shall count as failed devices. | |
| 2 | Internal Visual Inspection | 2017 | and Condition 'A' of Method 2010 |
| 3 | Workmanship | | See Para. 4.9.1. |
| 3a | Radiographic Inspection | 2012 | |
| 3b | External Visual Inspection | 2009 | |
| 3c | Physical Dimensions | | See detail specification and Para. 4.9.1.3 of this specification |
| 4 | High Temperature | 1008 | Condition 'B'. Electrical measurements as specified in the detail specification shall be recorded at 0, 168 and 500 + 48 hours. Total duration of tests shall be 2000 + 96 hours. Histograms shall be made at each measurement. The final drift percentage of each parameter in relation to the initial 0-hour measurement shall be recorded. |

**TABLE 11: TEST METHODS (continued)**

| No. | Test | MIL-STD-883, Method no. | Conditions and/or Remarks |
|---|---|---|---|
| 5 | Operating Life | 1005 | Conditions as specified in the detail specification. Electrical measurements as specified in the detail specification shall be recorded at 0, 168 and 500 + 24 hours; 1000 + 48 hours and 2000 + 48 hours. Total duration of tests shall be 2000 + 6 hours. Histograms shall be made at each measurement. The final drift percentage of each parameter in relation to the initial 0-hour measurement shall be recorded. |
| 6 | Thermal Shock | 1011 | Condition 'B'; go-no-go electrical measurements after test |
| 7 | Thermal Cycling | 1010 | -ditto- |
| 8 | Mechanical Shock | 2002 | Condition as specified in ESA PSS-01-608 |
| 9 | Vibration | 2007 | Condition 'A'; go-no-go electrical measurements after test |
| 10 | Constant Acceleration | 2001 | Condition as specified in ESA PSS-01-608; go-no-go electrical measurements after test |
| 11 | Seal | 1014 | Condition 'A', fine leak; Condition 'C', gross leak |
| 12 | Lead Integrity | 2004 | Conditions 'B1' and 'C1'as applicable. Measurements: only visual inspection for damage |
| 13 | Moisture Resistance | 1004 | Lead Integrity test is considered as initial conditioning |
| 14 | Solderability/ Weldability | 2003 | All terminations |

**TABLE 11: TEST METHODS (continued)**

| No. | Test | MIL-STD-883, Method no. | Conditions and/or Remarks |
|---|---|---|---|
| 15 | Marking Permanency | 2015 | |
| 16 | Bond Strength/ Adherence<br>(a) Bond Strength<br>(b) Chip Adherence<br>(c) Substrate Attachment Strength | <br><br>2011<br>2019<br>2027 | <br><br>Condition 'D' |

## 4.10 TEST REVIEW

### 4.10.1 Data Presentation

The data files to be prepared for each tested structure shall be entitled 'Data File of Capability Approval Testing of ......(part type)' and bear the relevant contract number and date. Each file shall contain:

#### 4.10.1.1 Summary Schedule Sheet(s)

This sheet (or sheets) shall summarise the entire test sequence and include in/out burn-in numbers, scheduled and actual data of each operation and relevant electrical tests (e.g. go-no-go recorded etc.). The sheet(s) shall be presented in such a way that status can easily be ascertained.

Updated summary sheet(s), showing relevant part type and lot number(s), shall be sent to ESA at each agreed milestone.

#### 4.10.1.2 Equipment Accuracy

The manufacturer shall provide ESA with a list of all equipment to be used and the accuracy thereof, including the applicable calibration controls.

#### 4.10.1.3 Data Records and Histograms

Data records and histograms shall provide all information obtained from the time of burn-in up to and including end of test. Any data related to the Subgroup Control Device shall also be included. Each recorded parameter shall be marked with a symbol and listed together with the pertinent measurement conditions and limits.

Where a parameter drift requirement is specified, the data shall include both drift percentage and absolute change. The same information shall be provided in respect of parameters measured during life testing, even if no parameter drift criteria are applicable during such testing.

The manufacturer shall supply histograms of the measured parameters, containing all records from time of burn-in up to and including end of testing as well as the average sigma and two sigma. If parameter drift is specified, a histogram of the percentage and/or absolute drift shall be included.

#### 4.10.1.4 Other Requirements

The test review data shall include an index and any relevant comments and graphs.

### 4.10.2 Failure Criteria and Classification

Failures of any of the categories specified in the following subparagraphs shall contribute towards failure. Each part exhibiting a failure of any of these categories shall count as one failure.

#### 4.10.2.1 Visual and Mechanical Inspection

These inspections form part of the Quality Audit Procedure. The detection of any defective units at this stage may be cause for verification of the entire lot, the replacement of defective parts or the suspension of testing and ordering of a new lot. Such defective parts shall be considered as rejects and contribute towards lot acceptance/rejection.

#### 4.10.2.2 Out-of-tolerance Parameters

These parameters shall be measured during the initial electrical tests. Defective units shall not be submitted to qualification testing. Any defects noted during subsequent electrical measurements shall be considered as rejects and contribute towards lot acceptance/rejection.

#### 4.10.2.3 Degradation

This applies to those parameters that, following the original measurement, exceed the specified limits when subsequent measurements are performed. Any devices whose parameters do not conform to the specified limits shall be considered as rejects.

If the relevant detail specification prescribes delta values for a particular parameter, the applicable limit shall be the absolute limit plus or minus the appropriate delta limit.

#### 4.10.2.4 Parameter Drift

Devices whose parameter drift exceeds the limits defined in the detail specification shall be considered as rejects and contribute towards failure. Even if no accept/reject criteria are specified, ESA reserves the right to suspend the approval of test results in the event of sudden large parameter changes and/or anomalous behaviour for which no reasonable explanation can be given.

#### 4.10.2.5 Catastrophic Failures

This type of failure occurs when parameters exceed the specified limits to such an extent that a device is rendered ineffective. Devices that have failed catastrophically shall be considered as rejects.

#### 4.10.2.6 Operator Errors

These are failures caused by electrical or mechanical overstress which, normally, do not contribute towards failure. However, when a failure of this category is detected, the testing of the subgroup concerned shall cease immediately and the manufacturer shall notify ESA without delay. The manufacturer shall then take appropriate action to determine the cause of the failure and, when this is established, satisfy ESA that such cause has been isolated and remedied. ESA will then decide in the light of all the available evidence whether or not those parts that may have suffered overstress are to be replaced. Any replacement parts shall be submitted to all the tests that the replaced parts have undergone. Replacement parts shall always be from the same production lot as the original parts and must have been processed identically.

## 4.11 CAPABILITY APPROVAL

Capability approval status will be granted by ESA authority upon satisfactory completion of evaluation and capability approval testing and will be valid for two years.

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# SECTION 5: MAINTENANCE, SUSPENSION AND WITHDRAWAL OF CAPABILITY APPROVAL

## 5.1 MAINTENANCE OF CAPABILITY APPROVAL

Capability approval is maintained by the continuous production of devices according to the technology defined in the PID. At least two months before the expiry date of line approval, the manufacturer shall furnish ESA with the following details of lots processed to ESA Specification PSS-01-608: lot numbers, deliverable parts and numbers and a synthsis of failures during burn-in, environmental and life testing. If considered necessary, ESA may require further details.

The minimum requirement for capability approval is that, during the last 12-month lapse period, one lot of hybrids has been manufactured, screened and tested for lot acceptance in accordance with ESA PSS-01-608. Renewal of capability approval shall be valid either from the date on which

(a) the previous approval expired, or
(b) the date on which lot acceptance testing was completed successfully if this date occurred more than six months before (a).

In addition, the manufacturer shall provide ESA with three samples of a recently manufactured hi-rel batch of components for destructive physical analysis (DPA). On the basis of both the information received and the DPA results, ESA will then decide whether approval can be maintained. In the case of any deviations from the qualified technology, i.e. if new materials and/or processes are to be introduced, ESA and the manufacturer will jointly agree on a testing programme which will cover the new techniques and serve for approval maintenance purposes.

## 5.2 SUSPENSION OF CAPABILITY APPROVAL

ESA may suspend the approval status of a production line, or any part thereof, for the following reasons:

(a) failure(s) that cannot be remedied within a reasonably short period of time;
(b) failure of more than two consecutive lots.

In the event of (a) and (b), the manufacturer shall initiate any corrective action considered appropriate and, to achieve reinstatement of approval status, supply ESA with evidence that the cause of failure has been eliminated.

During the suspension period, the line shall not be considered as approved and not be used for the production of circuits unless they serve for approval purposes.

## 5.3 WITHDRAWAL OF CAPABILITY APPROVAL

Approval status will be withdrawn:

(a) at the request of the manufacturer;

(b) in the case of persistent nonadherence to the production processes agreed for capability approval.

# ANNEX
# DEFINITIONS

**CHIP COMPONENT**

A component in its ultimate state of miniaturrisation.

**COMPONENT**

A device which performs an electronic, electrical or electromechanical function and consists of one or more elements joined together which, normally, cannot be disassembled without destruction. The terms component and part are interchangeable. Typical examples of components are: transistors, integrated circuits, hybrids, capacitors etc.

**DESTRUCTIVE PHYSICAL ANALYSIS (DPA)**

A series of inspections, tests and analyses of a sample component to verify that the materials, design and workmanship used for its construction as well as the construction itself meet the requirements of the applicable specification and are auitable for the intended application.

**DEVIATION**

A written authorisation to accept a specific item which, during production or after inspection, has been found to deviate from the applicable requirements, but is nevertheless considered to be suitable for 'use-as-is' or after 'rework' by an approved method.

**FILM NETWORK**

Layers of conductive, resistive, dielectric and/or passivating materials deposited onto an insulating substrate for the purpose of performing electronic circuit functions.

**HYBRID MICROCIRCUIT**

A component performing an electronic circuit function which consists of a thick- or thin-film network on a substrate which supports active and/or passive chip components connected to it.

**LIMITED LIFE MATERIAL**

A material that can be processed and stored for only a limited period of time before deterioration of its specified properties occurs.

**NONCONFORMANCE**
An apparent or proven condition of any item or document that does not conform to the specified requirements and may lead to incorrect operation or interpretation during its envisaged usage. The term 'nonconformance' is also used for failure, discrepancy, defect, anomaly, malfunction and deficiency.

**PROCESS IDENTIFICATION DOCUMENT (PID)**
A set of frozen documents defining the technology, processes and inspection procedures applicable to the manufacture of the components or items on order.

**PRODUCTION LOT**
A production lot consisting of a quantity of a specific device type manufactured on the same production line by the same processing techniques and according to the same component/part design using the same raw materials during one uninterrupted production run.

**SELECTED SUBLOT**
A selected sublot is that part of a production lot which is manufactured in excess of the actual quantity of components required.

**SYMBOLS AND ABBREVIATIONS**
The symbols and abbreviations defined in MIL-S-19500, MIL-M-38150, MIL-STD-883, specifications ESA PSS-01-60, ESA PSS-01-606, this specification and the applicable detail specifications shall be applicable.

**THICK FILM**
A network onto which the film is deposited by screen-printing methods. The thickness of the fixed film is usually in the range of 10 to 25 micrometres.

**THIN FILM**
A network onto which the film is deposited by one or more of the following processes: electro-depositing, plating, evaporation, sputtering, anodisation or polymerisation. The thickness of the film may be in the range of 50 to 2000 Å.

**TRACEABILITY**
To derive from recorded identification data the history, application, use and location of an item.