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Capability approval programme for microwave hybrid integrated circuits (MHICs)

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ABSTRACT

This specification defines the general requirements for capability approval of a manufacturing line for Microwave Hybrid Integrated Circuits (MHICs). For procurement requirements, see ESA PSS-01-608. ESA approval mandate will be exercised upon conclusion of the Evaluation Phase and at the end of the programme.

DOCUMENTATION CHANGE RECORD

Rev. letter	Rev. date	Page	Change item	Approved DCR no.

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SECTION 1: SCOPE

This specification defines the general requirements for capability approval of a manufacturing line for Microwave Hybrid Integrated Circuits (MHICs). For procurement requirements, see ESA PSS-01-608. ESA approval mandate will be exercised upon conclusion of the Evaluation Phase and at the end of the programme.

Before the Evaluation Phase can commence, the manufacturer shall define the capability approval domain by specifying the processes, materials and techniques involved in the technology for which approval is sought.

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SECTION 2: GENERAL

2.1 INTRODUCTION

The manufacturer shall have and implement an evaluation and approval programme compatible with this specification. The review of this programme by ESA is part of the capability approval.

The manufacturer shall be responsible for the performance of tests and inspections required by this specification. All of these tests and inspections shall be performed at the plant of the manufacturer and approved by the manufacturer's Quality Assurance organisation. The use of external facilities and/or services is subject to prior ESA approval.

ESA, or its designated representative, reserves the right to participate in, or execute, surveys, audits, reviews and source inspections as well as to witness any tests and to have resident or temporary personnel at the manufacturer's plant during the programme period. Participation by ESA, or its designated representative, in any approval activities shall never be considered as substitution for, or release from, the manufacturer's responsibilities.

The manufacturer shall grant personnel of ESA, and/or its designated representative, free access to any documentation, hardware and facilities listed in the Process Identification Document (PID).

2.2 APPLICABLE DOCUMENTS

The following documents are applicable to the extent specified herein.

ESA PSS-01-20	Quality assurance of ESA spacecraft and associated equipment
ESA PSS-01-60	Component selection procurement and control for ESA spacecraft and associated equipment
ESA PSS-01-606	Capability approval programme for hermetic thick-film hybrid microcircuits
ESA PSS-01-70	Materials and process selection and quality control for ESA spacecraft and associated equipment
ESA PSS-01-201	Contamination and cleanliness control
ESA PSS-01-608	Generic specification for hybrid microcircuits
ESA PSS-01-611	Checklist for thin-film hybrid microcircuit manufacturers and line survey
MIL-STD-202	Test methods for electronic and electrical component parts
MIL-STD-883	Test methods and procedures for micro-electronics
MIL-S-19500	Semiconductor devices, general specification for
MIL-M-38510	Microcircuits, general specification for

2.3 DEFINITIONS

The definitions listed in the Annex shall apply.

2.4 ACCESS TO MANUFACTURING FACILITIES

2.4.1 Manufacturer's authorisation

To enable the survey team of ESA, or its delegated representative, to carry out the capability survey and line survey, the manufacturer shall grant free access to the facilities concerned. He shall also enable the team to witness any development, engineering, production and quality assurance operations involved in the processes for which approval is sought.

2.4.2 Checklist

To facilitate the evaluation procedure, ESA will apply Checklist ESA PSS-01-611.

2.5 CAPABILITY SURVEY

The purpose of this survey is to assess the following aspects of the manufacturer's organisation:

(a) General organisation and management,
(b) Quality and Reliability Assurance organisation, including definition of authority and effectiveness,
(c) Facilities and capabilities of the plant in which the microwave hybrid integrated circuits will be manufactured and tested,
(d) Nonconformance control.

Before and/or during the actual survey, the manufacturer shall provide ESA with any documentation which may assist the survey team in the execution of its tasks. As a minimum, this documentation shall include:

- An organigram delineating authority, responsibility and interrelationship between Engineering, Production, Quality and Reliability Assurance, Procurement and Management;
- Expertise of all key personnel employed in the Production and Product Assurance Departments;
- A list of contracts with ESA and/or national space agencies for component evaluation and qualification;
- The name(s) and location(s) of any other plant(s) of the manufacturer where electronic parts are produced according to the same, or a similar, technology as applied to the hybrid integrated circuits for which qualification is sought;

- A flow-chart and any available procedures relative to the processes and controls applied in the production of the devices to be evaluated and approved.

2.5.1 Organisation and management

The manufacturer shall clearly define his policy on:

- Authority and responsibility of quality and reliability management vis-a-vis general management;
- Support requested by the research and development department from engineering and/or quality assurance personnel;
- Employee motivation (bonus scheme, incentives, operator training and certification etc.).

2.5.2 Assessment of design rules

For assessment of the design of Microwave Hybrid Integrated Circuits, the manufacturer shall provide ESA with the design rules he proposes to apply. General design guidelines are given in ESA PSS-01-610.

2.6 PRODUCT ASSURANCE REQUIREMENTS

2.6.1 Organisation and responsibilities

The manufacturer shall have an effective Quality and Reliability organisation, suitable facilities and component Product Assurance personnel with a sufficient degree of independence from the company's design and manufacturing functions to deal objectively with the Product Assurance aspects of the hybrid integrated circuits in compliance with the applicable ESA documents.

The Quality and Reliability organisation shall have direct and unimpeded access to higher management, to which it shall report regularly on the status and adequacy of the programme.

The Quality Assurance organisation shall be responsible for the implementation of all requirements of this specification and the execution of this programme to the satisfaction of ESA. It shall present to the customer only those items/documents which it determines to be in full compliance with those requirements of this and all applicable specifications listed that concern ESA.

2.6.2 Quality assurance requirements

The manufacturer shall establish and implement a Quality and Reliability programme which fully complies with the applicable ESA PSS specifications listed in Section 2.2. Special attention shall be paid to:

- Training of operators/inspectors,
- Definition of workmanship standards,
- Configuration Control,
- Quality assurance activities according to ESA PSS-01-20,
- Materials and process selection according to ESA PSS-01-70 and ESA PSS-01-701.

2.7 LAY-OUT OF FACILITIES

Before the line survey, the manufacturer shall provide ESA with a plan of the facilities to be surveyed, showing the location of each production area, the cleanliness standards and dust count frequency applicable to each area and operation, and including a list of equipment, specifying its accuracy and calibration frequency.

2.8 LINE SURVEY

During this survey which will comprise all aspects of the production line, special attention will be paid to those processes, process steps, materials, piece parts and controls that are involved in the manufacture of the devices concerned. The manufacturer shall demonstrate to ESA the methods evolved on the basis of in-house experience for investigation and optimisation of all processes for which approval is sought. For the purpose of this survey, the subject test structures will be divided according to the major processes performed in the three main production areas of a microwave hybrid integrated circuit manufacturing facility, namely:

(a) Thin-film Network
The pure thin-film circuit requires basically the film deposition and the etching technique, resistor trimming (if applicable), without additions or encapsulation;

(b) Thin-film Hybrid Assembly
This involves the adding-on of chips or other circuits and their connection to the substrate;

(c) Encapsulation or Mounting of Microwave Circuit
This involves the encapsulation of the substrate or its mounting onto a base-plate or similar structure.

NOTE: In certain cases, mounting may be considered as part of assembly (b).

2.8.1 Production documents

All documents related to the processes for which capability approval is sought shall be made available to ESA. Any proprietary documents shall be included, but marked as such.

These documents shall include the following:

2.8.1.1 Process flow-chart

These charts, a relevant example of which shall be provided to ESA before the line survey, shall show the sequence of production and inspection steps for each product type. Inspections shall include each measurement, test or visual examination performed. The flow-charts shall also show:
- number, issue and revision date of the specification applicable to each production and inspection step;
- department, division or section responsible for each operation involved in the processing, production and quality control;
- point at which statistical control records are applied.

The issue and revision date of the above-mentioned documents may be listed separately.

2.8.1.2 Travelling documents

The manufacturer shall prepare and use a travelling document for each lot. This document shall show as a minimum:
- lot identification,
- operation,
- date of each operation,
- number in/out at each operation and where applicable serial numbers of the items removed,
- operator identification,
- nonconformance references,
- Serial numbers of the items constituting the lot (where applicable).

2.8.1.3 Process control chart

The process control chart shall show as a minimum:
- title of relevant process,
- name or code number of station at which it is used,
- lot identification,
- dates recorded,
- number of items inspected,
- identification of equipment adjustment,
- percentage of defective devices,
- average nominal values,
- average limits.

2.8.1.4 Process documentation

The manufacturer shall prepare and maintain documents for incoming inspection, production, quality assurance and process control such as specifications and procedures establishing:
- materials and piece parts,
- operations,
- equipment,
- calibration methods,
- measurements,
- tests,
- inspections,
- tolerances.

The relevant issues (and only those issues) of the process documents shall be available at all times to operating personnel and, upon request, shown to the evaluating and qualifying authority.

2.8.2 Traceability

The manufacturer shall record the manufacturing data and material history of all units processed according to this specification and maintain these records for a minimum of five years. These records shall be traceable to the serial numbers of the individual hybrid circuits delivered.

2.9 LOCATION OF PROCESSING AREAS

The manufacturer shall specify the location at which each of the key processing steps is performed. The evaluating authority shall be notified of any changes in these locations to determine whether re-evaluation is required.

2.10 WORK AREAS

2.10.1 General requirements

The subject devices shall be produced in a controlled area. This implies that:
- only authorised personnel shall have access to such area and that within such area:
  . personnel shall wear protective clothing,
  . smoking, drinking and eating shall be prohibited,
  . housekeeping shall be according to a written schedule,
  . equipment shall be compatible with the cleanliness standard required in the controlled area,
  . atmospheric pressure differences shall be used to maintain the required standards of cleanliness.

2.10.2 Environmental control

The manufacturer shall specify for each process step:
- temperature,
- relative humidity,
- particle count.

He shall demonstrate the manner in which these conditions are controlled, taking into account the relevant requirements defined in Table 1 and Specification ESA PSS-01-201.

2.11 HANDLING OF HYBRID INTEGRATED CIRCUITS

The manufacturer shall furnish evidence that adequate provisions are in force for the careful handling and storage of microwave circuits throughout the production cycle. Any damage shall be recorded together with details of the station and/or stage of operation at which the damage occurred.

2.12 PURITY OF MATERIALS

The manufacturer shall keep records to verify that the materials used in production are of a consistent level and meet the application requirements.

Table 1 ENVIRONMENTAL REQUIREMENTS

Process step	Cleanliness Class	Humidity (% RH)	Temperature (°C)
Cutting of masters (if used).	100 000	50 ± 5	To be specified by manufacturer
Photoreduction, -plotting and manufacture of production masks.	100	50 ± 5	ditto
Photoresist preparation, -application, -drying, including pattern exposure and development processes.	100	50 ± 5	ditto
Etching and cleaning processes.	100	50 ± 5	ditto
Attachment of encapsulated or unencapsulated passive components and encapsulated semiconductor components. Attachment of substrates to baseframes, -plates or -structures; including flux removal and cleaning processes	100 000	to be specified by manufacturer	ditto
Final cleaning attachment of unencapsulated semiconductor components, mounting of substrate into hermetic package. Also includes possible burn-in, precap, visual inspection and other control processes before final sealing.	100	ditto	ditto
Mounting of component-equipped structures into non-hermetic packages; including cleaning after mounting.	10 000	ditto	ditto
Packaging of finished product into sealed plastic bag.	10 000	50 ± 5	ditto

SECTION 3: EVALUATION PHASE

3.1 GENERAL

The Evaluation Phase shall consist of:

(a) *Capability Survey*
This survey is made to assess a manufacturer's general capability in the production of reliable circuits.

(b) *Line Survey*
This survey consists of an analysis of a manufacturer's technology and production line based on applied processes and controls and a detailed study of all available test data for the identification of critical processes and controls.

(c) *Evaluation Testing*
This involves the selection, production and testing of test structures for determination of their stress limits and weaknesses.

(d) *Corrective Actions*
If, as a result of evaluation testing, the test structures show weaknesses or deficiencies, the manufacturer shall take any corrective actions required by ESA.

(e) *ESA Approved Capability Domain*
After all required corrective actions have been implemented to the full satisfaction of ESA, ESA will approve the manufacturer's capability domain as defined in the PID at the end of this phase. This approval will enable the manufacturer to start the next phase of the programme.

3.2 EVALUATION TESTING

Evaluation testing shall comprise four sequential steps, viz.:

(a) Selection of techniques, processes and materials to be certified;
(b) Based on the selection specified under (a) above, manufacture of test structures or circuits;
(c) Testing of test structures or circuits;
(d) Evaluation of test results.

3.2.1 Selection of techniques

On the basis of processes, materials and techniques proposed by the manufacturer for approval, the manufacturer shall propose the main techniques and types of encapsulation, define the test structures and draw up the test plans in accordance with the requirements of this specification.

Tables 2 and 3 show the possible main techniques and encapsulation or mounting methods respectively. Only certain combinations of main techniques and encapsulation or mounting methods shall be permitted; these are shown in Table 4 together with the type designations of the corresponding test structures. In determining the need for hermeticity, it is mandatory that all active devices shall be hermetically encapsulated either at module level by the use of a hermetically sealed enclosure or at device level by the use of a hermetic package.

The manufacturer shall be free to choose which of the different subtechniques applicable to a specific main technique he wishes to use. However, the layout and content of the corresponding test structure shall be agreed with ESA. The selection shall be made before commencing manufacture of the test structures. Table 5 lists the various subtechniques.

The manufacturer shall draw up a list of processes and select the raw materials, piece parts and added-on or applied materials, and ascertain their conformance to the design, quality and procurement requirements defined in this specification and ESA Specifications PSS-01-60, PSS-01-70 and PSS-01-608, as relevant. Alternatively, he shall prove their suitability for space application by other documentary evidence.

Each process step shall be chosen solely on the basis of the materials, techniques and controls applied at the time of evaluation. A preliminary Process Identification Document (PID) shall be prepared for the processes and procedures to be applied. The PID shall list all constituent materials and piece parts.

The manufacturer shall ensure that all materials and processes for which certification is sought are adequately covered by the programme. Prior to its implementation, this programme shall be submitted to ESA for approval.

Table 2 MAIN TECHNIQUES

A	Single-layer conductor, 0.1 W per cm^2 or less of substrate area. Terminal current less than 0.5 A. with or without attached components.
B	Single-layer resistor and conductor, 0.1 W per cm^2 or less of substrate area. Terminal current less than 0.5 A. With or without attached components.
C	Single-layer conductor with barrier layer, 0.2 W per cm^2 or less of substrate area. Terminal current less than 2.0 A. With or without attached component.
D	Single-layer resistor and conductor with barrier layer, 0.2 W per cm^2 or less of substrate area. Terminal current less than 2.0 A. With or without attached components.

Table 3 MOUNTING AND ENCAPSULATION

Q	Unencapsulated and unmounted substrate
R	Substrates attached to mounting plate
S	Substrates mounted in hermetically sealed metal enclosure
T	Substrates attached to mounting plate and assembled in hermetically sealed metal enclosure
U	Substrates mounted in nonhermetic enclosure
V	Substrates attached to mounting plate in non hermetic enclosure

Table 4 PERMITTED COMBINATIONS OF MAIN TECHNIQUES AND MOUNTING OR ENCAPSULATION METHODS FOR DEFINITION OF TEST STRUCTURES

	MOUNTING OR ENCAPSULATION					
Main technique	Q	R	S	T	U	V
A	QA1 and QA2	RA1 and RA2	SA 1	TA1	UA1	VA1
B	QB1 and QB2	RB1 and RB2	SB1	TB1	UB1	VB1
C	QC1 and QC2	RC1 and RC2	SC1	TC1	UC1	VC1
D	QD1 and QD2	RD1 and RD2	SD1	TD1	UD1	VD1

Example

SB1 is a type B1 test substrate (covering single-layer thin-film resistor and conductors with components attached) attached to a mounting plate.

Definition of Main Technique: See Table 2.

Definition of Mounting and Encapsulation Methods Q to V: See Table 3.

Definition of Test Substrates A1 to D2: See Table 6.

Table 5 - SUBTECHNIQUES

I	Single-layer conductor
II	Single-layer conductor and resistor
III	Single-layer conductor with barrier layer
VI	Single-layer conductor with barrier layer and resistor
V	Substrate hole drilling and profiling
VI	Protective covering
VII	Substrate attachment to mounting plate
VIII	Chip and wire bonding
IX	Attachment of passive component chips
X	Crossover by wire bonding
XI	Beam lead chip attachment
XII	Attachment of encapsulated components
XIII	RF grounding of substrates
XiV	Connection to substrates
XV	Interconnection of substrates
XVI	Post-assembly tuning
XVII	Substrate mounting into enclosure
XVIII	Mounting plate attachment into enclosure
XIX	RF and DC connector mounting into enclosure
XX	Microwave absorbers
XXI	Enclosure sealing

3.2.2. Sequence of operations for selection, manufacture and testing of test structures

(a) The manufacturer shall propose and submit to ESA for approval those processes that he wishes to adopt.
(b) Joint agreement by ESA and the manufacturer on sub-techniques (see Table 5).
(c) Joint agreement by ESA and the manufacturer on main techniques and mounting or encapsulation methods.
(d) Preparation by the manufacturer of the applicable documentation and layouts of test structures.
(e) Manufacture and testing of test structures, preparation of report.
(f) ESA may require that it or its representative monitor certain tests.
(g) Destructive Physical Analysis (DPA) of control devices by ESA or an independent test laboratory.

3.2.3 Test structures for line evaluation

The test structures to be manufactured shall:
- be based on the processes selected,
- be such that they are representative of the technology involved,
- be in accordance with the controls, limits and constaints agreed between ESA and the manufacturer,
- meet the requirements of this specification,
- be tested for any weakness, so that restraints of the applied processes and technologies may be determined, and
- take into account any inherent criticalities.

3.2.4 Test structures and applicable test programmes

Table 6 specifies the test substrates to be used in the manufacture of the different test structures and refers to the Paragraphs in which details are described.

Table 7 shows type designations and numbers of test structures to be manufactured for evaluation testing together with the applicable test plans as per Paragraph 3.2.6.

Table 6 TEST STRUCTURES AND PROCEDURES

SUB-STRATE	DESCRIPTION	PARA.
A1	Substrate for microwave circuit with one-layer conductor pattern	3.2.5.1
A2	Substrate for component attachment with one-layer conductor pattern	3.2.5.1
B1	Substrate for microwave circuit with on-layer resistor and one layer conductor pattern	3.2.5.2
B2	Substrate for component attachment with one-layer resistor and one layer conductor pattern	3.2.5.2
C1	Substrate for microwave circuit with one-layer conductor pattern and barrier layer	3.2.5.3
C2	Substrate for component attachment with one-layer conductor pattern and barrier layer	3.2.5.3
D1	Substrate for microwave circuit with one-layer resistor, one-layer conductor pattern and barrier layer	3.2.5.4
D2	Substrate for component attachment with one-layer resistor, one-layer conductor pattern and barrier layer	3.2.5.4

Table 7 TYPE DESIGNATIONS AND NUMBERS OF TEST STRUCTURES TO BE MANUFACTURED AND APPLICABLE TEST PLANS

Description	Test structure	No. of pieces.to be manufactered	Test plan no.	Example
Microwave circuit, 1-layer conductors with attached components, unencapsulated	QA1	21	1	Mounting or encapsulation definition; see Table 3 ↓ R A1 ↑ Substrate type definition; see Table 6
Substrate, 1-layer conductors with attached components, unencapsulated.	QA2	21	1	
Microwave circuit, 1-layer conductors with attached components on mounting plate.	RA1	21	1	
Substrate, 1-layer conductors with attached components on mounting plate.	RA2	21	1	
Microwave circuit, 1-layer conductor with attached components in hermetic enclosure.	SA 1	13	2	
Microwave circuit, 1-layer conductors with attached components in nonhermetic enclosure	UA1	13	4	
Microwave circuit, 1-layer conductors with attached components on mounting plate in hermetic enclosure.	TA1	13	2	
Microwave circuit, 1-layer conductors with attached components on mounting plate in nonhermetic enclosure.	VA1	13	4	
Microwave circuit, 1-layer resistors and conductors with attached components, unencapsulated.	QB1	21	1	
Substrate, 1-layer resistors and conductors with attached components unencapsulated.	QB2	21	1	

Table7 -TYPE DESIGNATIONS AND NUMBERS OF TEST STRUCTURES TO BE MANUFACTURED AND APPLICABLE TEST PLANS (continued)

Description	Test structure	No. of pieces to. be manufactured	Test plan no.	Example
Microwave circuit, 1-layer resistors and conductors with attached components on mounting plate.	RB1	21	1	Mounting or encapsulation definition; see Table 3 ↓ R A1 ↑ Substrate type definition; see Table 6
Substrate, 1-layer resistors and conductors with attached components on mounting plate	RB2	21	1	
Microwave circuit, 1-layer resistors and conductors with attached components in hermetic enclosure.	SB1	13	2	
Microwave circuit, 1-layer resistors and conductors with attached components in nonhermetic enclosure.	UB1	13	4	
Microwave circuit, 1-layer resistors and conductors with attached components on mounting plate in hermetic enclosure	TB1	13	2	
Microwave circuit, 1-layer resistors and conductors with attached components on mounting plate in non hermetic enclosure.	VB1	13	4	
Microwave circuit, 1-layer conductors and barrier layer with attached components, unencapsulated.	QC1	26	3	
Substrate, 1-layer conductors and barrier layer with attached components, unencapsulated.	QC2	26	3	

Table 7 TYPE DESIGNATIONS AND NUMBERS OF TEST STRUCTURES TO BE MANUFACTURED AND APPLICABLE TEST PLANS (continued)

Description	Test structure	No. of pieces to be manufactured	Test plan no.	Example
Microwave circuit, 1-layer conductors and barrier layers with attached components on mounting plate.	RC1	26	3	
Substrate, 1 -ayer conductor and barrier layer with attached components on mounting plate	RC2	26	3	
Microwave circuit, 1-layer conductors and barrier layer with attached components in hermetic enclosure.	SC1	13	2	Mounting or encapsulation definition; see Table 3
Microwave circuit, 1-layer conductors and barrier layer with attached components in non hermetic enclosure.	UC1	13	4	
Microwave circuit, 1-layer conductors and barrier layer with attached components on mounting plate in nonhermetic enclosure.	TC1	13	2	R A1
Microwave circuit, 1-layer conductors and barrier layer with attached components on mounting plate in non hermetic enclosure.	VC1	13	4	Substrate type definition; see Table 6
Microwave circuit, 1-layer resistors and conductors with barrier layer with attached components, unencapsulated.	QD1	26	3	
Substrate, 1-layer resistors and conductors with barrier layer with attached components, unencapsulated.	QD2	26	3	

Table 7 TYPE DESIGNATIONS AND NUMBERS OF TEST STRUCTURES TO BE MANUFACTURED AND APPLICABLE TEST PLANS (continued)

Description	Test structure	No. of pieces to be manufactured	Test plan no.	Example
Microwave circuit, 1-layer resistors and conductors with barrier layer with attached components on mounting plate.	RD1	26	3	Mounting or encapsulation definition; see Table 3 ↓ R A1 ↑ Substrate type definition; see Table 6
Substrate, 1-layer resistors and conductors with barrier layer with attached components on mounting plate.	RD2	26	3	
Microwave circuit, 1-layer resistors and conductors with barrier layer with attached components in hermetic enclosure.	SD1	13	2	
Microwave circuit, 1-layer resistors and conductors with attached components in nonhermetic enclosure.	UD1	13	4	
Microwave circuit, 1-layer resistors and conductors with barrier layer with attached components on mounting plate in hermetic enclosure.	TD1	13	2	
Microwave circuit, 1-layer resistors and conductors with barrier layer with attached components in nonhermetic enclosure.	VD1	13	4	

3.2.5 Description and layout of test substrates

Paragraphs 3.2.5.1. to 3.2.5.4. describe the layout of test substrates A, B, C and D. As a guideline, the test structures described and illustrated in these paragraphs have been implemented on 25.4 x 50.8 mm substrates. The manufacturer shall, however, use the maximum substrate size included in his capability.

In general, each test substrate shall contain a series of test patterns for evaluating photo-engraving, plating and etching quality. After scribing, part of the substrate shall be used in a functional microwave circuit and another as a vehicle for assessment of add-on component attachment. Depending on the technology, the assembled substrates may be unencapsulated or attached to a mounting plate for evaluation testing. Microwave functional circuits either unencapsulated or attached to mounting plates shall be assembled for evaluation testing into hermetic or nonhermetic enclosures (depending on the technology being approved).

This concept, which is identical for each microwave substrate is illustrated in Figure 1 for Test Substrate A.

In this example, two microwave functional circuit patterns, A1 and two add-on component assessment patterns, A2 have been incorporated on a single substrate.

The full substrate is used for evaluating conductor pattern quality and registration. Assessment of component attachment on either unmounted and unencapsulated substrates, QA1 and QA2, or substrates attached to mounting plates, RA1 and RA2, is then carried out. QA1 and QA2 (or RA1 and RA2) shall include the range of add-on components and assembly subtechniques required to be included within the capability (see Table 5). Microwave assessment shall be carried out on QA1 (or RA1).

The functional microwave circuit shall be assembled into a metal hermetic enclosure, SA1 or TA1 or nonhermetic metal enclosure (UA1 or VA1) for evaluation, including microwave assessment.

Any commercially available added-on parts required for assembly shall be as far as possible equivalent to space-qualified parts.

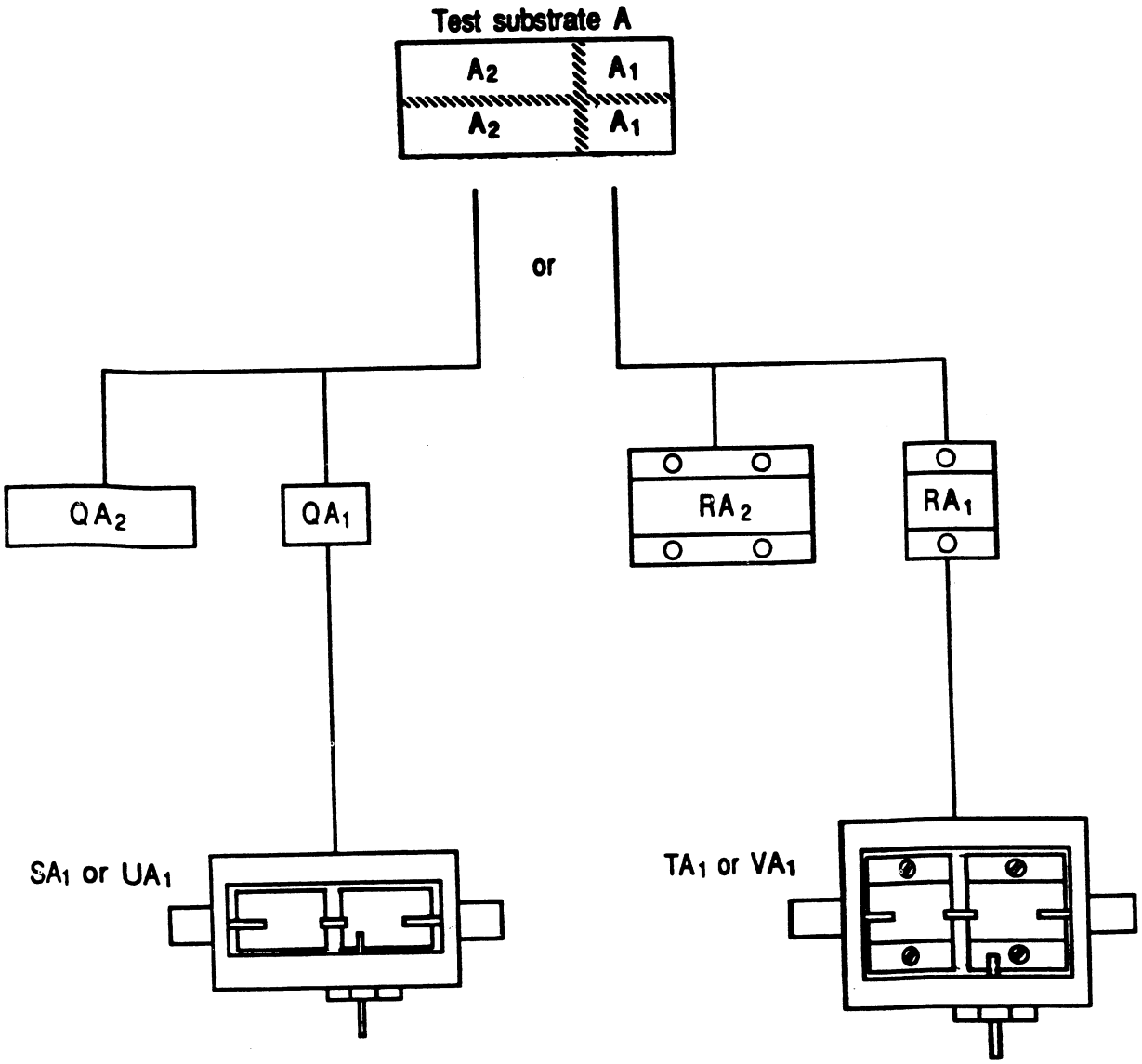

Figure 1. EXAMPLE OF TEST STRUCTURE FLOW CHART.

3.2.5.1 Test structures A1 and A2 for microwave hybrid integrated circuits with thin-film conductors

Test substrate A, which is subdivided into Test Structures A1 and A2, is illustrated in Figure 2 and is designed to evaluate the photoengraving, plating and etching quality of microwave circuits with thin-film conductors as well as the attachment of a range of add-on components. After scribing, Test Structure A1 is designed to perform as a functional microwave circuit. Test Structure A2 is designed for the attachment of a range of add-on components.

Figure 2 is an example of one realisation of the test substrate. The manufacturer shall design the layout applicable to his own technology and capability requirements.

Features assessed by means of Test Substrate A prior to scribing are:
- conductor thickness
- backface metallisation thickness
- registration of pattern to substrate
- conductor adhesion
- minimum conductor width
- minimum conductor-to-conductor spacing

Features assessed by means of Test Structures A1 and A2 either unencapsulated or attached to a mounting plate are:
- profiling of substrates
- hole drilling in substrates
- attachment to mounting plate
- provision of RF ground to top face of substrate
- assembly of largest and smallest chip capacitor (for each style)
- assembly of largest and smallest chip resistor (for each style)
- assembly of maximum dissipation conductor
- assembly of maximum pin count semiconductor
- maximum current density in conductor (endurance test)
- wire bond pull strength
- die bond shear strength

Features assessed by means of Test Structure A1 when assembled into a metal enclosure either directly or on a mounting plate are:
- either attachment of substrate or attachment of mounting plate to enclosure base
- attachment of DC and RF connectors to enclosure
- RF and DC connection to substrate
- RF interconnection of substrates
- post-assembly tuning techniques
- maximum enclosure dimensions

In addition, for a hermetic enclosure the following features are to be assessed:
- maximum seal periphery
- enclosure hermeticity

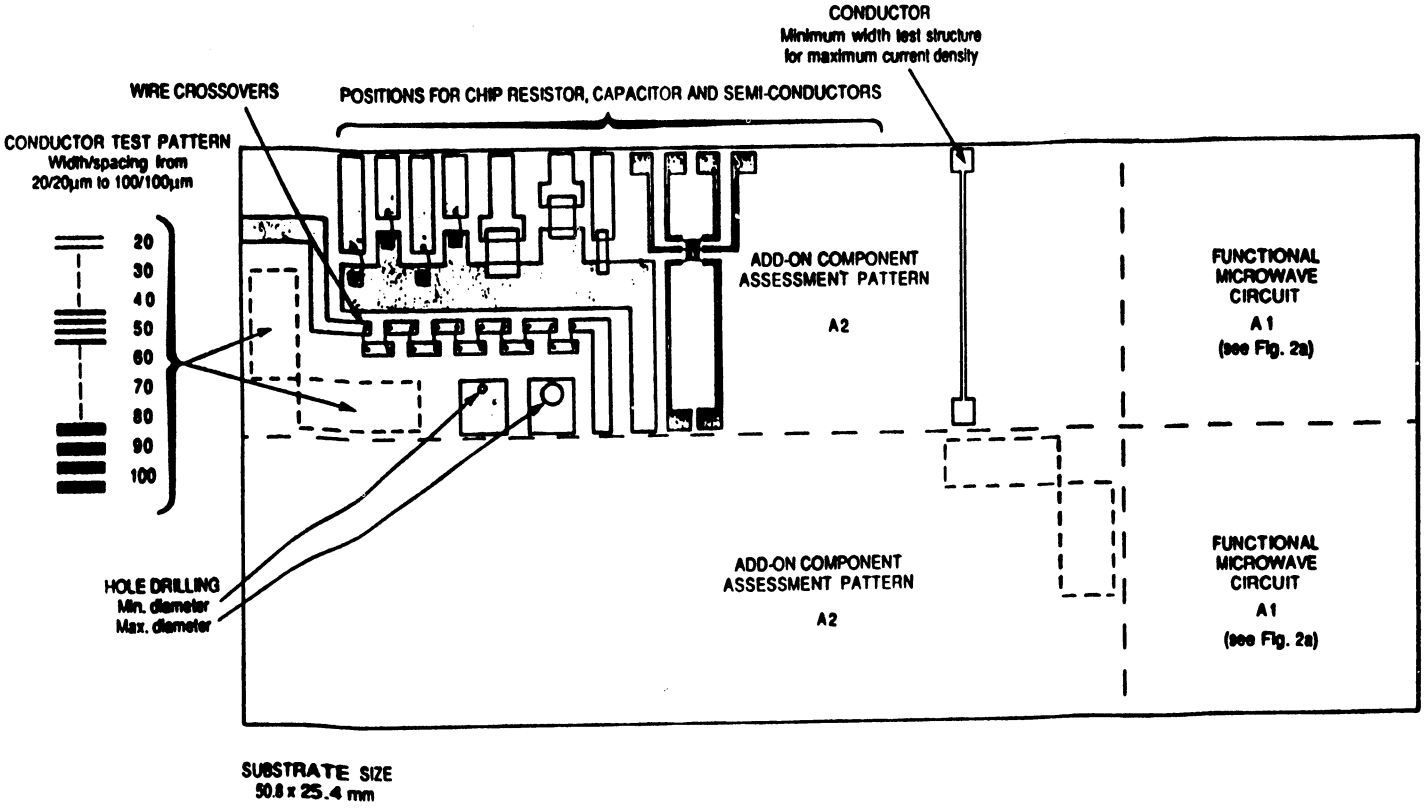

Figure 2. TEST SUBSTRATE A

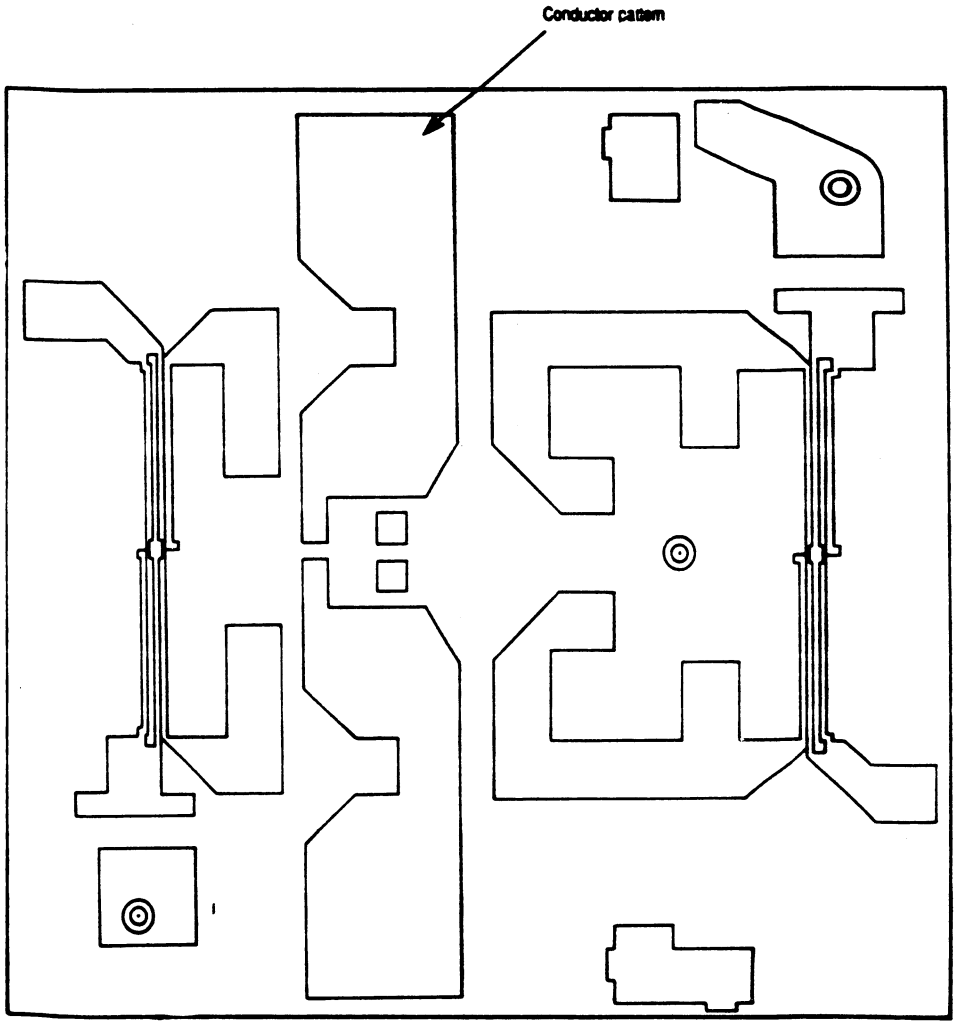

Figure 2A. EXAMPLE OF A FUNCTIONAL MICROWAVE CIRCUIT USING MAIN TECHNIQUE A.

3.2.5.2 Test structures B1 and B2 for microwave hybrid integrated circuits with thin-film resistors and conductors

Test Substrate B, which is sub-divided into Test Structures B1 and B2, is illustrated in Figure 3 and is designed to evaluate the photo-engraving, plating and etching quality of microwave circuits with thin-film resistors and conductors as well as the attachment of a range of add-on components. Test Structure B1 is designed to perform as a functional circuit after scribing. Test Structure B2 is designed for attachment of a range of add-on components.

Figure 3 shows an example of one realisation of the test substrate. The manufacturer shall design the layout applicable to his own technology and capability requirements.

Features assessed by means of Test Substrate B prior to scribing are:
- conductor thickness
- backface metallisation thickness
- registration of pattern to substrate
- conductor adhesion
- minimum conductor width
- minimum conductor-to-conductor spacing
- minimum and maximum resistor aspect ratio

Features assessed by means of Test Structures B1 and B2 either unencapsulated or attached to a mounting plate are:
- profiling of substrates
- hole drilling of substrates
- attachment to mounting plate
- provision of RF ground to top face of substrate assembly of largest and small chip capacitor (for each style)
- assembly of largest and small chip resistor (for each style)
- assembly of maximum dissipation semiconductor
- assembly of maximum pin-count semiconductor
- maximum current density in conductor (endurance test)
- maximum dissipation in thin-film resistor (endurance tests)
- wire bond pull strength
- die bond shear strength

Features assessed by means of Test Structure B1 when assembled into a metal enclosure either directly or on a mounting plate are:
- either attachment of substrate or attachment of mounting plate to enclosure base
- attachment of DC and RF connectors to enclosure
- RF and DC connection to substrate
- RF interconnection of substrates

- post-assembly tuning techniques
- maximum enclosure dimensions

In addition, for a hermetic enclosure the following features are to be assessed:
- maximum seal periphery
- enclosure hermeticity

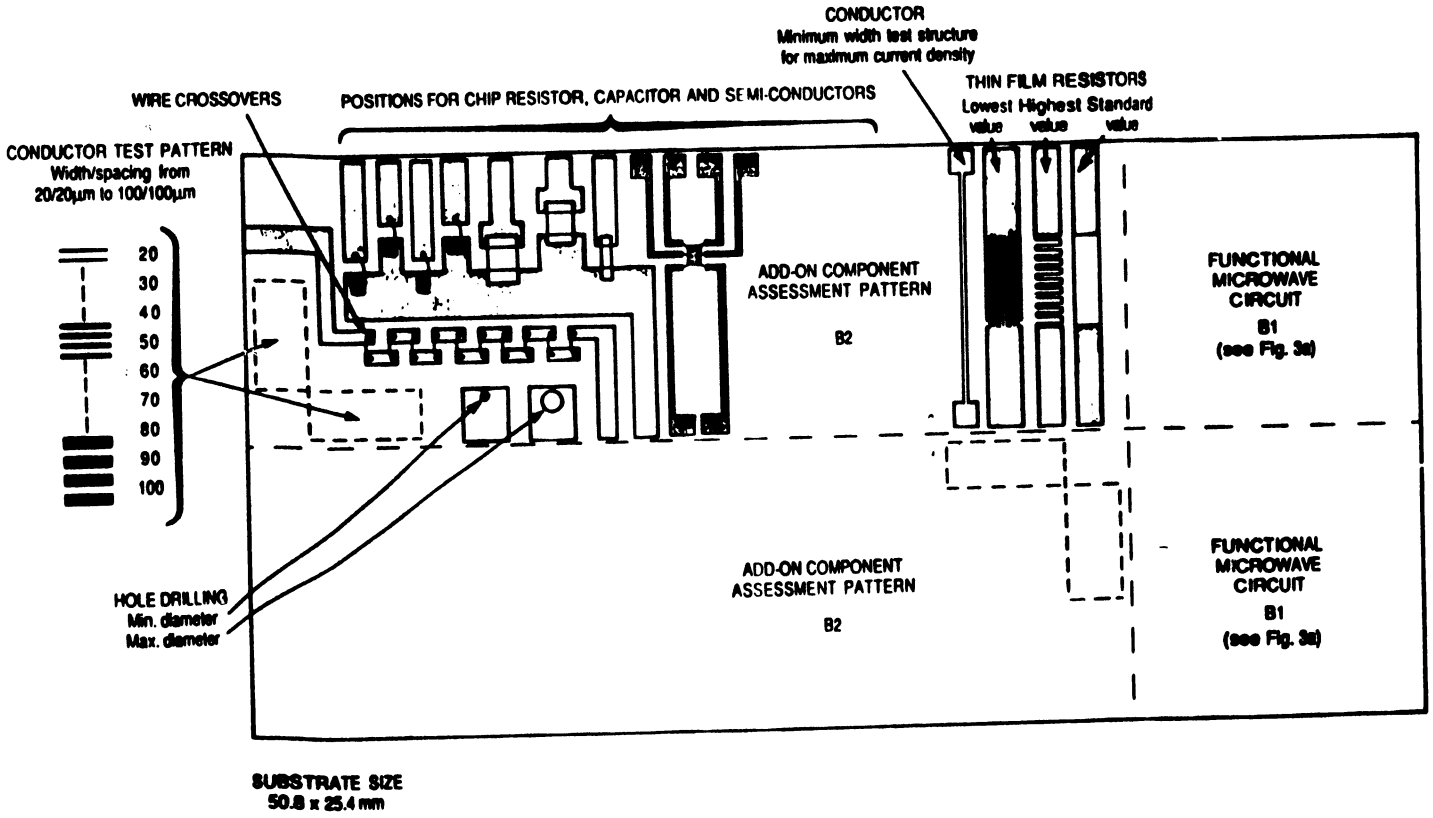

Figure 3. TEST SUBSTRATE B.

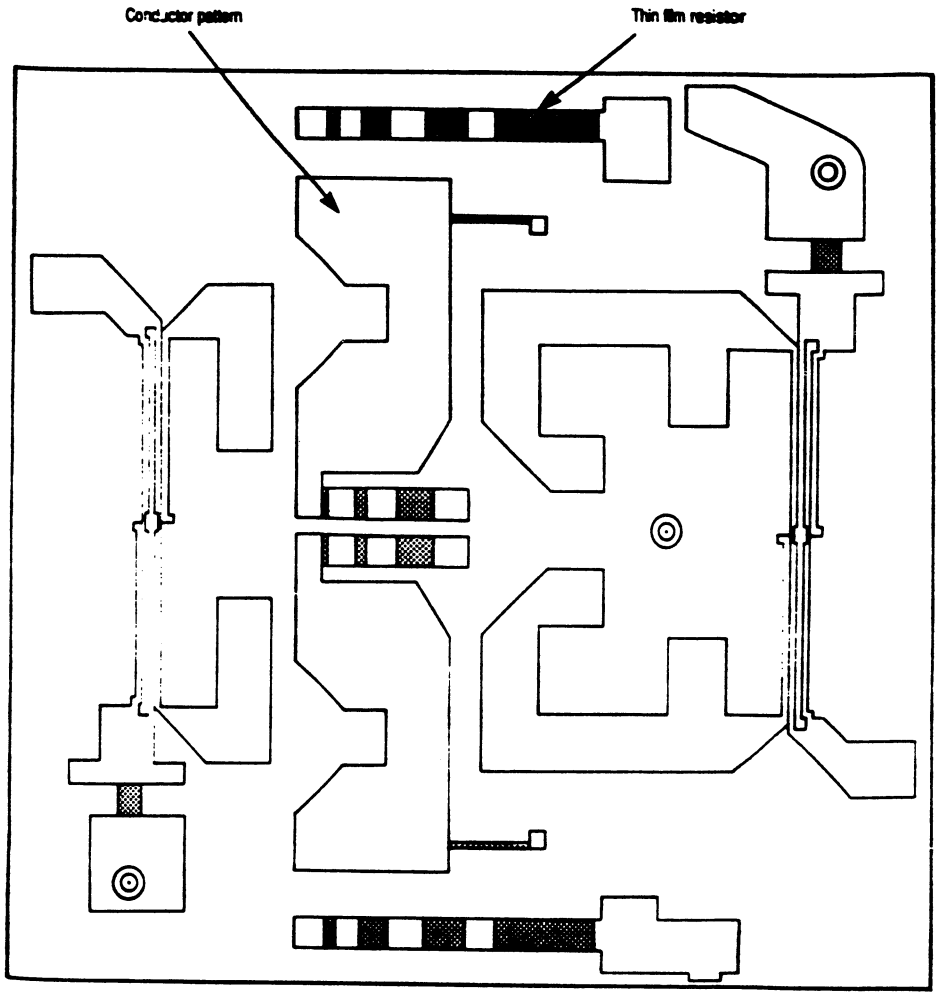

Figure 3A. EXAMPLE OF A FUNCTIONAL MICROWAVE CIRCUIT USING MAIN TECHNIQUE B

3.2.5.3 Test structures C1 and C2 for microwave hybrid integrated circuits with thin-film conductors and barrier layers

Test substrate C which is subdivided into Test Structures C1 and C2 is illustrated in Figure 4 and is designed to evaluate the photo-engraving, plating and etching quality of microwave circuits with thin-film conductors and barrier layers as well as the attachment of a range of add-on components. Test Structure C1 is designed to perform as a functional microwave circuit after scribing. Test Structure C2 is designed for the attachment of a range of add-on components.

Figure 4 illustrates an example of one realisation of the test substrate. The manufacturer shall design the layout applicable to his own technology and capability requirements.

Features demonstrated by means of Test Substrate C prior to scribing are:

- conductor thickness
- backface metallisation thickness
- registration of pattern to substrate
- registration of barrier layer to conductor pattern
- conductor adhesion
- barrier layer adhesion
- minimum conductor width
- minimum conductor-to-conductor spacing

Features assessed by means of Test Structures C1 and C3 either unencapsulated or attached to a mounting plate are:

- hole drilling of substrates
- attachment of mounting plate
- provision of RF ground to top face of substrate
- assembly of largest and smallest chip capacitor (for each style)
- assembly of largest and smallest chip resistor (for each style)
- assembly of maximum dissipation semiconductor
- assembly of maximum pin-count semiconductor
- maximum current density in conductor (endurance test)
- wire bond pull strength
- die bond shear strength

Features assessed by means of Test Structure C1 when assembled into a metal hermetic enclosure either directory or on a mounting plate are:

- either attachment of substrate or attachment of mounting plate to enclosure base
- attachment of DC and RF connectors to enclosure
- RF and DC connection to substrate

- RF interconnection of substrates
- post-assembly tuning techniques
- maximum enclosure dimensions

In addition, for a hermetic enclosure the following features are to be assessed:
- maximum seal periphery
- enclosure hermeticity

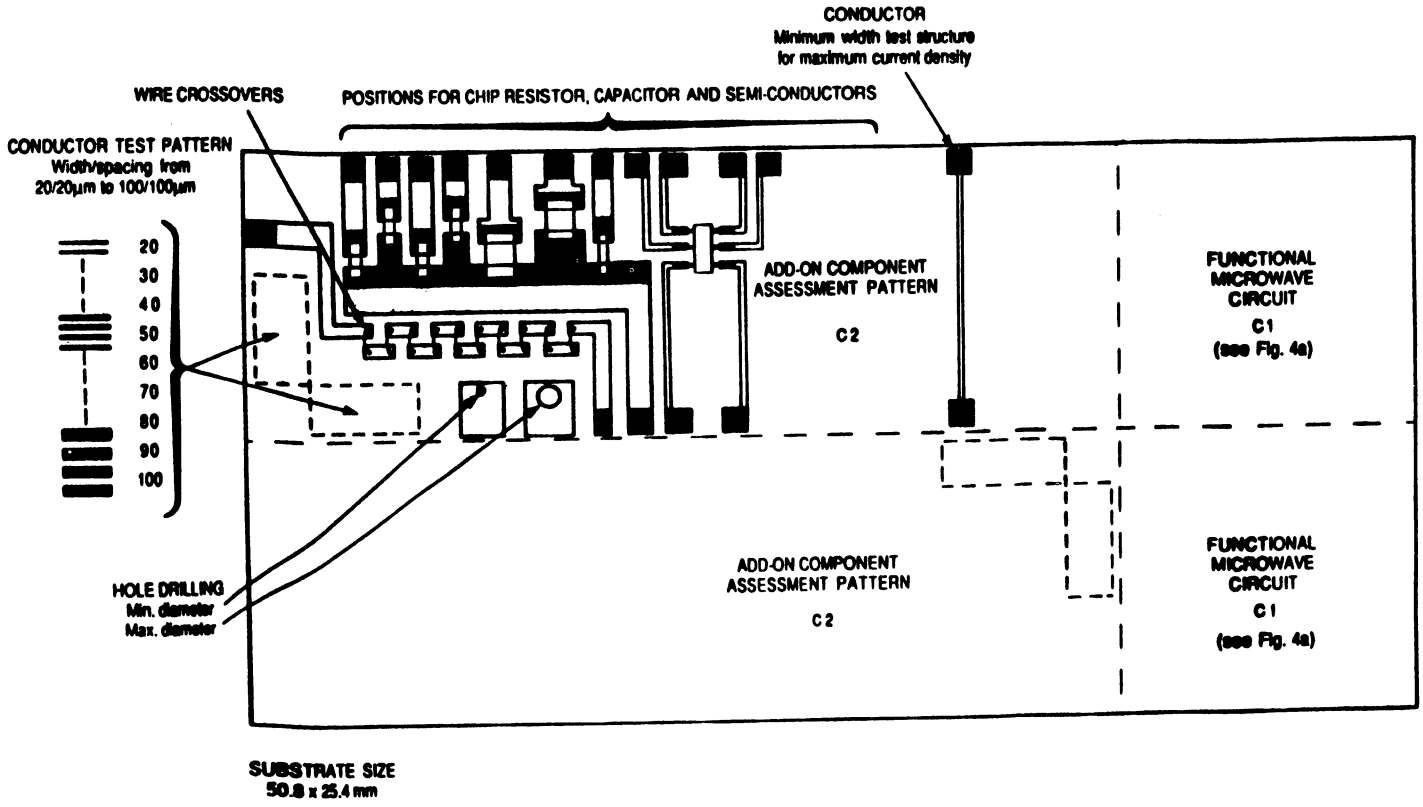

Figure 4. TEST SUBSTRATE C

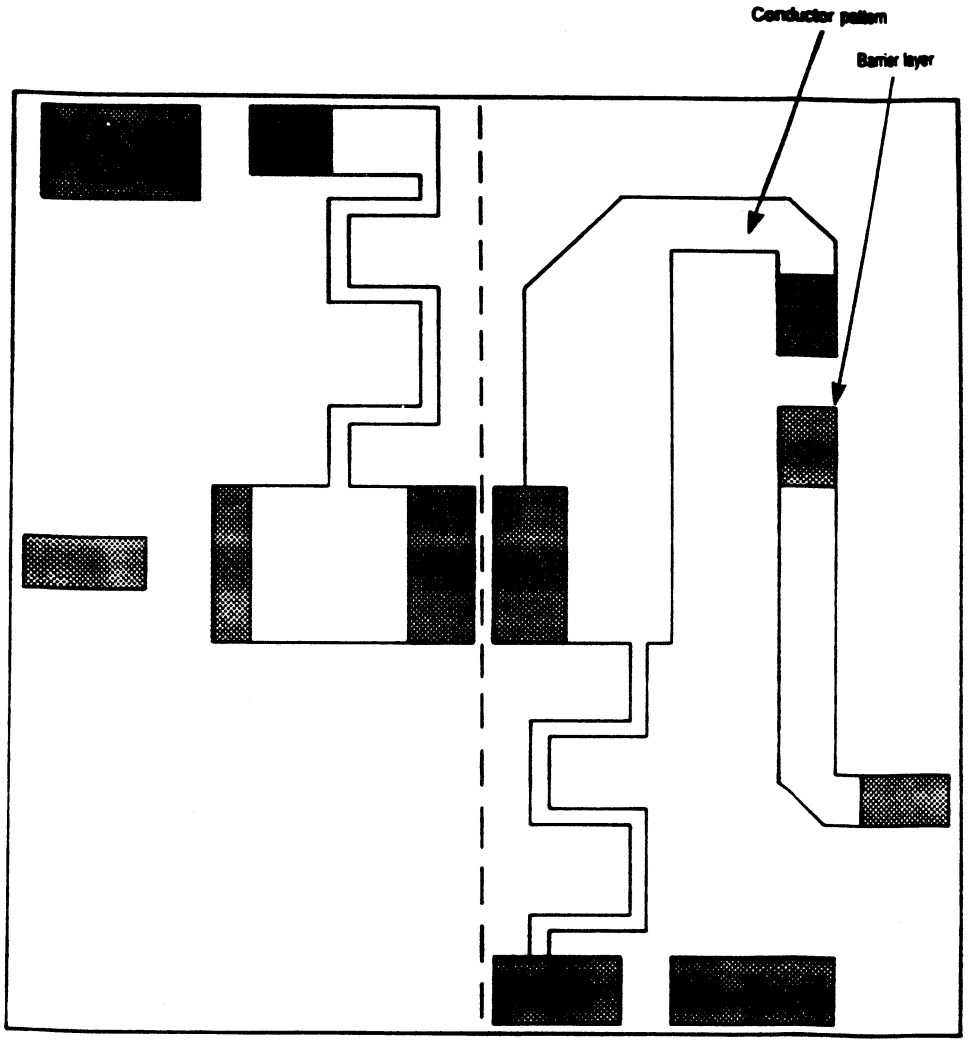

Figure 4A. EXAMPLE OF A FUNCTIONAL MICROWAVE CIRCUIT USING MAIN TECHNIQUE C

3.2.5.4 Test structures D1 and D2 for microwave hybrid integrated circuits with thin-film resistors and conductors with barrier layers

Test Substrate D which is subdivided into Test Structures D1 and D2 is illustrated in Figure 5 and is designed to evaluate the photo-engraving, plating and etching quality of microwave circuits with thin-film resistors and conductors as well as the attachment of a range of add-on components. Test Structure D1 is designed to perform as a functional microwave circuit after scribing. Test Structure D2 is designed for attachment of a range of add-on components.

Figure 5 shows an example of one realisation of the test substrate. The manufacturer shall design the layout applicable to his own technology and capability requirements.

Features assessed by means of Test Substrate D prior to scribing are:

- conductor thickness
- backface metallisation thickness
- registration of pattern to substrate
- conductor adhesion
- minimum conductor width
- minimum conductor-to-conductor spacing
- minimum and maximum resistor aspect ratio

Features assessed by means of Test Structures D1 and D2 either unencapsulated or attached to a mounting plate are:

- profiling of substrates
- hole driiling of substrates
- attachment to mounting plate
- provision of RF ground to top face of substrate
- assembly of largest and smallest chip capacitor (for each style)
- assembly of largest and smallest chip resistor (for each style)
- assembly of maximum dissipation semiconductor
- assembly of maximum pin-count semiconductor
- maximum current density in conductor (endurance test)
- maximum dissipation in thin-film resistor (endurance test)
- wire bond pull strength
- die bond shear strength

Features assessed by means of Test Structure D1 when assembled into a metal enclosure either directly or on a mounting plate are:

- either attachment of substrate or attachment of mounting plate to enclosure base
- attachment of DC and RF connectors to enclosure
- RF and DC connection to substrate
- RF interconnection of substrates

- post-assembly tuning techniques
- maximum enclosure dimensions

In addition, for a hermetic enclosure the following features are to be assessed:
- maximum seal periphery
- enclosure hermeticity

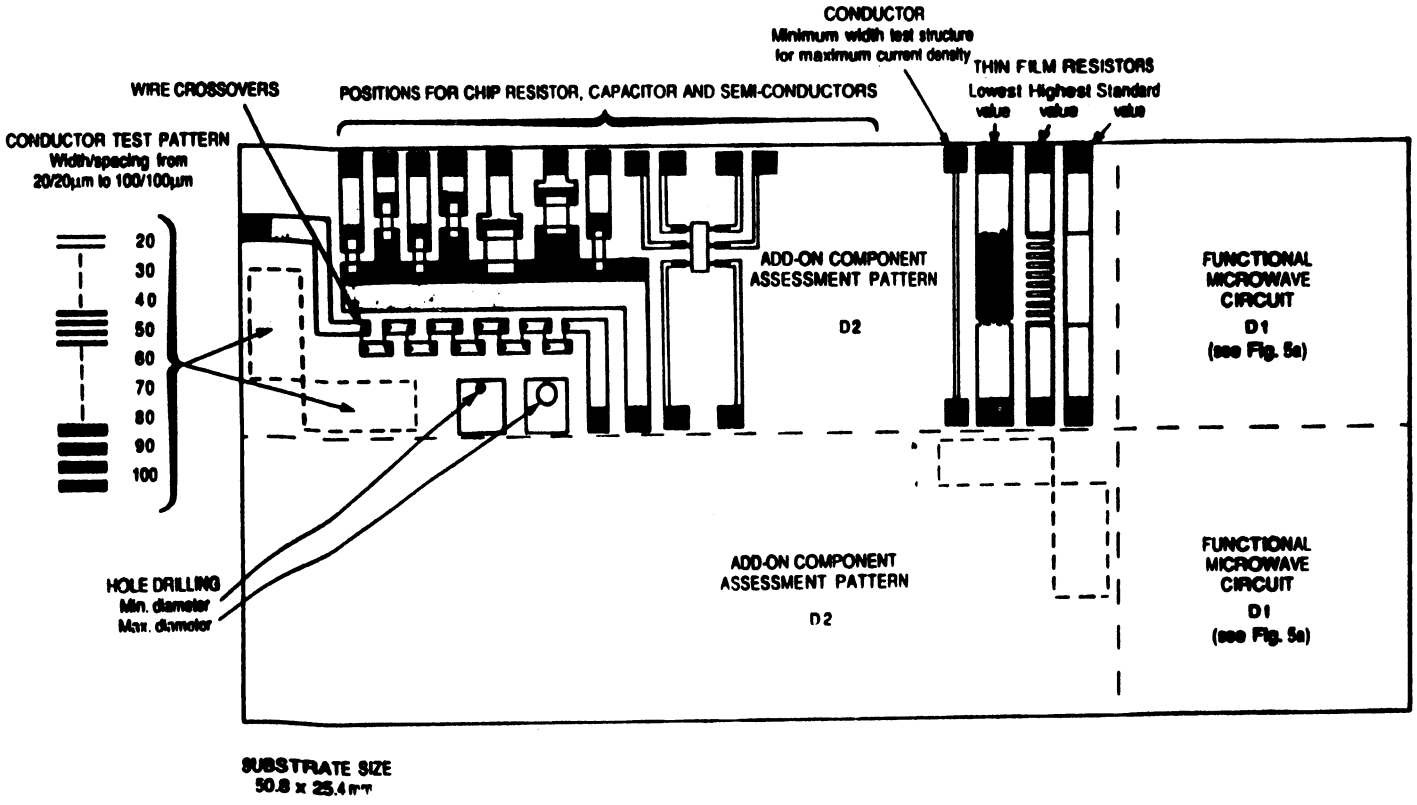

Figure 5. TEST SUBSTRATE D

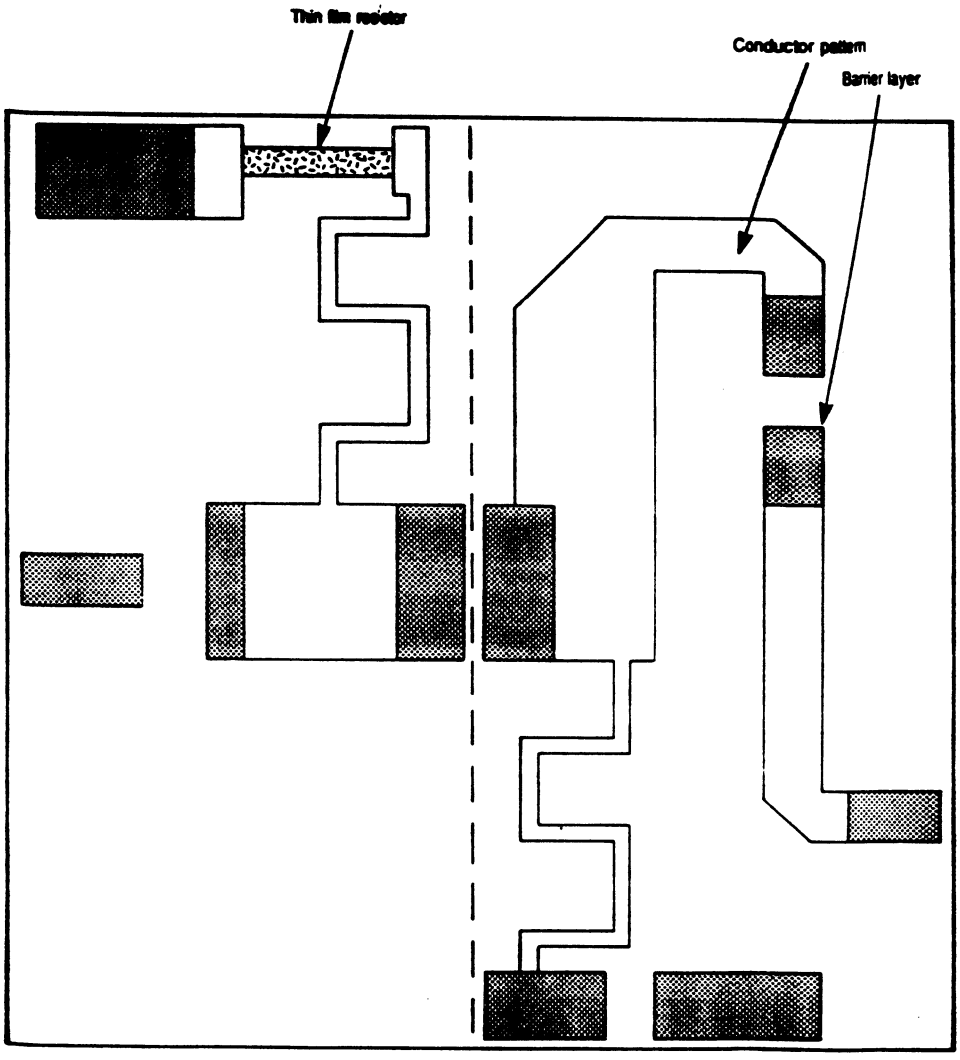

Figure 5A. EXAMPLE OF A FUNCTIONAL MICROWAVE CIRCUIT USING MAIN TECHNIQUE D

3.2.6 Evaluation test plans

Testing, analysis of test results and presentation of the evaluation test programme shall be in accordance with the test plan and tables specified herein for each test structure. All structures and devices submitted for testing shall be clearly identified by serial numbers.

Upon completion of testing, all devices, test and inspection results, including a summary of all failure analysis results, shall be submitted to ESA. All measurements shall be recorded.

The reference devices mentioned in the test plan shall serve as control devices to measure the electrical/mechanical characteristics of the test samples.

If termination and/or area identification numbers differ from those referenced in this specification, the manufacturer shall provide ESA with a cross-reference table.

The following test plans are applicable to the test structures specified in Table 7 and Paragraph 3.2.4.

NOTE: For MHICs incorporating certain microwave absorbers (see ESA PSS-01-610), outgassing at high temperature may be a problem. If, therefore, it is necessary to restrict the maximum temperature of operation of such circuits, this must be agreed with ESA and detailed in the appropriate test plans.

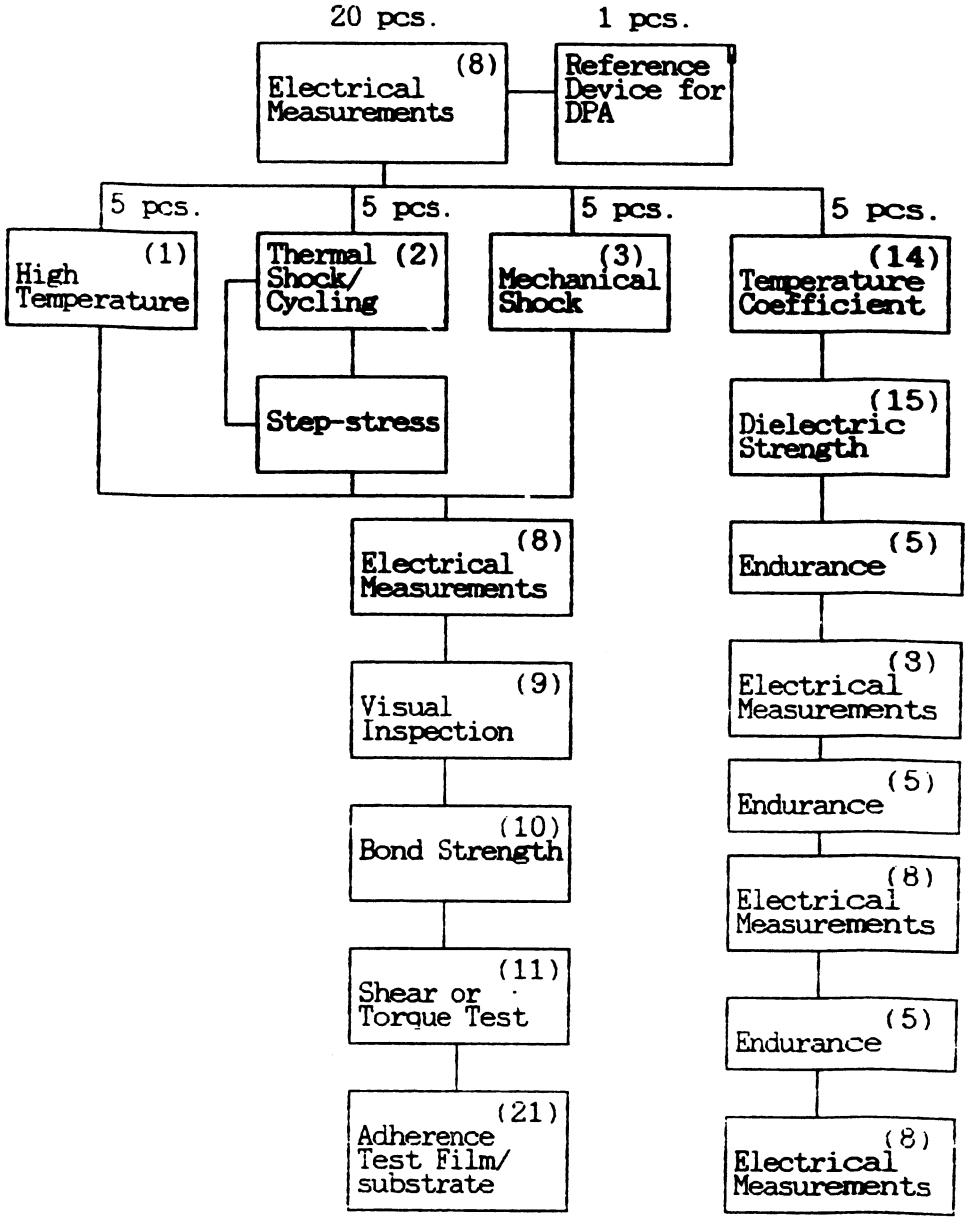

Figure 6. TEST PLAN 1

Note: Numbers in parentheses refer to test numbers of Table 8.

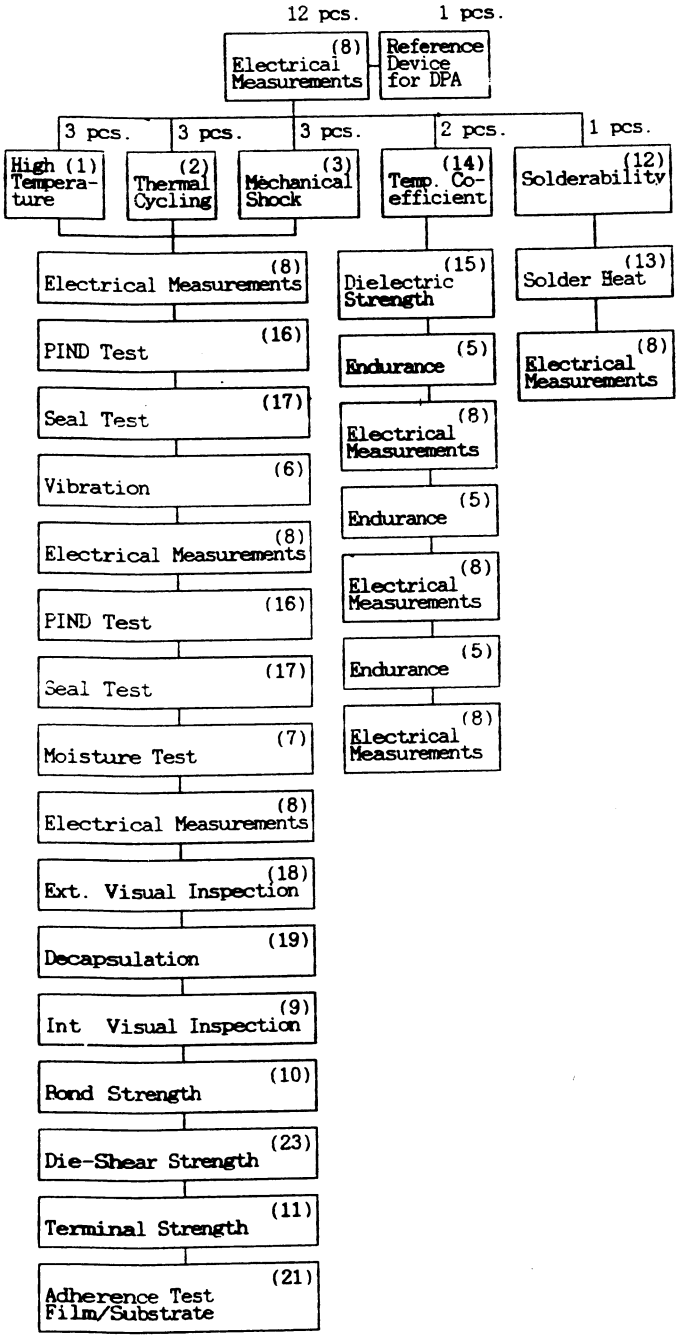

Figure 7. TEST PLAN 2

Note: Numbers in parentheses refer to test numbers of Table 8.

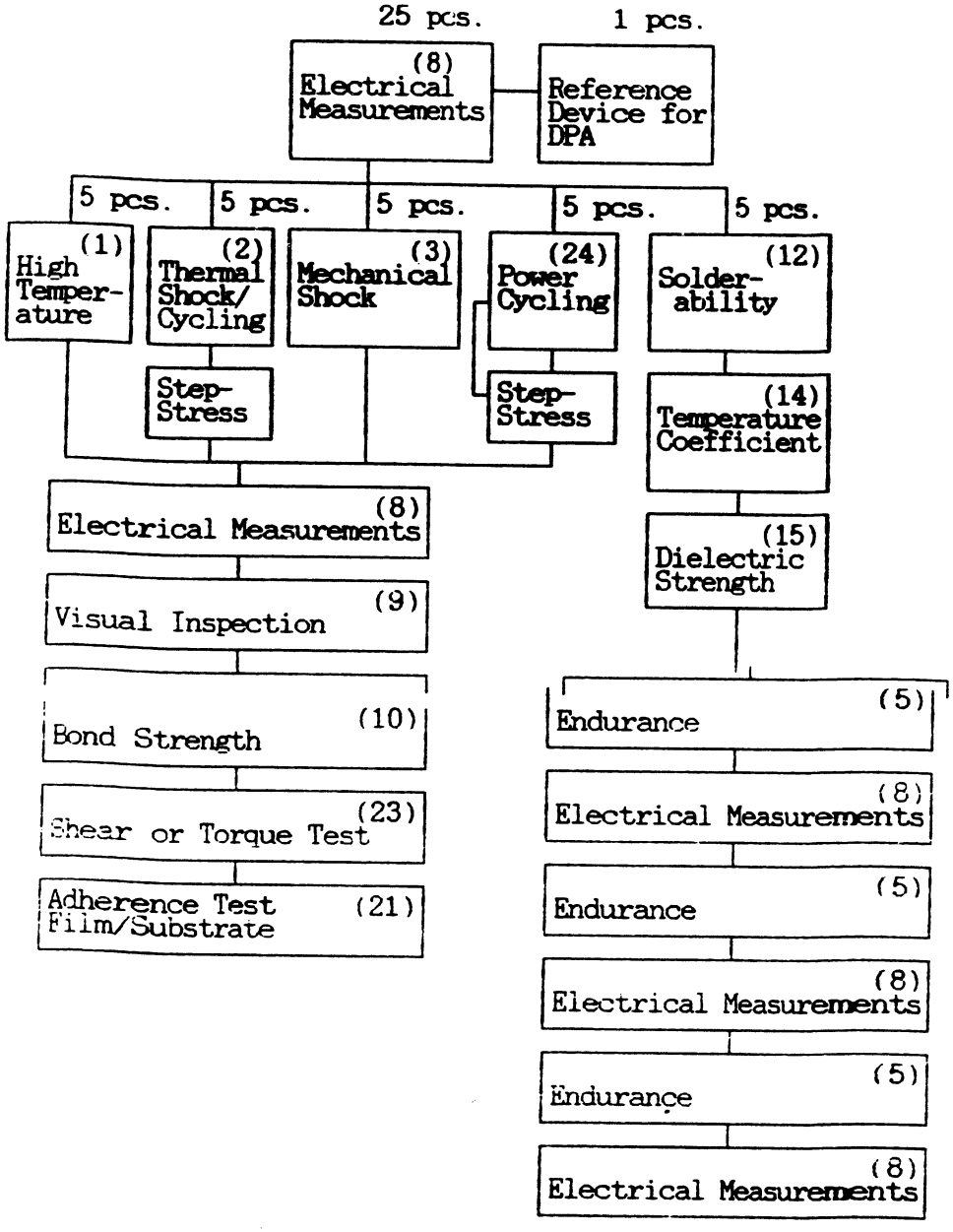

Figure 8. TEST PLAN 3

Note: Numbers in parentheses refer to test number of Table 8.

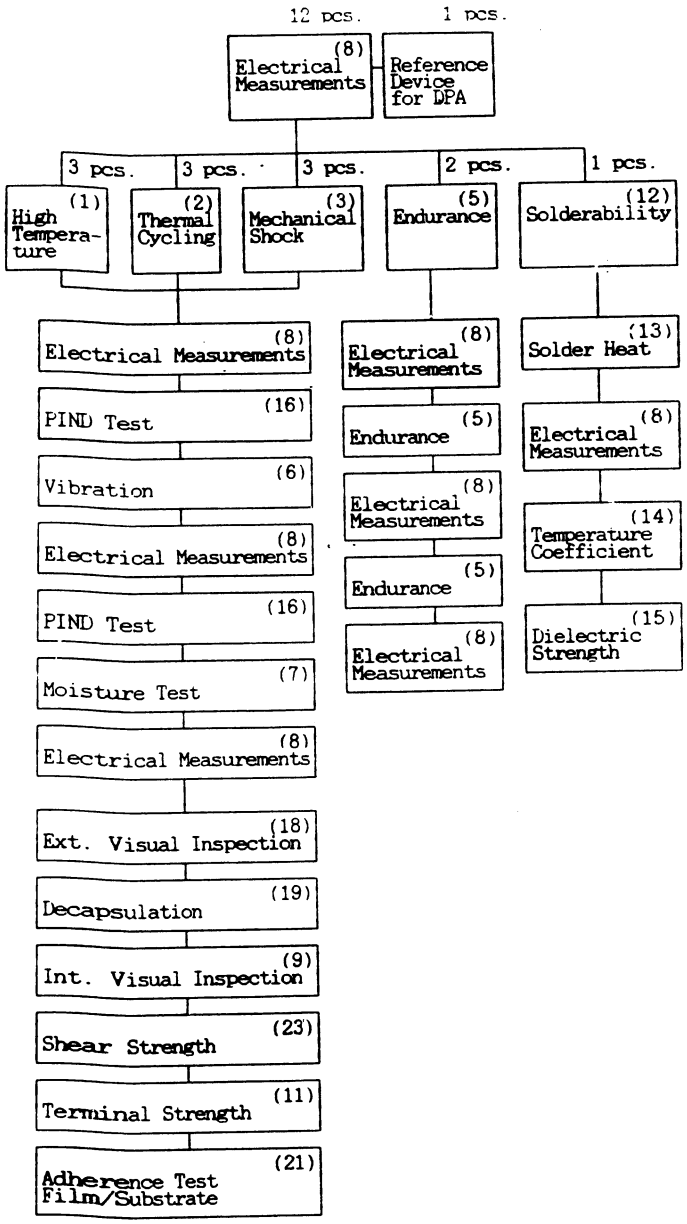

Figure 9. TEST PLAN 4

Note: Numbers in parentheses refer to test numbers Table 8.

3.2.7 Description of tests

The test procedures pertinent to Test Plans 1 to 4 inclusive are listed in Table 8 together with reference to the applicable MIL specifications. The number of each test corresponds to that shown in the test plans.

Table 8 shall be used in conjunction with the supplementary test instructions specified for each of the individual test structures listed in Paragraph 3.2.4.

Table 8 TEST PROCEDURES

No.	Test	MIL-STD /	Method	Test conditions and remarks
1	High-temperature storage	883	1008	Condition "B": + 125 °C, 200 hours
2	Thermal cycling	883	1010	Condition "B", 100 cycles per step up to 500 cycles or failure
3	Mechanical shock	883	2002	Condition "C", as per detail spec.
4	Humidity	202	103B	Duration 2000 hours, no voltage
5	Endurance	202	108A	Temperature: + 125 °C, condition "F", 2000 hours. Electrical load as specified in Paragraph 3.4.3.1
6	Vibration	883	2007	Condition "B", 50 g. Test item shall be glued to the vibration fixture
7	Moisture resistance	883	1004	10V d.c. between all terminals connected together and package; + on terminals
8	Electrical measurements - Resistance	202	303	Test accuracy: ± 0.02% thin-film resistors
	- Capitance		305	F = 1 MHz; Test accuracy on C = ± 0.1%. Registration of loss factor down to 0.001. Capacitor chips.
	- Insulation resistance		302	Condition "A", 100V. The test items are the same as specified for Test 15, "Dielectric strength".
	- Semiconductor components			Functional test. Electrical operational conditions shall be the normal ones for component concerned. To be specified after joint agreement by ESA and manufacturer.
	- Microwave characteristics			Test methods and test conditions suitable for assessing the device shall be defined by the manufacturer and agreed with ESA.
9	Internal visual inspection	883	2017	Not applicable to hermetically sealed semiconductor components attached to substrate.
10	Bond strength	883	2011	Wire-bonds: Test condition "D"

Table 8 TEST PROCEDURES (Continued)

No.	Test	MIL-STD /	Method	Test conditions and remarks
11	Terminal strength (ext. termination)	883	2004	Flexible leads soldered to thin-film Condition "A"; Force = 30 x Q (Newton); Q = lead (mm^2) Flexible and semi-flexible leads in packages. As above. Rigid feed-throughs in packages D 1 mm: as above. Rigid feed-throughs in packages D 1 mm: condition "C1"; Torque 1.5 N.cm.
12	Solderability (Ext. termination)	202	208	Three terminals per test item.
13	Soldering heat (Ext. terminations)	202	210	Condition "B". Three terminals per test item. Visual inspection by microscope (magnification X4) to verify that terminals, glass seals, connection to thin-film substrate or substrate itself are not damaged.
14	Temperature coefficient of resistance (TCR)	202	304	Maximum temperature: + 125 °C Minimum temperature: - 55 °C.
15	Dielectric strength	202	301	Test voltages. Thin-film pattern (all terminals connected together) to plate on reverse side of substrate, to base plate or package: 100 V DC. Between conductors 100 V DC.
16	Particle Impact Noise Detection (PIND)	883	2020	Condition "A".
17	Seal test	883	1014	Step 1: Condition "A1" or "A2"; Step 2: "C1"
18	External visual inspection	883	2009	10V d.c. between all terminals connected together and package; + on terminals

Table 8 TEST PROCEDURES (Continued)

No.	Test	MIL-STD / Method		Test conditions and remarks
19	Decapsulation	Lid shall be removed in such a way that interior of package is not contaminated		
20	Radiographic inspection	883	2012	
21	Adherence test	Under consideration		Under consideration
23	Die-shear strength	883	2019	Shall also be performed on chip capacitors, chip resistors and leadless chip carriers attached to the substrate. Alternatively, torque test may be performed on leadless chip carriers.
24	Power cycling	–	–	All components to be powered at nominal power dissipation level. Power shall be switched on and off 500 times (cycles). Lapse time for each cycle shall be 3 X time constant. Power shall be increased in steps up to failure.

3.2.8 Detail specifications of test structures

The manufacturer shall write a detail specification of each test structure to be evaluated. Each specification shall contain tables of the detailed electrical measurments to be performed before and after exposure to environmental tests. The following shall be stated:

(a) Line-etching quality

Statement of minimum line-width and line-distance.

(b) Thin-film resistors

Manufacturing tolerances	± 15% (untrimmed), ± 0.1% (trimmed)
Maximum change during test	± 0.2%
Maximum temperature coefficient calculated for any range between two test temperatures	As specified by the manufacturer
Maximum voltage coefficient	As specified by the manufacturer
Visual inspection	As per MIL-STD-883

(c) Capacitors, attached chips

Maximum loss factor	As specified by chip manufacturer
Maximum change of loss factor during test	1.5 x initial value
Insulation resistance	$10^{10}\Omega$ minimum
Dielectric strength	As per MIL-STD-202
Bond strength	As per MIL-STD-883
Visual inspection	As per MIL-STD-883

(d) Semiconductors, attached

Electrical functional test	Test limit to be agreed jointly by manufacturer and ESA
Bond strength	As per MIL-STD-883
Visual inspection	As per MIL-STD-883

(e) Wire cross-overs, internal connections

Bond strength	As per MIL-STD-883
Visual inspection	As per MIL-STD-883

(f) External connections and leads

Terminal strength	As per MIL-STD-883
Visual inspection	As per MIL-STD-883
Solderability	As per MIL-STD-202
Soldering heat	As per MIL-STD-202

(g) Assembly and package

Internal visual inspection	As per MIL-STD-883
External visual inspection	As per MIL-STD-883
PIND test	As per MIL-STD-883
Seal test	As per MIL-STD-883
Radiographic inspection	As per MIL-STD-883

(h) Thermal characteristics of high power structures

Thermal resistance to heatsink of:

Each thin-film resistor	Max. 1.5 °C x cm^2/W (*)
Semiconductor chip	Max. 0.75 °C x cm^2/W (*)
Temperature of connection leads	Wire-bonded connections

(*) cm^2 area of thick-film resistor or semiconductor chip.

(i) Structures with baseplate

Visual inspection	As per MIL-STD-883
Radiographic inspection (power structures)	Area of void(s) under dissipative source shall not be more than 25% of the area of that source. Total void area (sum of all voids at substrate/baseplate interface) shall not exceed 25% of substrate area
Insulation resistance	Minimum $10^{10}\ \Omega$

3.2.9 Failure analysis

All failed items shall be subjected to failure analysis. The applied procedure shall permit determination of the cause of failure, failure mode and any corrective action required. A detailed test report of all failed items shall be submitted to ESA.

3.3 EVALUATION REPORT

The manufacturer shall produce an Evaluation Report in compliance with this specification, signed on behalf of the company.

3.3.1 Analysis of results

At the end of the Evaluation Phase, ESA will analyse the results of:
- Line survey
- Evaluation testing.

On the basis of outcome of this review, ESA will decide whether the manufacturer may proceed to the next phase of the programme and whether any corrective actions are required.

3.3.2 Corrective actions

ESA may recommend certain modifications in the manufacturer's organisation, the production line and/or processes. If the manufacturer wishes to proceed to the next phase, he shall implement such modifications. If major changes are deemed necessary, ESA may require repetition of certain evaluation tests and/or re-evaluation of test results.

3.3.3 Process Identification Document (PID)

The manufacturer shall establish a PID, specifying the agreed procedures for manufacturing control. Details of the contents of the PID are given in Paragraph 4.2.

3.4 COMPLETION OF EVALUATION PHASE

Upon satisfactory completion of the Evaluation Phase, ESA will agree the definition of the manufacturer's capabilities and give its consent to proceed to capability approval testing.

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SECTION 4: CAPABILITY APPROVAL TESTING PHASE

4.1 GENERAL

The Capability Approval Testing Phase shall cover all tests approved by ESA upon completion of the Evaluation Phase and consist of:

- the freezing of the processes, process and inspection documents, and materials defined in the Process Identification Document (PID) and
- the manufacture and testing of either test structures or actual circuit types.

4.2 PROCESS IDENTIFICATION DOCUMENT (PID)

Prior to the manufacture of the test structures to be subjected to testing, the manufacturer shall prepare the PID and agree its contents with ESA. The PID shall be divided into sections according to the following guidelines and reference each process to be applied:

Section 1

- Cover page, showing title of PID, issue number and date, and - if applicable - revision letter and date
- Revision list, showing revised pages and dates of revision
- List of contents, showing PID sections.

Section 2

Flow chart of manufacture, assembly and testing with reference to the applicable specifications. An example of this flow chart is depicted in Figure 10.

Section 3

List of specifications with titles, issue/revision numbers and dates referenced in the flow-chart, and used for the manufacture and control of the devices.

Section 4

Organisation of the company, including organigrammes of:

4.1 Management
4.2 Production department
4.3 Quality department

Section 5
Processing of hi-rel orders:
5.1 In-house processing flow-chart of hi-rel orders, showing the extent to which each department (Design Engineering, Reliability, Product Assurance, Production, Quality Control etc.) is responsible for the execution of external orders for hybrid circuits.
5.2 Procurement options, viz. variants and testing levels of qualified hybrid microcircuits which the manufacturer can offer.
5.3 Specimen of a hi-rel traveller
5.4 Points for inspection by orderer.

Section 6
List of subtechniques, materials and rework:
6.1 All subtechniques and asociated test structures used shall be listed. This section shall include a colour photograph of the test structure(s) to be tested.
6.2 All materials, such as substrates, films, epoxies (with infrared spectrum), wires, packages, etc., shall be listed together with the manufacture's name, incoming inspection specification and, where applicable, the validation procedure.
6.3 Provisions for rework shall detail how, when, the number of times and according to what procedure, rework is permitted.

Section 7
Manufacturing line layout:-
7.1 Overall line layout
7.2 Details of testing area
7.3 Dust, humidity and temperature control of the various areas.

Section 8
- Equipment list.

Section 9
- List of failure analysis equipment.
- Standard failure-analysis procedure.

Section 10
Records of lots processed according to the PID, including number(s) and type(s) of circuits, lot acceptance results and applicable qualification reports. This section shall be annually updated.

The information contained in this section shall be arranged as exemplified in Table 9 and, as a minimum, include the items listed therein.

The established PID shall be called up automatically in any documentation applicable to deliveries according to this specification or ESA Procurement Specification PSS-01-608. Any deviations from the PID shall be subject to prior ESA approval.

The complete PID, comprising all called-up specifications, shall be kept by the manufacturer at the production plant; it shall be made available to ESA or its designated representative for review.

A condensed PID, comprising all basic information, e.g. flow-charts, lists of specifications, materials and processes, but complemented by copies of only the most important specifications, shall be kept by ESA and treated as proprietary information.

The PID shall be made available to the Orderer for inspection. The production flow-chart shall always be made available to the Orderer upon request.

Travel-logs shall include all processing details, dates and yields of major process steps and any useful comments. They shall be signed or stamped on behalf of the manufacturer's Quality Assurance department in respect of those operations that are listed as functions of that department. The manufacturer shall keep the travel-logs for a minimum period of three years and, upon request, make them available to ESA, its designated representative, or the Orderer.

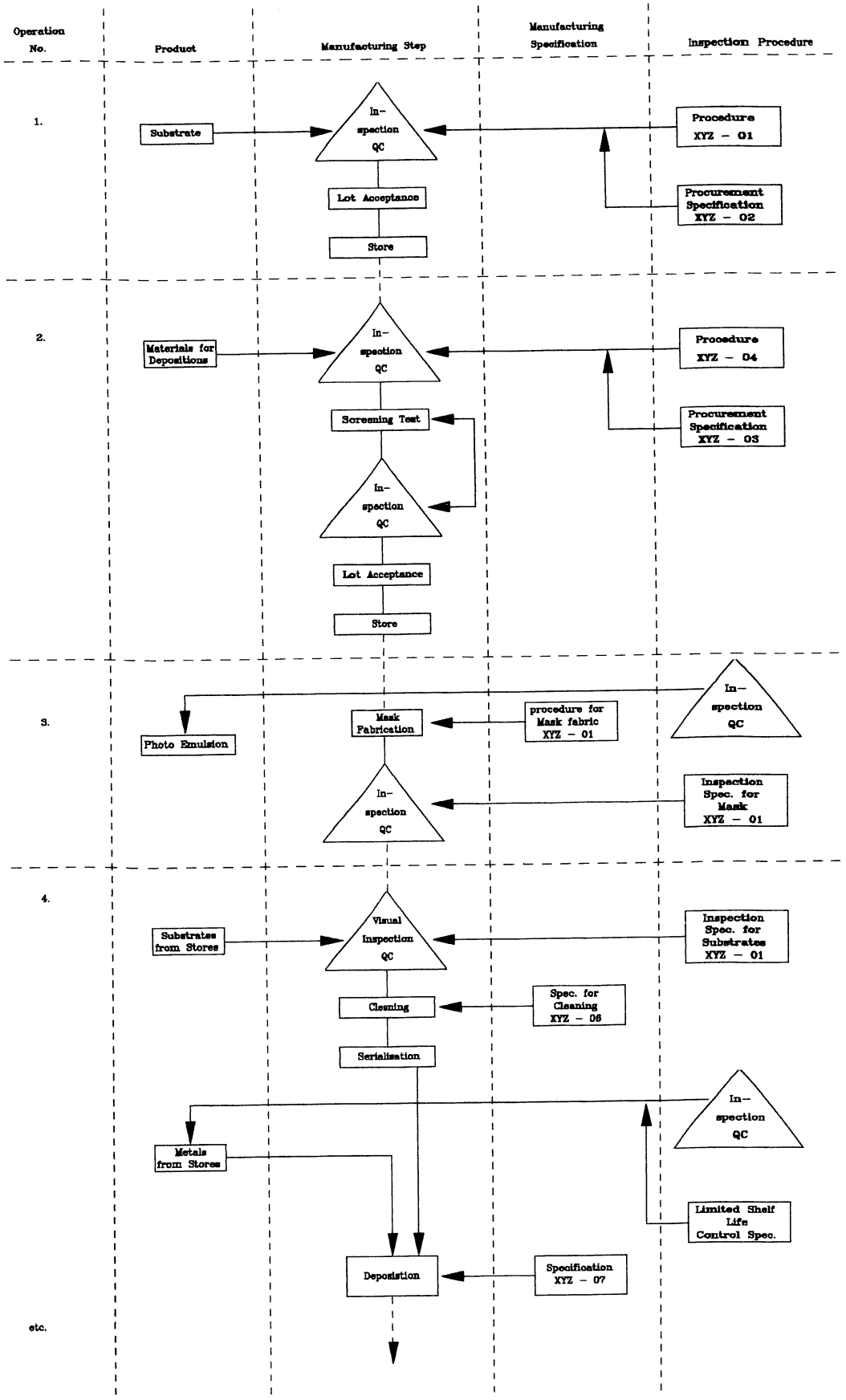

Figure 10. EXAMPLE OF MANUFACTURING FLOW CHART

Table 9 EXAMPLE OF PID - SECTION 10 INFORMATION

Programme or project	*No. of circuits produced*	*Screening level*	*Description of circuit*	*Spec. no.*	*Lot no.*	*Lot qual. report.*
EXOSAT	*20*	*B*	*Control circuit*	*XYZ-123*	*8230*	*ABC-456*

4.3 DETAIL SPECIFICATIONS

Before testing commences, all detail specifications of test structures shall be prepared by the manufacturer and submitted to ESA for approval. They shall be written according to Annex "B" of ESA PSS-01-608.

4.4 MANUFACTURE OF TEST STRUCTURES

Lot manufacture shall be in accordance with the approved PID. ESA reserves the right to participate in precap visual inspection.

4.5 ADDED-ON COMPONENTS

All added-on components can be commercially available parts provided they are technologically equivalent to space-qualified parts.

4.6 REWORK

Some of the circuits submitted to testing shall have been reworked according to the methods described in the PID.

General rules for rework are as specified in MIL-M-38510 for class "s" devices.

4.7 LOT PRODUCTION REPORTS

The manufacturer shall submit to ESA reports of:
- screening (including burn-in parameter drift values)
- final acceptance test
- failure analysis of parts failed during screening
- in/out figures relevant to the following inspections and tests:
  - visual inspection and final test of thin-film network
  - pre-seal acceptance test
  - screening
  - final acceptance test

The in/out figures shall be recorded in terms of the number of parts submitted to a specific test, or group of tests, and the number of rejects. Failure mode data shall be included.

4.8 TEST PLAN

The manufacturer shall prepare and submit to ESA for approval a test plan, including a specification of each test structure and a time schedule for production and tests. The time schedule shall show the dates envisaged for performance of the following milestone operations:

- start of manufacture
- start of pre-seal acceptance test
- start of screening and final test
- start of mechanical, environmental and endurance tests
- completion of mechanical, environmental and endurance tests.

The manufacturer shall notify ESA, or its delegated representative, as soon as each of these operations has been completed.

All documents specified herein for review by ESA shall be submitted at least 22 working days before either the due review date or the date on which the manufacturer intends to proceed to the next action in the sequence of operations.

4.9 CAPABILITY APPROVAL TESTING

Testing shall be performed in accordance with the test plan shown in Figures 11 and 12 for microwave hybrid integrated circuits in nonhermetic or hermetic enclosures, respectively, and the requirements defined in the following subparagraphs.

The total number of test structures shall depend on the number of test structure/types to be tested. It may be necessary to test more than one type of structure. If so, the number of structures specified in Table 10 shall be applicable. The layout of the test structure(s) may be identical to that of any structure specified for the Evaluation Phase or that of a new structure.

Satisfactory test results of reworked test structures shall automatically imply the acceptance of nonreworked test structures.

In the case of several types of test structures, they shall be distributed over the various subgroups as shown in Table 10.

Table 10 NUMBER OF TEST STRUCTURES FOR CAPABILITY APPROVAL

Number of test structure types	Number of types required per subgroup						Total number per type
	I	II	III	IV	V	VI	
1	6	6	3	3	10	6	34
2	3	3	2	2	6	3	19
3	2	2	1	1	4	2	12

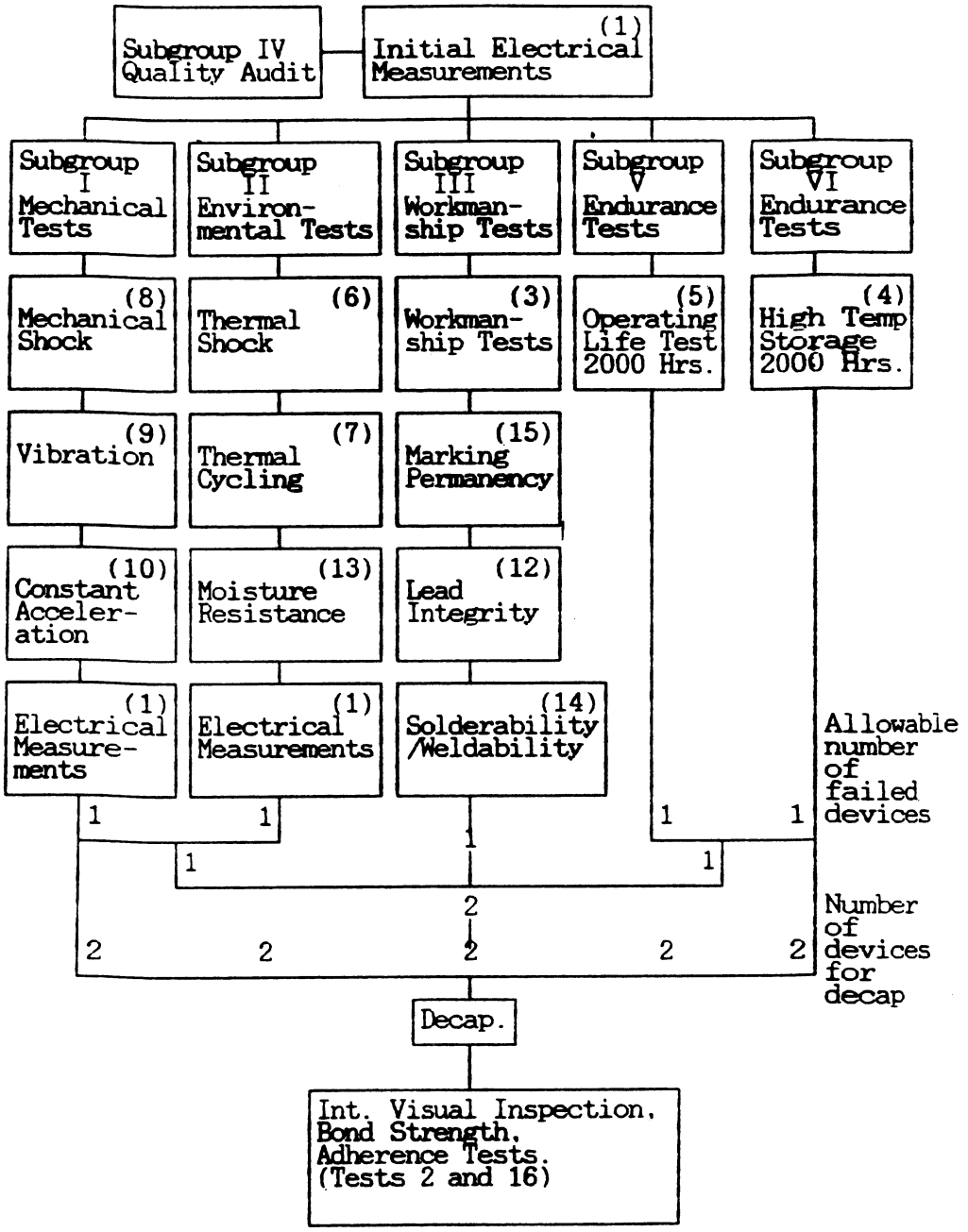

Figure 11. TEST PLAN

Note: Numbers in parentheses refer to test numbers of Table 11

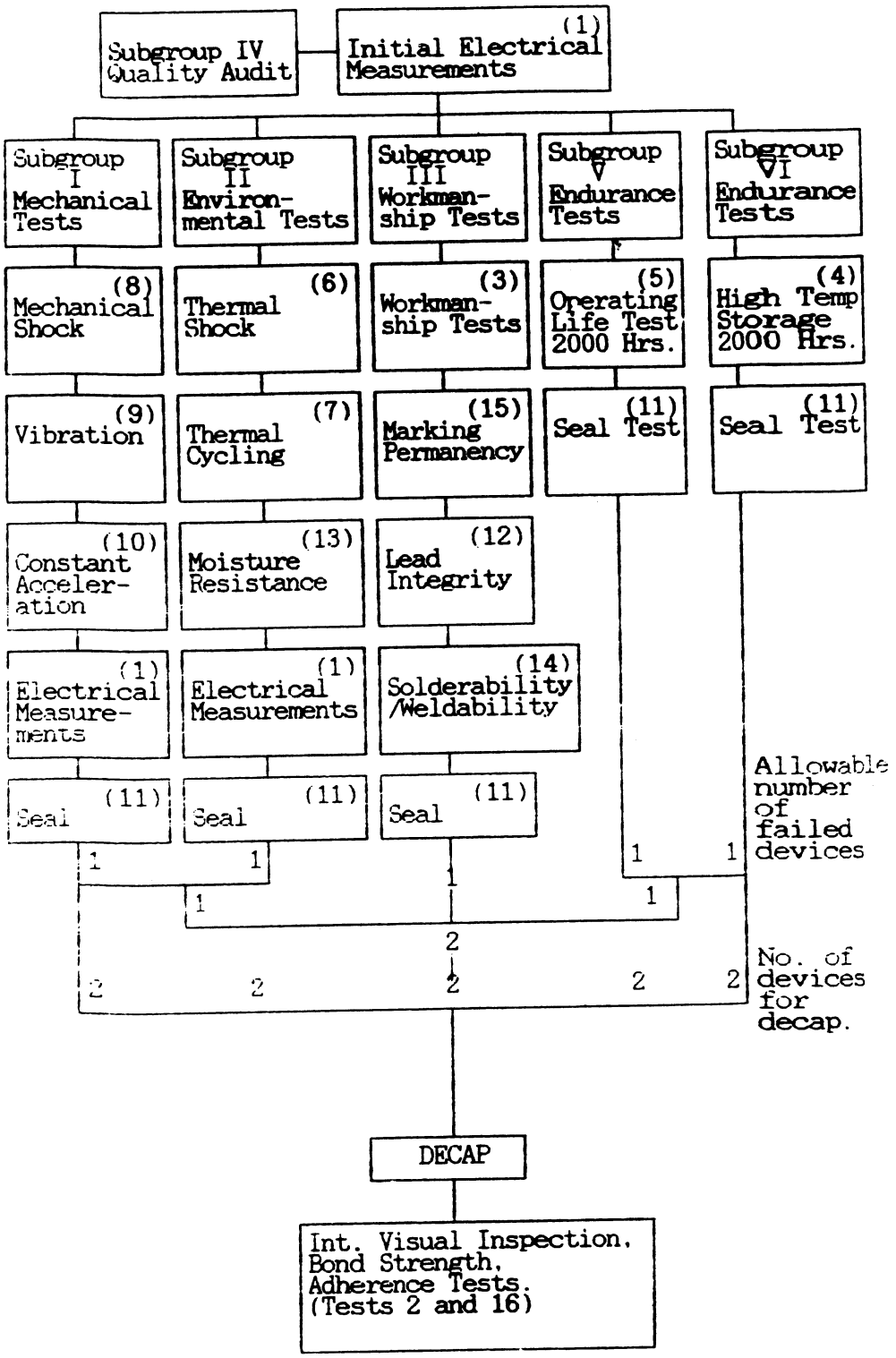

Figure 12. TEST PLAN

Note: Numbers in parentheses refer to test numbers of Table 11

4.9.1 Subgroup III, workmanship

Workmanship shall be assessed as follows:
- Radiographic inspection
- External visual inspection (including marking)
- Physical dimensions and weight
- Internal water-vapour content (for Test Plan 12 only)

4.9.1.1 Radiographic inspection

This inspection shall be performed in accordance with MIL-STD-883, Method 2012.

4.9.1.2 External visual inspection (including marking)

This inspection shall be performed according to MIL-STD-883, Method 2009. The marking shall be inspected to ascertain its conformance to the requirements of the applicable test structure detail specification. It shall be legible and unambiguous. Any misalignment of the highest and lowest letters in a row shall not exceed 70% of the letter size. The overlapping of the lowest letters of one row and the highest letters of the next row shall constitute a failure.

4.9.1.3 Physical dimensions and weight

All physical dimensions specified in the applicable detail specification shall be measured. Any nonconforming part shall be considered as a failure and contribute towards qualification failure. Two or more nonconforming dimensions of one part shall count as one failure.

All parts shall be weighed and the average weight per part recorded.

4.9.1.4 Internal water vapour content

According to MIL-STD-883C, Method 1018.2, on 1 (one) package.

4.9.2 Subgroup IV, quality audit

The devices of this subgroup, together with the results of the initial electrical test, shall be sent to ESA for construction analysis as follows:

The devices of this group will be subjected to the inspections and operations defined in the following sub-paragraphs. A record will be made of each separate step and all records will be compiled and summarised in one report together with the analysis results.

(a) Decap

The parts will be decapped or opened without damage to the functional elements. Any inspection of a decapped device will take place in a controlled atmosphere.

(b) Description

Each part type will be described fully and photographed such that interior of package and functional elements are highlighted. Descriptions will include measurement data of physical dimensions and relative location of added parts.

(c) Internal visual inspection

The parts will be inspected for conformity to the applicable requirements of MIL-STD-883, Method 2017 and Condition "A" of Method 2010.

Any visual anomalies will be microphotographed and the presence of any foreign matter will be recorded. The parts will be inspected by a Scanning Electron Microscope (SEM) to verify that bonds, joints, trimming paths, metallisation steps etc. meet the specified requirements. Each of these items will also be photographed.

(d) Bond strength/adherence group

The control devices will be submitted to the following tests of Table 11:

Bond strength	(Test 16a)
Chip adherence	(Test 16b)
Substrate adherence	(Test 16c)

All test results, including failure categories will be recorded.

(e) Any other construction analysis tests.

For example: seal test, PIND test, water vapour content etc.

Table 11 TEST METHODS

No.	Test	MIL-STD-883, method	Conditions and/or remarks
1	Electrical measurements	Electrical measurements of all parameters listed in the detail specification shall be performed in accordance with the test methods and conditions specified in that specification. All results shall be recorded and all samples allocated to testing shall be submitted to these electrical tests prior to the start of testing. There shall be no catastrophic electrical failures at this stage. Any such failures shall invalidate the approval. Any devices exhibiting electrical out-of-tolerance parameters shall be replaced. Inspections shall be made during and on completion of the mechanical, environmental and endurance tests. Failures observed during these measurements shall count as failed devices.	
2	Internal visual inspection	2017	and condition "A" of method 2010
3	Workmanship		See paragraph 4.9.1
3a	Radiographic inspection	2012	
3b	External visual inspection	2009	
3c	Physical dimensions		See detail specification and Paragraph 4.9.1.3 of this specification
3d	Internal water Vapour content	1018	On one (1) sample; Test plan 12 only
4	High temperature	1008	Condition "B". Electrical measurements as specified in the detail specification shall be recorded at 0, 168 and 500 + 48 hours. Total duration of tests shall be 2000 + 96 hours. Histograms shall be made at each measurement. The final drift percentage of each parameter in relation to the initial 0-hour measurement shall be recorded.

Table 11 TEST METHODS (Continued)

No.	Test	MIL-STD-883, method	Conditions and/or remarks
5	Operating life	1005	Conditions as specified in the detail specification. Electrical measurements as specified in the detail specification shall be recorded at 0, 168 and 500 + 24 hours; 1000 + 48 hours and 2000 + 48 hours. Total duration of tests shall be 2000 + 96 hours. Histograms shall be made at each measurement. The final drift percentage of each parameter in relation to the initial 0-hour measurement shall be recorded.
6	Thermal shock	1011	Condition "B"; go/no-go electrical measurements after test
7	Thermal cycling	1010	ditto
8	Mechanical shock	2002	Condition as specified in PSS-01-608
9	Vibration	2007	Condition "A"; go/no-go electrical measurements after test
10	Constant acceleration	2001	Condition as specified in PSS-01-608 go/no-go electrical measurements after test
11	Seal	1014	Condition "A", fine leak; Condition "C", gross leak
12	Lead integrity	2004	Conditions "B1" and "C1" as applicable. Measurements: Only visual inspection for damage
13	Moisture resistance	1004	Lead integrity test is considered as initial conditioning.
14	Solderability/ weldability	2003	All terminations
15	Marking permanency	2015	
16	Bond strength/ Adherence (a) bond strength (b) chip adherence (c) substrate attachement strength	2015 2011 2019 2027	Condition "D"

4.10 TEST REVIEW

4.10.1 Data presentation

The data files to be prepared of each tested structure shall be entitled "Data File of Capability Approval Testing of .....(part type)" and bear the relevant contract number and date. Each file shall contain:

4.10.1.1 Summary schedule sheet(s)

This sheet (or sheets) shall summarise the entire test sequence and include in/out burn-in numbers, scheduled and actual data of each operation and relevant electrical tests (e.g. go/no-go recorded etc.). The sheet(s) shall be presented such that status can be easily ascertained.

Updated summary sheet(s), showing relevant part type and lot number(s), shall be sent to ESA at each agreed milestone.

4.10.1.2 Equipment accuracy

The manufacturer shall provide ESA with a list of all equipment to be used and the accuracy thereof, including the applicable calibration controls.

4.10.1.3 Data records and histograms

Data records and histograms shall provide all information obtained from the time of burn-in up to and including end of test. Any data related to the Subgroup Control Device shall also be included. Each recorded parameter shall be marked with a symbol and listed together with the pertinent measurement conditions and limits.

Where a parameter drift requirement is specified, the data shall include both drift percentage and absolute change. The same information shall be provided in respect of parameters measured during life testing, even if no parameter drift criteria are applicable during such testing.

The manufacturer shall supply histograms of the measured parameters, containing all records from time of burn-in up to and including end of testing as well as the average sigma and two sigma. If parameter drift is specified, a histogram of the percentage and/or absolute drift shall be included.

4.10.1.4 Other requirements

The test review data shall include an index and any relevant comments and graphs.

4.10.2 Failure criteria and classification

Failures of any of the categories specified in the following subparagraphs shall contribute towards failure. Each part exhibiting a failure of any of these categories shall count as one failure.

4.10.2.1 Visual and mechanical inspection

These inspections form part of the Quality Audit Procedure. The detection of any defective units at this stage may be cause for verification of the entire lot, the replacement of defective parts or the suspension of testing and ordering of a new lot. Such defective parts shall be considered as rejects and contribute towards lot acceptance/rejection.

4.10.2.2 Out-of-tolerance parameters

These parameters shall be measured during the initial electrical tests. Defective units shall not be submitted to qualification testing. Any defects noted during subsequent electrical measurements shall be considered as rejects and contribute towards lot acceptance/rejection.

4.10.2.3 Degradation

This applies to those parameters that, following the original measurement, exceed the specified limits when subsequent measurements are performed. Any devices whose parameters do not conform to the specified limits shall be considered as rejects.

If the relevant detail specification prescribes delta values for a particular parameter, the applicable limit shall be the absolute limit plus or minus the appropriate delta limit.

4.10.2.4 Parameter drift

Devices whose parameter drift exceed the limits defined in the detail specification shall be considered as rejects and contribute towards failure. Even if no accept/reject criteria are specified, ESA reserves the right to suspend the approval of test results in the event of sudden large parameter changes and/or anomalous behaviour for which no reasonable explanation can be given.

4.10.2.5 Catastrophic failures

This type of failure occurs when parameters exceed the specified limits to such an extent that a device is rendered ineffective. Catastrophically failed devices shall be considered as rejects.

4.10.2.6 Operator errors

These are failures caused by electrical or mechanical overstress which, normally, do not contribute towards failure. However, when a failure of this category is detected, the testing of the subgroup concerned shall cease immediately and the manufacturer shall notify ESA without delay. The manufacturer shall then take appropriate action to determine the cause of the failure and, when established, satisfy ESA that such cause has been isolated and remedied. ESA will then decide in the light of all available evidence whether or not those parts that may have suffered overstress are to be replaced. Any replacement parts shall be submitted to all of the tests which the replaced parts have undergone. Replacement parts shall always be from the same production lot as the original parts and must have been processed identically.

4.10.2.7 Capability approval

Capability approval status will be granted by ESA authority upon satisfactory completion of Evaluation and Capability Approval testing and will be valid for two years.

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SECTION 5: MAINTENANCE, SUSPENSION AND WITHDRAWAL OF CAPABILITY APPROVAL

5.1 MAINTENANCE OF CAPABILITY APPROVAL

Capability approval is maintained by the continuous production of devices according to the technology defined in the PID. At least two months prior to the expiry date of line approval, the manufacturer shall furnish ESA with the following details of lots processed to ESA Specification PSS-01-608: lot numbers, deliverable parts and numbers and a synthesis of failures during burn-in, environmental and life testing. If considered necessary, ESA may require further details.

The minimum requirement for capability approval is that, during the previous 12-month period, one lot of hybrids has been manufactured, screened and tested for lot acceptance in accordance with ESA PSS-01-608. Renewal of capability approval shall be valid either from the date on which

(a) the previous approval expired, or
(b) the date on which lot acceptance testing was completed successfully if this date occured more than 6 months prior to (a).

In addition, the manufacturer shall provide ESA with three samples of a recently manufactured hi-rel batch of components for Destructive Physical Analysis (DPA). On the basis of both the information received and the DPA results, ESA will then decide whether approval can be maintained.

In the case of deviations from the qualified technology, i.e. if new materials and/or processes are to be introduced, ESA and the manufacturer will jointly agree on a testing programme which will cover the new techniques and serve for approval maintenance purposes.

5.2 SUSPENSION OF CAPABILITY APPROVAL

ESA may suspend the approval status of a production line, or any part thereof, for the following reasons:

(a) failure(s) which cannot be remedied within a reasonably short period of time
(b) failure of more than two consecutive lots.

In the event of (a) and (b), the manufacturer shall initiate any corrective action considered appropriate and, to achieve reinstatement of approval status, supply ESA with evidence that the cause of failure has been eliminated.

During the suspension period, the line shall not be considered as approved and not be used for the production of circuits unless they serve for approval purposes.

5.3 WITHDRAWAL OF CAPABILITY APPROVAL

Approval status will be withdrawn:

(a) at the request of the manufacturer

(b) in the case of persistent non-adherence to the production processes agreed for capability approval

ANNEX - DEFINITIONS

CHIP COMPONENT

A component in its ultimate state of miniaturisation.

COMPONENT

A device which performs an electronic, electrical or electromechanical function and consists of one or more elements joined together which, normally, cannot be dissambled without destruction. The terms component and part are interchangeable. Typical examples of components are: transistors, integrated circuits, hybrids, capacitors etc.

DESTRUCTIVE PHYSICAL ANALYSIS (DPA)

A series of inspections, tests and analyses of a sample component to verify that the materials, design and workmanship used for its construction, as well as the construction itself, meet the requirements of the applicable specification and are suitable for the intended application.

ENCLOSURE

A metal container with a lid into which one or more hybrid microcircuits are assembled either directly or after attachment to a mounting plate. Electrical connection to the hybrid microcircuit is by means of RF and DC connectors through the enclosure wall. The enclosure may be hermetic or nonhermetic.

FILM NETWORK

Layers of conductive, resistive, dielectric and/or passivating materials deposited onto an insulating substrate for the purpose of performing electronic circuit functions.

HYBRID MICROCIRCUIT

A component performing an electronic circuit function which consists of a thick-or thin-film network on a substrate which supports active and/or passive chip components connected to it.

LIMITED LIFE MATERIAL

A material which can be processed and stored for only a limited period of time before deterioration of its specified properties.

MICROWAVE

Frequencies above 1 GHz.

MOUNTING PLATE

A metallic plate or carrier providing both mechanical support and an RF ground plane for the substrate.

NONCONFORMANCE
An apparent or proven condition of any item or document that does not conform to the specified requirements and may lead to incorrect operation or interpretation during its envisaged usage. The term "nonconformance" is also used for failure, discrepancy, defect, anomaly, malfunction and deficiency.

PACKAGE
The primary encapsulation of a chip component.

PROCESS IDENTIFICATION DOCUMENT (PID)
A set of frozen documents defining the technology, processes and inspection procedures applicable to the manufacture of the components or items on order.

PRODUCTION LOT
A production lot consisting of a quantity of a specific device type manufactured on the same production line by the same processing techniques and according to the same component/part design using the same raw materials during one uninterrupted production run.

SELECTED SUBLOT
A selected sublot is that part of a production lot which is manufactured in excess of the actual quantity of components required.

SYMBOLS AND ABBREVIATIONS
The symbols and abbreviations defined in MIL-S-19500, MIL-M-38150, MIL-STD-883, ESA Specifications PSS-01-60, PSS-01-606, this specification and the applicable detail specifications shall be applicable.

THICK-FILM
A network onto which the film is deposited by screen-printing methods. The thickness of the fixed film is usually in the range of 10 to 25 micrometres.

THIN FILM
A network onto which the film is deposited by one or more of the following processes: electro-depositing, plating, evaporation, sputtering, anodisation or polymerisation. The thickness of the film may be in the range of 50 to 2000 Å.

TRACEABILITY
To derive from recorded identification data the history, application, use and location of an item.