ECSS-Q-ST-70-61C
8 April 2022

Space product assurance

High reliability assembly for surface mount and through hole connections

ECSS Secretariat
ESA-ESTEC
Requirements & Standards Section
Noordwijk, The Netherlands

Foreword

This Standard is one of the series of ECSS Standards intended to be applied together for the management, engineering, product assurance and sustainability in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards. Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

This Standard has been prepared by the ECSS-Q-ST-70-61C Working Group, reviewed by the ECSS Executive Secretariat and approved by the ECSS Technical Authority.

Precedence

Line drawings and illustrations are depicted herein to assist in the interpretation of the written requirements of this standard. The text takes precedence over the figures.

Disclaimer

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Change log

ECSS-Q-ST-70-61C 8 April 2022	First issue This new ECSS Standard was created by merging and updating the content of the following three standards: • ECSS-Q-ST-70-07C "Verification and approval of automatic machine wave soldering" • ECSS-Q-ST-70-08C "Manual soldering of high-reliability electrical connections" • ECSS-Q-ST-70-38C Rev.1 "High-reliability soldering for surface-mount and mixed technology" The intention of this completely new standard was to optimize the structure of the document, following the chronological order of assembly processes and introducing criterion for new technologies that were not covered by the three standards now superseded by this new standard.

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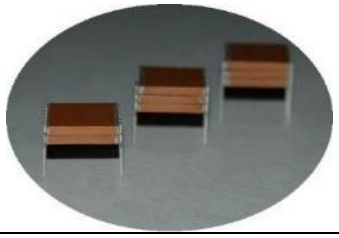
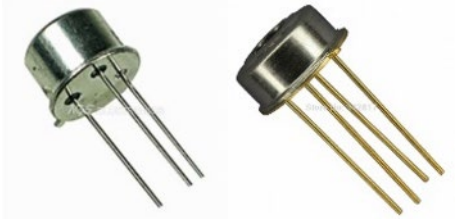
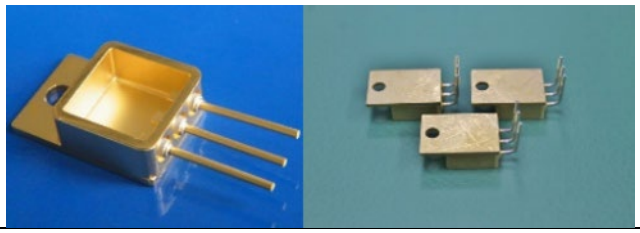
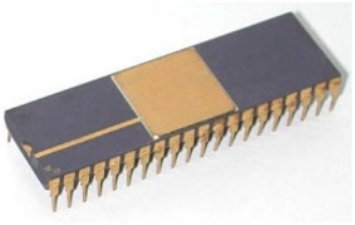
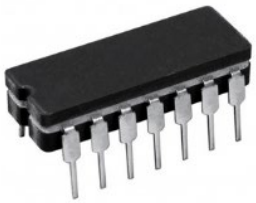
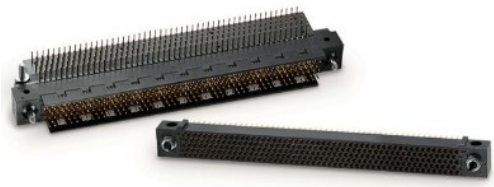
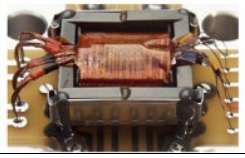
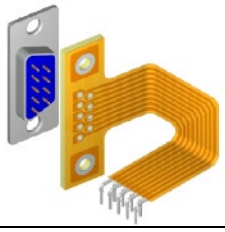
Introduction

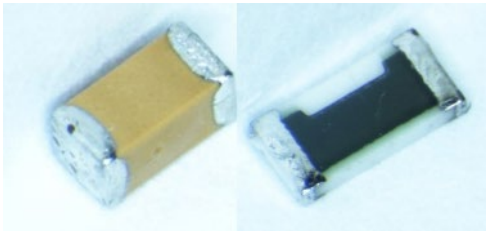
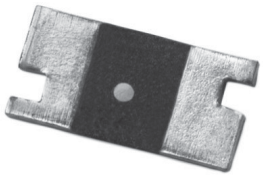
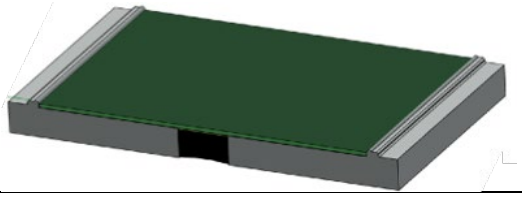
This document defines the technical requirements and quality assurance provisions for the manufacture and verification of high-reliability electronic circuits of surface mount, through hole, solderless assemblies, and soldering of harness and wire interconnection, for space applications, launchers, and associated equipment.

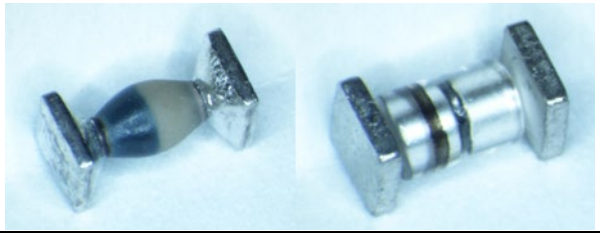
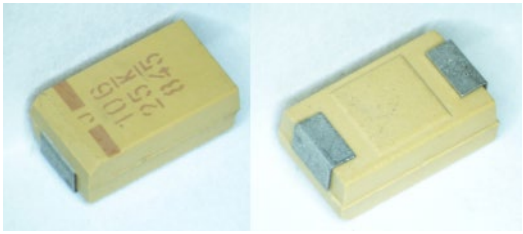
In the following table, principal types of through hole components and SMDs, including examples, can be gathered in the following families.

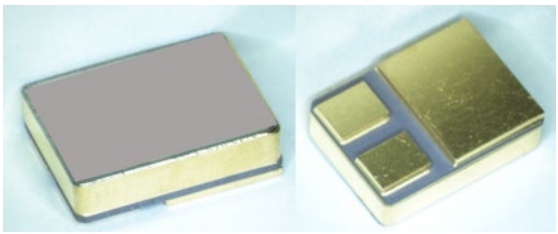
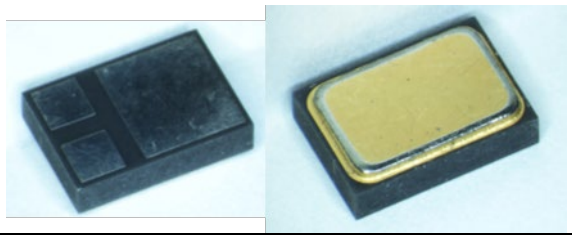
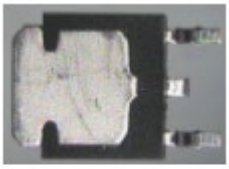
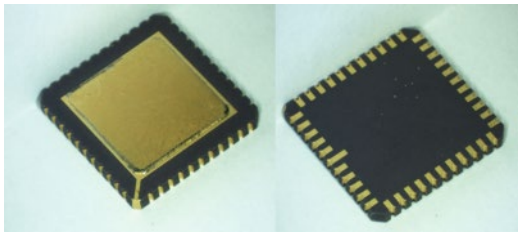
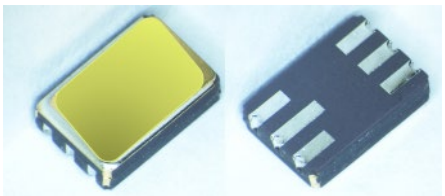
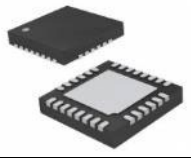
NOTE In the text of this document the term "component" is used instead of "device".

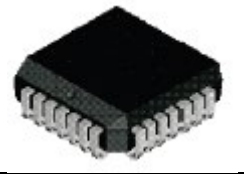
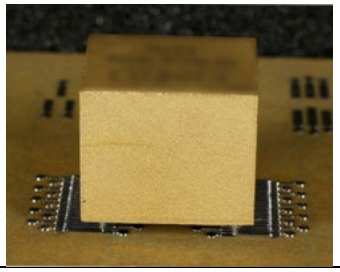
THROUGH HOLE COMPONENTS (non exhaustive list)	
Radial component resistors capacitors fuses diodes	
Axial component Capacitors resistors diodes	
Stacked capacitors CH capacitors CNC capacitors	
TO Metal Can package TO-39	
TO Metal tab package TO254	

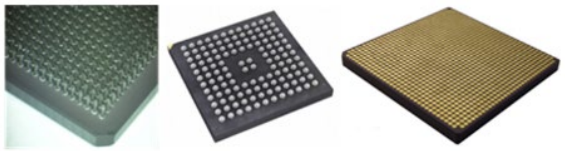
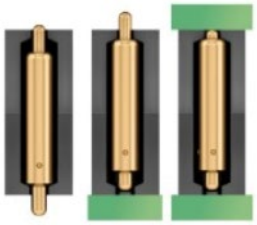
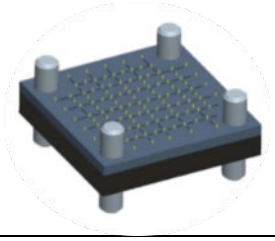
THROUGH HOLE COMPONENTS (non exhaustive list)	
Dual in Line Package (DIL or DIP) Side brazed DIP and DIL	 
Connectors	 
Leaded magnetics transformers with straight pins	  
Sculptured flex	

SMT COMPONENTS (non exhaustive list)	
Rectangular and square end-capped or end-metallized component with rectangular body, leadless chip (see 10.4.2) ceramic end capped chip resistors and capacitors.	
ceramic resistors arrays	
metallic terminations fuses, thermistors CSM 2512	
metallic termination resistor SMS 2512	
Cylindrical and square end-capped components with cylindrical or oval body, leadless chip (see 10.4.3) MELF for cylindrical end capped: • Diodes in MELF, minimelf or micromelf	

SMT COMPONENTS (non exhaustive list)	
• Resistors in MELF, minimelf or micromelf Square end capped: • D- 5 family for square end capped with cylindrical or oval bodies	 
Bottom terminated chip component (see 10.4.4) **This type of component has either metallised terminations on the bottom side or extended terminals from the bottom side.** Chip inductors	 
Component with inward formed L-shaped leads (see 10.4.5) moulded tantalum chip capacitors. SMD moulded shunt	 

SMT COMPONENTS (non exhaustive list)	
Leadless component with plane termination (see 10.4.6) - With metal plane termination: SMD0.5, SMD1, SMD2, SMD0.2*(TO276 JEDEC family denomination)	
- With non-metal plane termination: SMD0.2* ***Package exists in two versions**	
Leaded component with plane termination (see 10.4.7) Diode PAcKage (DPAK or TO252)	  DPAK
Leadless castellated ceramic chip carrier component (see 10.4.8) The main component of this type is leadless ceramic chip carrier (LCCC) LCC6	 
No lead QFN (see 10.4.9) quad flat pack no leads	

SMT COMPONENTS (non exhaustive list)	
Flat pack and gull-wing leaded component (see 10.4.10) small-outline transistor (SOT), small-outline package (SO), flat pack and quad flat pack (QFP) and SMD connectors with stress-relief (MHD). transformers Components with both flat rectangular and round leads are included in this group. The components can be delivered either with pre-formed leads or with straight leads which will be then in-house preformed by the user.	 
"J" leaded component (see 10.4.11) ceramic leaded chip carriers (CLCC) and plastic leaded chip carriers (PLCC).	
Components with ribbon terminals without stress relief (flat lug leads) (see 10.4.12) This package has flat leads extending from the sides	
Stacked modules components with leads protruding vertically from bottom (see 10.4.13)	

SMT COMPONENTS (non exhaustive list)	
Area array components (AAD) (see 10.4.14) Components connected via an array of solder columns (Column Grid Array - CGA), solder balls (Ball Grid Array - BGA) or directly to the board (Land Grid Array - LGA). The columns and balls consist of various types of solder with wide-ranging properties.	 CGA BGA LGA
Solderless connection (see 10.7) solderless connectors solderless interposers for LGA or connectors	 

1
Scope

This Standard defines the technical requirements and quality assurance provisions for the manufacture and verification of high-reliability electronic circuits of surface mount, through hole, solderless assemblies and soldering of harness and wire interconnection.

The Standard defines workmanship requirements, the acceptance and rejection criteria for high-reliability assemblies intended to withstand ground testing conditions including LTS (long term storage) and the environment imposed by space flight and launchers.

The mounting and supporting of components, terminals and conductors specified in this standard applies only to assemblies designed to continuously operate over the mission within the temperature limits of -55 °C to +85 °C at solder joint level.

Requirements related to printed circuit boards are contained in ECSS-Q-ST-70-60 and ECSS-Q-ST-70-12.

This standard does not cover lead-free soldering and associated requirements.

This Standard does not cover the qualification and acceptance of the EQM and FM equipment with high-reliability electronic circuits of surface mount, through hole and solderless assemblies.

This Standard does not cover verification of thermal properties for component assembly.

This Standard does not cover pressfit connectors due to the possible damage in the PCB that is not evaluated within this test requirement.

The qualification and acceptance tests of equipment manufactured in accordance with this Standard are covered by ECSS-E-ST-10-03.

This standard may be tailored for the specific characteristics and constraints of a space project, in accordance with ECSS-S-ST-00.

2
Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revision of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the more recent editions of the normative documents indicated below. For undated references, the latest edition of the publication referred to applies.

ECSS-S-ST-00-01	ECSS system - Glossary of terms
ECSS-M-ST-40	Space project management - Configuration and information management
ECSS-Q-ST-10-09	Space product assurance - Nonconformance control system
ECSS-Q-ST-20	Space product assurance - Quality assurance
ECSS-Q-ST-60	Space product assurance - Electrical, electronic and electromechanical (EEE) components
ECSS-Q-ST-60-05	Space product assurance - Generic requirements for hybrids
ECSS-Q-ST-60-13	Space product assurance - Commercial electrical, electronic and electromechanical (EEE) components
ECSS-Q-ST-70	Space product assurance - Materials, mechanical parts and processes
ECSS-Q-ST-70-01	Space product assurance - Cleanliness and contamination control
ECSS-Q-ST-70-02	Space product assurance - Thermal vacuum outgassing test for the screening of space materials
ECSS-Q-ST-70-12	Space product assurance - Design rules for printed circuit boards
ECSS-Q-ST-70-28	Space product assurance - Repair and modification of printed circuit board assemblies for space use
ECSS-Q-ST-70-60	Space product assurance -Qualification and procurement of printed circuit boards
ECSS-Q-ST-70-71	Space product assurance -Materials processes and their data selection
ESA-STR-258	ESA-Approved Skills Certification Requirements Electronic Assembly Domain
ESCC 23500 (September 2013)	Requirements for lead materials and finishes for components for space application
IPC J-STD-001H (September 2020)	Requirements for Soldered Electrical and Electronic Assemblies

IPC J-STD-004B-AM1 (November 2011)	Requirements for Soldering Fluxes
IPC J -STD-033D (January 2018)	Handling, Packing, Shipping and Use of Moisture, Reflow, and Process Sensitive Devices
IPC-TM-650 (Latest edition)	Test methods manual. Surface Insulation Resistance, Fluxes
ISO 9454-1:2016	Soft soldering fluxes; classification and requirements
ISO 14644-1:2015	Cleanrooms and controlled environments
MIL-STD-883 K Method 2009 (April 2016)	Test Method Standard, Microcircuits

3
Terms, definitions and abbreviated terms

3.1 Terms from other standards

a. For the purpose of this Standard, the terms and definitions from ECSS-S-ST-00-01 apply.

b. For the purpose of this Standard, the terms and definitions from ECSS-Q-ST-60 apply, in particular for the following term(s):

   1. commercial component

c. For the purpose of this Standard, the terms and definitions from ECSS-Q-ST-70-28 apply, in particular for the following term(s):

   1. repair
   2. rework

3.2 Terms specific to the present standard

3.2.1 Approval Authority

entity that reviews and accepts the verification programme, evaluating the test results and grants the final approval

3.2.2 assembly sensitive component

component prone to have cracks in solder joint exceeding 75 % of acceptance criteria of solder cracks or showing nonconformance outside the component manufacturer limit, due to assembly.

NOTE 1 The ESA list of assembly sensitive components is regularly updated and published on ESCIES for information, see www.escies.org, Technologies - ESA SMT Verification. ESA-TECMSP-MO-018961.

NOTE 2 Each company maintains its own list of assembly sensitive components in the PID.

3.2.3 bifurcated terminal

terminal containing a slot or split in which wires or leads are placed before soldering

NOTE The term "**split terminal**" is synonymous.

3.2.4 blister

delamination in form of localized swelling and separation between any of the layers of a laminated base material in a printed circuit board

3.2.5 bonding

application process of adhesive underneath a package for mechanical or thermal purpose

3.2.6 bridging

build-up of solder or conformal coating between components, component leads or base substrate forming an elevated path

3.2.7 clinched lead

conductor or component lead which passes through a printed circuit board and is then bent to contact the printed circuit board pad

NOTE The clinched portion is not forced to lie flat on the pad and some innate spring back is desirable before this form of termination is soldered.

3.2.8 cold flow

tendency of a solid material to move slowly or deform permanently under the influence of persistent mechanical stresses.

NOTE For example, for PTFE (Teflon) insulation sleeves under pressure.

3.2.9 cold solder joint

joint in which the solder has a blocky, wrinkled or piled-up appearance and shows signs of improper flow or wetting action

NOTE It can appear either shiny or dull, but not granular. The joint normally has abrupt lines of demarcation rather than a smooth, continuing fillet between the solder and the surfaces being joined. These lines are caused by either insufficient application of heat or the failure of an area of the surfaces being joined to reach soldering temperature.

3.2.10 conformal coating

thin polymeric film applied on a populated PCB that conforms to the shape of the surface it covers.

3.2.11 co-planarity

difference between maximum and minimum termination height when component rests on flat surface

3.2.12 collective assembled components

set of components that are soldered to PCB in one operation

NOTE For example, vapour phase soldered components, in contrast to manually soldered where each component is soldered individually.

3.2.13 critical zone

area in the solder joint in which the existence and magnitude of cracks is subject to acceptance or rejection

3.2.14 dewetting

condition in a soldered area in which the liquid solder has not adhered intimately, characterized by an abrupt boundary between solder and conductor, or solder and terminal/termination area

NOTE This is often seen as a dull surface with islands of thicker shiny solder.

3.2.15 disturbed solder joint

unsatisfactory connection resulting from relative motion between the conductor and termination during solidification of the solder

3.2.16 dynamic wave soldering machine

system that achieves wave soldering and which consists of stations for fluxing, preheating, and soldering by means of a conveyor

3.2.17 electrical clearance

spacing between separate electrical conductors of a printed circuit board assembly

3.2.18 exposed pad

exposed metallization on the bottom of a package

NOTE The exposed pad can have both electrical or thermal purpose and is often plated with same material and finish as the edge terminations, for soldering purposes. Exposed pad can be thermally bonded, soldered or left unconnected if not needed for the intended application.

3.2.19 fillet

smooth concave build-up of material between two surfaces

NOTE Example: A fillet of solder between a component lead and a solder pad or terminal, or a fillet of conformal coating material between a component and printed circuit board.

3.2.20 flux

material which, during soldering, removes the oxide film, protects the surface from oxidation, and permits the solder to wet the surfaces to be joined

3.2.21 glass meniscus

glass fillet of a lead seal which occurs where an external lead leaves the package body

3.2.22 modal survey

characterization of the dynamic properties of systems in the frequency domain

NOTE A typical example is testing structures under vibrational excitation

3.2.23 outsourcing

act of subcontracting work to another company in compliance with customer PID

3.2.24 pin in paste

process where a through hole component is mounted and soldered in the surface mounting process

3.2.25 pits

small holes or sharp depressions in the surface of solder

NOTE This can be caused by flux blow-out due to entrapment or overheating.

3.2.26 potting compound

compound, usually electrically non-conductive, used to encapsulate or as a filler between components, conductors, or assemblies

3.2.27 pressfit connector

solderless termination technology where each contact is pressed into a plated hole of a printed circuit board creating a mechanical and electrical joint

3.2.28 reprocessing

preparatory operation done on a component prior to assembly

NOTE Degolding, pretinning, lead forming, and cutting are examples of reprocessing.

3.2.29 shield

metallic sheath surrounding one or more wires, cables, cable assemblies, or a combination of wires and cables that is used to prevent or reduce the transmission of electromagnetic energy to or from the enclosed conductors

NOTE The shield also includes an insulating jacket that can cover the metallic sheath.

3.2.30 solder balls

numerous spheres of solder having not melted in with the joint form and being scattered around the joint area normally attached by flux residues

NOTE Can be caused by incorrect preheating or poor-quality solder.

3.2.31 solder-cup terminal

hollow, cylindrical terminal closed at one end to accommodate one or more conductors

3.2.32 solder icicle

conical peak or sharp point of solder usually formed by the premature cooling and solidification of solder upon removal of the heat sources

3.2.33 solder pad

conductive surface on a printed circuit board to which terminations are soldered to form electrical connections

3.2.34 solder stand-off

thickness of solder between the underside of the component termination and the solder pad

3.2.35 split terminal

see "**bifurcated terminal**" 3.2.3

3.2.36 staking

application process of adhesive on the outside of a package for mechanical purpose

3.2.37 stress relief

method or means to minimize stresses to the soldered termination or component

NOTE Generally, in the form of a bend or service loop in a component lead, solid or stranded wire to provide relief from stress between terminations, as that caused, for instance by movement or thermal expansion.

3.2.38 stud termination

upright conductor termination through a printed circuit board

3.2.39 technology samples

samples of boards assembled with representative technology

3.2.40 thermal shunt

element with good heat-dissipation characteristics used to conduct heat away from an article being soldered

3.2.41 turret terminal

round post-type grooved stud around which conductors are fastened before soldering

3.2.42 underfill

material deposited between a component and substrate

3.2.43 verification board

substrate assembled with components subjected to a verification programme

3.2.44 wicking

flow of molten solder or cleaning solution by capillary action

NOTE Occurs when joining stranded wire; solder is drawn within the strands, but normally not visible on outer surface of strands. Wicking can also occur within the stress relief bend of a component lead.

3.3 Abbreviated terms

For the purpose of this Standard, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
AAD	area array device NOTE: also known as "area array component"
AOI	automatic optical inspection
AWG	American wire gauge
AXI	automatic X-ray inspection
BGA	ball grid array
CBGA	ceramic ball grid array
CCGA	ceramic column grid array
CGA	column grid array
CLCC	ceramic leadless chip carrier
CTE	coefficient of thermal expansion
DCL	declared component list
DIL	dual in line
DIP	dual in line package
DPAK	diode package
DRD	document requirement definition
EDX	Energy dispersive X-ray
ETFE	ethylene tetrafluoroethylene
EPA	ESD protected area
ESD	electrostatic discharge
FEP	fluorinated ethylene propylene
FM	flight model or flight hardware
FP	flat pack package
IST	interconnect stress testing
JEDEC	Joint Electron Component Engineering Council
LCCC	leadless ceramic chip carrier

Abbreviation	Meaning
MELF	metal electrode face bonded NOTE: MELF includes the terms "minimelf" and "micromelf"
MIP	mandatory inspection point
MPCB	Materials, Mechanical Parts and Processes Control Board
MRR	manufacturing readiness review
MSL	moisture sensitivity level
PCB	printed circuit board
PLCC	plastic leaded chip carrier
PID	process identification document
PSD	power spectral density
PTFE	polytetrafluoroethylene
PTH	plated though hole
QFN	quad flat pack no leads
QFP	quad flat pack
R_g	resistance to ground
R_s	surface resistance
r.m.s.	root-mean-square
SEM	scanning electronic microscope
SIR	surface insulation resistance
SMD	surface mounted device NOTE: In the text of this document the term “component” is used instead of “device”
SMT	surface-mount technology
SO	small outline
SOD	small outline diode
SOT	small outline transistor
SOP	small outline package
TO	transistor outline
TRB	test review board
TRR	test readiness review
TSOP	thin small outline package
RF	radio frequency

3.4 Nomenclature

The following nomenclature apply throughout this document:

a. The word “shall” is used in this document to express requirements. All the requirements are expressed with the word “shall”.

b. The word “should” is used in this document to express recommendations. All the recommendations are expressed with the word “should”.

NOTE It is expected that, during tailoring, all the recommendations in this standard are either converted into requirements or tailored out.

c. The words “may” and “need not” are used in this document to express positive and negative permissions respectively. All the positive permissions are expressed with the word “may”. All the negative permissions are expressed with the words “need not”.

d. The word “can” is used in this document to express capabilities or possibilities, and therefore, if not accompanied by one of the previous words, it implies descriptive text.

NOTE In ECSS “may” and “can” have a completely different meaning: “may” is normative (permission) and “can” is descriptive.

e. The present and past tense are used in this document to express statement of fact, and therefore they imply descriptive text.

4
Principles of reliable soldered connections

The following are the general principles to provide reliable soldered connections:

- Reliable soldered connections are the result of proper design, control of tools, materials, processes work environments and workmanship performed in accordance to verified and approved procedures, inspection control and precautions.
- The basic design concepts to provide reliable connections and to avoid solder joint failure are as follows:
  - Stress relief is an inherent part of the design which reduces detrimental thermal and mechanical stresses on the solder connections.
  - Where adequate stress relief is not possible materials are so selected that the mismatch of thermal expansion coefficients is a minimum at the constraint points in the component mounting configuration.
- The assembled substrates are designed to allow easy inspection, rework, and repair.
- The electrical and mechanical integrity of components and assemblies are retained after exposure to processes employed during manufacture and assembly, as handling, baking, fluxing, soldering, cleaning depanelization, electrical test and PCB integration.
- Soldering to gold using tin-lead alloy can cause failure.

5
Preparatory conditions

5.1 Facility cleanliness

ECSS-Q-ST-70-61_1510001

a. Personnel facilities shall be separated from the soldering areas.

NOTE Example: Washrooms, eating areas, smoking facilities.

ECSS-Q-ST-70-61_1510002

b. Furniture shall be arranged to allow thorough cleaning of the floor and workbench.

ECSS-Q-ST-70-61_1510003

c. Areas used for soldering shall be kept free from contaminants.

NOTE Loose material such as dirt, dust, solder particles, oil or clipped wires can contaminate soldered connections.

ECSS-Q-ST-70-61_1510004

d. Working areas shall be kept free from any tools or equipment not used for the current task.

ECSS-Q-ST-70-61_1510005

e. Working surfaces shall be covered with an easily cleaned hard top or have a replaceable surface of clean, non-corrosive, silicone-free ESD compatible paper.

ECSS-Q-ST-70-61_1510006

f. Tools used during soldering operations shall be free of visible contaminant.

ECSS-Q-ST-70-61_1510007

g. Excess lubricants shall be removed from tools before soldering starts.

5.2 Environmental conditions

ECSS-Q-ST-70-61_1510008

a. The clean room shall be compliant to the requirements of clause 5.3.1 of ECSS-Q-ST-70-01.

ECSS-Q-ST-70-61_1510009

b. The soldering area shall have as minimum a cleanliness level of ISO Class 8.2 in accordance with ISO 14644-1 (2015).

NOTE Particle concentrations for ISO Class 8.2 are not mentioned in the ISO Standard and can only be calculated with the formula in Annex E of ISO 14644-1 (2015). See Table 5-1.

Table 5-1: Particle concentrations classes 8 till 9 according to ISO 14644-1 (2015)

Particle sizes				
ISO class	**0,5 µm**	**1 µm**	**5 µm**	**Comment**
ISO-class 8	3 520 000	832 000	29 300	From Table 1 of ISO
ISO-class 8.1	4 430 000	1 050 000	36 800	Calculation acc ISO Annex E equation
ISO-class 8.2	5 570 000	1 320 000	46 400	Calculation acc ISO Annex E equation
ISO-class 8.5	11 100 000	2 630 000	92 500	From Annex E in ISO
ISO-class 9	35 200 000	8 320 000	293 000	From Table 1 of ISO

ECSS-Q-ST-70-61_1510010

c. Areas used for assembly or cleaning of components and areas where toxic or volatile vapours are generated or released shall include a local air extraction system.

ECSS-Q-ST-70-61_1510011

d. The room temperature of the facility shall be maintained at (22 ±3) °C.

ECSS-Q-ST-70-61_1510012

e. The relative humidity at room temperature of the facility shall be maintained at (55 ±10) %.

ECSS-Q-ST-70-61_1510013

f. The soldering area shall not be exposed to draughts.

ECSS-Q-ST-70-61_1510014

g. Air shall be supplied to the room through a filtering system that provides a positive pressure difference with respect to adjacent rooms.

5.3 Lighting requirements

ECSS-Q-ST-70-61_1510015

a. Lighting intensity shall be a minimum of 1080 lux on the work surface.

NOTE In selecting a light source, the colour temperature of the light is an important consideration. Light ranges from 3000 K-5000 K enable users to distinguish various printed circuit assembly features and contaminants with increased clarity.

ECSS-Q-ST-70-61_1510016

b. At least 90 % of the work area shall be without shadows or severe reflections.

5.4 Precautions against static discharges

5.4.1 Overview

Electronic components are particularly sensitive to electrostatic charging and discharging. To protect these components, it is necessary to define measures with regard to their handling, transport and storage.

The ESD control programme helps reducing to a minimum level the ESD-related damage to components. Main topics of the programme are:

- ESD coordinator,
- Training,
- Product qualification,
- Compliance verification,
- Grounding/bonding systems,
- Personnel grounding,
- EPA requirements,
- Packaging systems,
- Marking.

The controls referenced in this document have been selected from document "ANSI/ESD S20.20-2014 2.0 SCOPE". The goal is to prevent damage of the isolated conductors and of the ESD sensitive devices (ESDS) which are susceptible to discharges that are greater than or equal to 100 V (Human Body Model) or 200 V (Charged Device Model).

5.4.2 General

ECSS-Q-ST-70-61_1510017

a. An ESD Control Programme in accordance with EN 61340-5-1 (2016) shall be developed and implemented by the supplier.

NOTE EN 61340-5-2 guideline can be used for editing the ESD Control Programme.

ECSS-Q-ST-70-61_1510018

b. The process for the selection of new components shall include their ESD sensitivity.

ECSS-Q-ST-70-61_1510019

c. Electrostatic sensitive components shall be handled, prepared, mounted, soldered, and cleaned in an ESD protected area compatible with ESD class of the components.

NOTE Electrostatic sensitive components are classified in different categories. For some, additional ESD conditions to the nominal are needed.

5.4.3 ESD Protected Area

ECSS-Q-ST-70-61_1510020

a. ESD sensitive devices shall be assembled in an EPA.

ECSS-Q-ST-70-61_1510021

b. As a minimum, a dissipative mat, a wrist strap and common grounding facility for both shall be in place in the EPA.

ECSS-Q-ST-70-61_1510022

c. EPA areas shall be visibly marked as such.

ECSS-Q-ST-70-61_1510023

d. ESD rules and regulations shall apply as specified in EN 61340-5-1 (2016).

ECSS-Q-ST-70-61_1510024

e. If the measured electrostatic field or surface potential exceeds the stated limits, ionization or other charge mitigating techniques shall be used.

ECSS-Q-ST-70-61_1510025

f. Relative Humidity shall be controlled in the EPA in accordance with requirement 5.2e.

5.4.4 Precautions against ESD during manufacturing

ECSS-Q-ST-70-61_1510026

a. Delimited EPA and corresponding ESD control items shall be in compliance with Table 5-2.

ECSS-Q-ST-70-61_1510027

b. Ionized air in presence of high voltage or RF shall be used in compliance with components manufacturer recommendations.

NOTE Static charges on isolated components or tooling can be dissipated using ionised air.

ECSS-Q-ST-70-61_1510028

c. A wrist strap shall be worn by the operator.

ECSS-Q-ST-70-61_1510029

d. Powered equipment at the workstation shall be grounded.

ECSS-Q-ST-70-61_1510030

e. The normal value of the resistance between the tip of the soldering system and the ground of the ESD protected area shall not exceed 5 Ω.

NOTE The measurement is generally performed at soldering temperature.

ECSS-Q-ST-70-61_1510031

f. A ground-fault circuit interrupter shall be installed.

ECSS-Q-ST-70-61_1510032

g. Protective clothing shall be made from static dissipative material.

ECSS-Q-ST-70-61_1510033

h. Gloves and finger cots shall be made from static dissipative material.

ECSS-Q-ST-70-61_1510034

i. Tools, such as mounting aids, consumables, masking tape, shall be conductive or static dissipative.

ECSS-Q-ST-70-61_1510035

j. Paperwork accompanying ESD sensitive components shall be contained in static dissipative bags or envelopes.

NOTE Example of accompanying paperwork are traveller logs, drawings, and instructions.

ECSS-Q-ST-70-61_1510036

k. Paperwork shall not come into contact with ESD sensitive components.

ECSS-Q-ST-70-61_1510037

Table 5-2: EPA requirements summary

ESD Control item		Limits values * (unit: Ω)
Working surfaces, storage, racks and trolleys	Dissipative top surface	$R_s < 1 \times 10^9$
	ESD protected to ground	$R_g < 1 \times 10^9$
Flooring	ESD protected to ground	$R_g < 1 \times 10^9$
Ionization		Decay (1000 V to 100 V) in less than 20 s Offset voltage ± 35V
Seating	ESD protected to ground	$R_g < 1 \times 10^9$
Wrist strap system	ESD protected to ground	$R_g < 35 \times 10^6$
* Values are taken from Tables 2 and 3 of EN 61340-5-1:2016.		

5.4.5 Protective packaging and ESD protection

ECSS-Q-ST-70-61_1510038

a. All ESD-sensitive items shall be contained within ESD-protective containers for movement between and within ESD-protected areas.

ECSS-Q-ST-70-61_1510039

b. ESD protective packaging shall display ESD warning signs.

ECSS-Q-ST-70-61_1510040

c. If the packaging is not ESD safe, it shall be labelled accordingly.

NOTE The objective of ESD protection is to prevent ESD to the item contained within, to allow for dissipation of charge, and to prevent charging of the ESD item by an external electrostatic field.

ECSS-Q-ST-70-61_1510041

d. A container providing mechanical and ESD protection shall be used, whenever the ESD-sensitive electronic assembly is transported within a manufacturing plant or during shipment to external destinations.

NOTE This can be achieved by a container with:

- an outer shell that provides adequate mechanical protection for the contents,
- foam or bubble wrap shock absorbing liners that have static shielding covers,
- shielding package for the ESD sensitive contents.

ECSS-Q-ST-70-61_1510042

e. All static-shielding bags shall be metallized.

ECSS-Q-ST-70-61_1510043

f. Bags, film, bubble wrap or foam of Pink-Polyethylene shall not be used near any ESD-sensitive item or within an ESD protected area.

NOTE Pink-polyethylene provides little protection against ESD events and voltage fields and is a contaminants source.

ECSS-Q-ST-70-61_1510044

g. Shipping popcorn, foam liners and polystyrene foam shall not be used near ESD-sensitive items unless shielding overwrap protects them.

ECSS-Q-ST-70-61_1510045

h. Electrostatic sensitive components shall be kept in appropriate ESD protected packaging.

NOTE For example, kept in shielded bags.

ECSS-Q-ST-70-61_1510046

i. Containers for ESD sensitive components shall be labelled as such.

5.5 Equipment and tools

5.5.1 General

ECSS-Q-ST-70-61_1510047

a. Equipment and tools shall be inspected to meet requirements from respective clauses 5.5.2 to 5.5.19.

ECSS-Q-ST-70-61_1510048

b. All tools and inspection equipment shall be maintained and calibrated, and their results recorded in accordance with clause 17.

ECSS-Q-ST-70-61_1510049

c. Equipment shall not generate, induce, or transmit electrostatic charges to components being placed.

ECSS-Q-ST-70-61_1510050

d. Any machine or part of machine, in particular the conveyor, shall be grounded to avoid electrostatic discharge.

ECSS-Q-ST-70-61_1510051

e. Machines and equipment used to solder surface mount components shall either be a type incorporating dynamic single or dual solder wave or be of the solder reflow type.

ECSS-Q-ST-70-61_1510052

f. The supplier shall verify, based on the available documentation, that the equipment do not impose any processing parameters that are in

contradiction to the processing parameters given by the individual component data sheets.

NOTE Examples of processing parameters include maximum temperature to avoid internal melting, thermal shocks, thermal damages, removal of marking ink, degradation of encapsulating plastic.

ECSS-Q-ST-70-61_1510053

g. Temperature and time profiles for assembly shall be identified by the supplier and approved by the Approval Authority.

ECSS-Q-ST-70-61_1510054

h. The supplier shall identify changes and implement a verification programme in compliance with the requirements from clause 13.

ECSS-Q-ST-70-61_1510055

i. The supplier shall demonstrate the reproducibility of their processes.

5.5.2 Brushes

ECSS-Q-ST-70-61_1510056

a. Medium-stiff natural- or synthetic bristle, ESD-safe, brushes shall be used for cleaning.

NOTE 1 Special care has to be taken not to damage any surface or adjacent materials.

NOTE 2 Brushes with wooden handle can be used.

ECSS-Q-ST-70-61_1510057

b. Brushes shall be cleaned in a solvent in accordance with clause 6.4.

ECSS-Q-ST-70-61_1510058

c. Brushes shall not be damaged by the solvents used for PCB cleaning.

ECSS-Q-ST-70-61_1510059

d. Wire brushes shall not be used.

5.5.3 Cutters and pliers

ECSS-Q-ST-70-61_1510060

a. Cutting edge profiles and cutter usage shall be in accordance with Figure 5-1.

ECSS-Q-ST-70-61_1510061

b. The cutter used for trimming conductor wire and component leads shall shear sharply, producing a clean, flat, smooth-cut surface along the entire cutting edge.

NOTE 1 These measures minimize the transmission of mechanical and shock loads to delicate components.

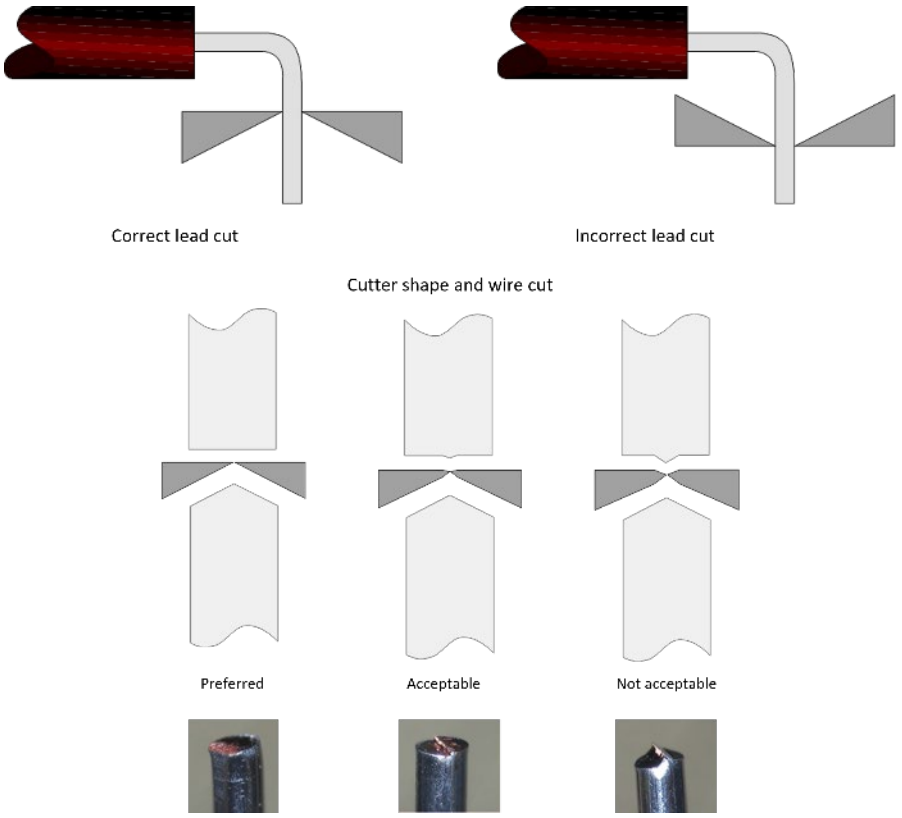
NOTE 2 Smooth, long-nose pliers or tweezers can be used for attaching or removing conductor wires and component leads.

ECSS-Q-ST-70-61_1510062

c. No twisting action shall occur during the cutting operation.

ECSS-Q-ST-70-61_1510063

d. Cutting edges shall be checked for damage and maintained in a sharp condition.



ECSS-Q-ST-70-61_1510064

Figure 5-1: Profile of correct cutters for trimming leads

5.5.4 Bending tools

ECSS-Q-ST-70-61_1510065

a. Component leads shall be bent or shaped using tools, including automatic bending tools, which do not nick or damage the leads or insulation.

ECSS-Q-ST-70-61_1510066

b. Components shall not be damaged by the bending process specified in clause 8.2.7.

NOTE It is good practice to use bending tools with polished finish.

ECSS-Q-ST-70-61_1510067

c. Bending tools shall have no sharp edges in contact with the component leads.

ECSS-Q-ST-70-61_1510068

d. A maximum reduction of 10 % of initial section of the lead may be acceptable provided that it is representative of the verified configuration.

5.5.5 Clinching tools

ECSS-Q-ST-70-61_1510069

a. Clinching tools shall not damage the surfaces of printed-circuit conductors, components or component leads.

5.5.6 Insulation strippers

5.5.6.1 Thermal strippers

ECSS-Q-ST-70-61_1510070

a. The temperature of the stripper shall not burn, blister, or cause excessive melting of the insulation.

NOTE 1 Thermal insulation strippers can be used for wire insulation types susceptible to damage by mechanical strippers.

NOTE 2 It is good practice to apply thermal strippers for use with AWG 22 and smaller wire sizes where there is a possibility of the wire stretching if a mechanical stripper is used.

NOTE 3 Local air extraction units can be used during thermal stripping.

5.5.6.2 Precision mechanical cutting-type strippers

ECSS-Q-ST-70-61_1510071

a. Mechanical strippers shall be of the following types:

   1. Automatic power-driven strippers with precision, factory-set, cutting, and stripping dies and wire guards, or
   2. Precision-type hand strippers with accurately machined and factory-pre-set cutting heads.

      NOTE Figure 5-2 shows an example of acceptable mechanical strippers.

ECSS-Q-ST-70-61_1510072

b. Stripping tools or machines shall fit the size of the wire conductor.

   NOTE It is good practice to mask off the die openings for wire sizes not in use.

ECSS-Q-ST-70-61_1510073

c. The conductor shall not be twisted, ringed, nicked, cut, or scratched by the process.

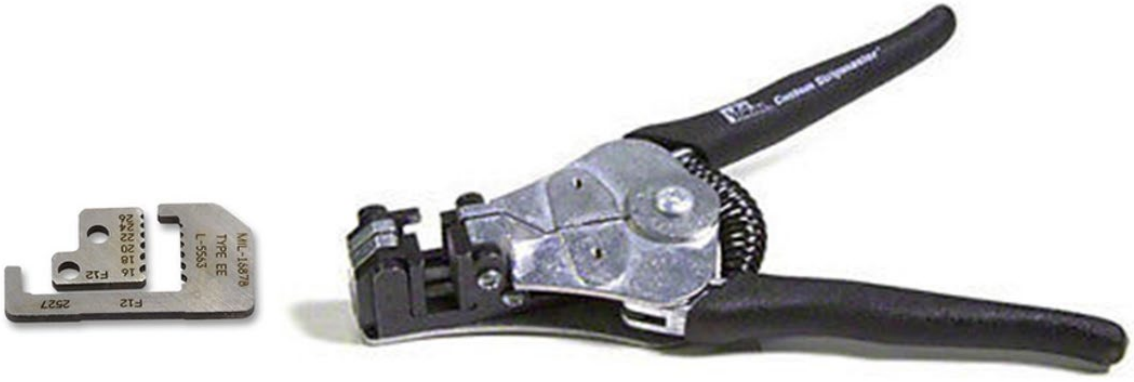


Figure 5-2: Example of suitable mechanical strippers

5.5.6.3 Enamel stripping for wires

ECSS-Q-ST-70-61_1510074

a. The enamel shall be removed by chemical or thermal means.

ECSS-Q-ST-70-61_1510075

b. The enamel may be removed by mechanical means provided that visual inspection using a minimum magnification of x40 is carried out to confirm absence of damage of the conductor.

ECSS-Q-ST-70-61_1510076

c. When stripping the ends of enamel wires the complete removal of the enamel shall be verified by visual inspection.

ECSS-Q-ST-70-61_1510077

d. Chemical stripping materials shall be completely neutralised and be cleaned such that there are no residues from the stripping, neutralizing, or cleaning steps.

ECSS-Q-ST-70-61_1510078

e. The enamel shall not be visually contaminated by the stripping process.

5.5.6.4 Verification of stripping tools

ECSS-Q-ST-70-61_1510079

a. Thermal and mechanical stripping tools shall be verified by removal of insulation at the start of each production batch.

5.5.7 Hot air blower

ECSS-Q-ST-70-61_1510080

a. Hot air blower shall be used for shrinking of sleeves

ECSS-Q-ST-70-61_1510081

b. Hot air blower may be used for removal of some adhesives

ECSS-Q-ST-70-61_1510082

c. Hot air blower shall be able to maintain and control a defined temperature.

ECSS-Q-ST-70-61_1510083

d. Temperature of the hot air blower shall be set at a temperature in compliance with the materials and not degrade surrounding assembly or materials.

NOTE it is good practice to have a thermocouple around to ensure absence of degradation.

ECSS-Q-ST-70-61_1510084

e. Hot air blower shall meet requirement 5.5.1d against ESD.

5.5.8 Soldering tools

5.5.8.1 General

ECSS-Q-ST-70-61_1510085

a. The leads shall not be damaged during preparation and assembly.

5.5.8.2 Holding tools

ECSS-Q-ST-70-61_1510086

a. Holding tools used as soldering aids shall not be wetted by the solder during the assembly.

5.5.8.3 Thermal shunts

ECSS-Q-ST-70-61_1510087

a. A thermal shunt shall be able to act as heat sink to protect thermally sensitive components.

NOTE 1 An effective clamp-type thermal shunt can be constructed by inserting small copper bars into the jaws of an alligator clip.

NOTE 2 Shunts can be held in place by friction, spring tension or any other means that does not damage the finish or insulation.

5.5.8.4 Anti-wicking tools

ECSS-Q-ST-70-61_1510088

a. The conductor gauge sizes of the anti-wicking tools shall be marked on the tool.

NOTE Anti-wicking tools can be used for pretinning the stranded wires.

5.5.8.5 Soldering irons

ECSS-Q-ST-70-61_1510089

a. The size and shape of the soldering iron and tip shall not damage adjacent areas or connections during soldering operations.

ECSS-Q-ST-70-61_1510090

b. Temperature-controlled soldering irons shall be used.

ECSS-Q-ST-70-61_1510091

c. Temperature of the solder tip shall be verified once a week and after each solder tip change.

ECSS-Q-ST-70-61_1510092

d. Selected temperature of the solder tip shall remain within +/-10°C.

ECSS-Q-ST-70-61_1510093

e. Resistance between the soldering tip and the workstation grounding point shall be compliant with IPC- J/STD/001H Sept 2020.

ECSS-Q-ST-70-61_1510094

f. AC and DC current leakage from heated tip to ground shall not create deleterious effects on equipment or components.

ECSS-Q-ST-70-61_1510095

g. Tip transient voltages generated by the soldering equipment shall not exceed 2 V peak under a minimum loading impedance of 100 kΩ.

ECSS-Q-ST-70-61_1510096

h. A soldering iron holder shall be used.

NOTE It is good practice to use a cage-type holder that leaves the soldering-iron tip unsupported when a temperature-controlled soldering iron is used.

5.5.9 Baking and curing ovens

ECSS-Q-ST-70-61_1510097

a. An oven for baking and curing shall be able to heat and maintain the temperature of a printed circuit board or assembly within ±10 °C.

NOTE 1 It is good practice to take into account the size and number of objects to be heated, when selecting capacity and size of the oven.

NOTE 2 A vacuum oven can be used for drying operation.

ECSS-Q-ST-70-61_1510098

b. An oven used for silicone shall not be used to bake out PCBs.

ECSS-Q-ST-70-61_1510099

c. An oven used for silicone shall not be used to cure adhesives other than silicone.

ECSS-Q-ST-70-61_1510100

d. The oven shall be equipped with an independent automatic shutdown system to protect from overheating.

5.5.10 Solder deposition equipment

ECSS-Q-ST-70-61_1510101

a. Equipment used to deposit solder pastes shall be of a screening, stencilling, dispensing, roller coating, dotting or jet printing type.

ECSS-Q-ST-70-61_1510102

b. Solder deposit equipment shall deposit reproducible amount of solder paste.

NOTE The use of Solder Paste Inspection (SPI) equipment helps to ensure reproducible volume of deposited solder paste.

ECSS-Q-ST-70-61_1510103

c. Equipment shall apply pastes of a viscosity and quantity such that the positioned component is retained on the board before and during soldering operations, ensuring self-centring and solder fillet formation.

ECSS-Q-ST-70-61_1510104

d. Equipment used to apply solder preforms shall align the preform with the land or component lead and termination.

ECSS-Q-ST-70-61_1510105

e. Solder paste deposition procedures and associated acceptance criteria shall be controlled and documented.

5.5.11 Automatic component placement equipment

ECSS-Q-ST-70-61_1510106

a. Automatic or computer-controlled equipment used for component placement shall be of the coordinate-driven pick-and-place type or of the robotic type.

ECSS-Q-ST-70-61_1510107

b. The placement equipment used shall be of a type that:

1. prevents component or board damages,
2. indexes components with respect to the circuit and
3. aligns the component terminations with the board terminal areas.

5.5.12 Dynamic wave-solder machines

ECSS-Q-ST-70-61_1510108

a. Dynamic soldering machines shall be of automatic type and of a design offering the following:

1. Controlling the flux application.
2. Controlling preheating to drive off volatile solvents and to avoid thermal shock damage to the PCB and component packages.
3. Maintaining the solder temperature at the printed circuit board assembly to within ±5°C of the established bath temperature throughout the duration of any continuous soldering run when measured 3,0 mm below the surface of the wave.
4. Having a wave system that limits shadowing and allows solder fillet formation.
5. Having carriers made from a material that cannot contaminate, degrade or damage the printed circuit board or substrate nor transmit vibration or shock stress from the conveyors to a degree permitting physical, functional or electrostatic damage to components, board or substrate during transport through preheating, soldering and cooling stages.
6. Showing an extraction system, either integral or separate, conforming to the requirements of clause 5.2.

NOTE to item 4: It is good practice to use nitrogen atmosphere.

ECSS-Q-ST-70-61_1510109

b. The following wave soldering machine parameters shall be controlled:

1. the amount of flux and its coverage,
2. the preheat temperature and duration to avoid damage to the PCB and to the component packages,
3. the solder temperature so that the solder in the wave making contact with the board is 235 °C to 275 °C.

ECSS-Q-ST-70-61_1510110

c. The supplier shall provide evidence that:

1. the conveyor speed does not vary by more than ±5 %, and
2. the height of the solder wave remains to a constant pre-selected value across the width of the wave.

5.5.13 Selective wave solder equipment

ECSS-Q-ST-70-61_1510111

a. Selective wave soldering machines shall be of automatic type and of a design offering the following:

1. A holding mechanism for the board to be soldered, which can fixate the board during the process, without degrading or damaging the PCB or the mounted components.
2. Nozzle, through which a local solder wave applies solder selectively per component or termination, from the solder side of the PCB to the component leads to be soldered.
3. Automatic relative movement between nozzle and PCB both in-plane and out-of-plane direction.
4. Controllable flux application.
5. Maintain the preheating temperature to within ±5 °C during soldering to avoid thermal shock damage to the PCB and to component packages.
6. Maintaining the wave solder temperature to within ±5 °C of the established soldering temperature throughout the process.
7. Showing an extraction system, either integral or separate, conforming to the requirements of clause 5.2.

NOTE to item 2: It is good practice to use local flow of nitrogen around the solder nozzle.

ECSS-Q-ST-70-61_1510112

b. The following selective wave soldering machine parameters shall be controlled:

1. the amount of flux and its coverage,
2. the preheat temperature,
3. the solder temperature so that the solder in the selective wave making contact with the board is maximum 300 °C,
4. the nozzle speed so that the soldering time per lead does not exceed 10 s.

5.5.14 Reflow process equipment

5.5.14.1 Condensation (vapour phase) reflow machines

ECSS-Q-ST-70-61_1510113

a. Condensation reflow machines shall:

1. not transmit a movement or vibration into the assemblies being soldered that result in misalignment of components or disturbed solder joints,
2. be capable of preheating an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering,
3. use a reflow fluid whose boiling point is a minimum of 17 °C above the melting point of the solder being used,
4. maintain the preselected temperature to within ±5 °C in the reflow zone during soldering,
5. include an extraction system that conforms to clause 5.2.

NOTE to item 3: For boards with high thermal mass or for mixed terminations finish on components, it is a good practice to select a higher peak temperature and to use a delta of 30°C for a good wettability.

ECSS-Q-ST-70-61_1510114

b. Reflow process parameters for condensation reflow machines shall be controlled and documented according to clause 5.5.14.5.

5.5.14.2 Local hot gas reflow machines

ECSS-Q-ST-70-61_1510115

a. Local hot gas reflow machines shall:

1. not transmit movement or vibration to the assemblies being soldered which result in misalignment of components or disturbed solder joints,
2. preheat an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering,
3. heat the area of the assembly to be soldered using focused or unfocussed energy, to a preselected temperature that is a minimum of 30°C above the melting point of the solder being used as measured at laminate or substrate surface,
4. prevent the reflow of adjacent components and components localized on the opposite side,
5. prevent excessive temperature that can degrade surrounding materials such as adhesive, underfill,
6. Not to be above maximum allowed component temperature,

7. maintain the preselected reflow temperature within ±5°C as measured at the substrate surface.

ECSS-Q-ST-70-61_1510116

b. Reflow process parameters for local hot gas reflow machines shall be controlled and documented according to clause 5.5.14.5.

5.5.14.3 Forced convection and infrared reflow systems

ECSS-Q-ST-70-61_1510117

a. Forced convection and infrared reflow machines shall be of design such that the system:

1. provides a controlled temperature profile and does not transmit movement or vibration into the assembly being soldered,
2. preheats an assembly with solder paste to the temperature recommended by the solder paste manufacturer prior to soldering,
3. heats the area of the assembly to be soldered using focused or unfocussed energy, to a preselected temperature that is a minimum of 30°C above the melting point of the solder being used as measured at laminate or substrate surface,
4. maintains the preselected temperature to within ±5 °C in the reflow zone during soldering,
5. not transmit movement or vibration to the assemblies being soldered which result in misalignment of components or disturbed solder joints.

ECSS-Q-ST-70-61_1510118

b. Reflow process parameters for forced convection and infrared reflow systems shall be controlled and documented according to clause 5.5.14.5.

5.5.14.4 Other equipment for reflow soldering

ECSS-Q-ST-70-61_1510119

a. Other solder reflow systems may be approved for use by the Approval Authority under the condition that they meet the requirements of either clause 5.5.14.1, 5.5.14.2 or 5.5.14.3.

5.5.14.5 Reflow process control parameters

ECSS-Q-ST-70-61_1510120

a. The following reflow process parameters shall be controlled and documented:

1. preheat temperature to avoid damage to the PCB, to the component packages and to reduce the solder dwell time,
2. solder reflow parameters and cooling parameters to stay inside the solder paste requirements,

3. reflow temperature to be maintained within ±5 °C of the verified soldering temperature throughout the process,
4. peak temperature is within the range of 200°C minimum and 235°C maximum, tolerances of point 3 included when measured at PCB level.
5. capability to heat the soldering elements as PCB, components and to retain the present temperature within ±5 °C, and
6. conveyor speed not to vary by more than ±5 %.

NOTE 1 to item 3 and 4: It is good practice to use nitrogen if forced convection oven is used.

NOTE 2 to item 1 and 6: It is good practice to apply a preheating rate of 2 °C ±0,5 °C/mn.

5.5.15 Depanelization tool

ECSS-Q-ST-70-61_1510121

a. To prevent any damage on assembled PCB during depanelization, tools shall be able to meet following requirements:
   1. support PCBs to avoid bending and damage from vibration during process,
   2. guide cutting tool to avoid damage on PCB,
   3. use a local protection to avoid contamination,
   4. be a reproducible depanelization process.

5.5.16 Cleanliness testing equipment

ECSS-Q-ST-70-61_1510122

a. Cleanliness testing equipment shall be able to:
   1. test the cleanliness of bare and assembled printed circuit boards,
   2. be sensitive enough to fulfil requirement 11.1.4e.2,
   3. meet the requirements of IPC-TM-650 Method 2.3.25.

5.5.17 Optical microscope

ECSS-Q-ST-70-61_1510123

a. Optical microscope used for visual inspection shall provide optical magnification from 4x to 40x.

ECSS-Q-ST-70-61_1510124

b. Optical microscope used for failure analysis shall provide, in addition to requirement 5.5.17a, an optical magnification from 50x to 500x.

5.5.18 Automatic Optical Inspection (AOI) equipment

ECSS-Q-ST-70-61_1510125

a. AOI shall not replace final visual inspection.

NOTE AOI is an aid for inspection.

ECSS-Q-ST-70-61_1510126

b. AOI equipment should be capable of detecting the following defects:

1. Missing component
2. Wrong type of component
3. Wrong polarization
4. Component upside down
5. Misplacement
6. Tombstoning or component placed on its edge
7. Solder bridging
8. Lack of solder
9. Shape of solder joint when using a 3D AOI equipment.

5.5.19 X-ray inspection equipment

ECSS-Q-ST-70-61_1510127

a. X-ray equipment shall be equipped with the following:

1. X-ray tube with an acceleration voltage that permitted to provide the required resolution,
2. X-ray tube with micro-focus technology,
3. a digital detector with high resolution, and
4. a system with variable expansion factor.

NOTE X-ray equipment not intended for electronic assemblies or not properly set up can damage sensitive components.

ECSS-Q-ST-70-61_1510128

b. X-ray equipment shall be calibrated to evaluate the total dose received by the components during the inspection.

NOTE To minimize the dose given to the component, it is good practice to:

- Record the total dose received.
- Use off-line image analysis as much as possible.
- Use filters, optimizing the direction of the X-ray beam and masking sensitive areas.

ECSS-Q-ST-70-61_1510129

c. The resolution of the X-ray equipment shall be able to detect solder balls having a diameter of 0,03 mm.

ECSS-Q-ST-70-61_1510130

d. The sensitivity shall be demonstrated by means of actual 0,03 mm diameter solder balls, stuck to adhesive tape, attached to the multilayer board assembly being inspected.

ECSS-Q-ST-70-61_1510131

e. AXI (Automatic X-ray inspection) shall not replace final visual inspection.

NOTE AXI can be used for inline inspection.

ECSS-Q-ST-70-61_1510132

f. AXI equipment should be capable of detecting the following defects:

1. Missing component
2. Component upside down
3. Misplacement
4. Tombstoning or component placed on its edge
5. Solder bridging
6. Lack of solder.

6
Material selection

6.1 General

ECSS-Q-ST-70-61_1510133

a. Material selection shall be in accordance with the requirements of ECSS-Q-ST-70 and ECSS-Q-ST-70-71.

ECSS-Q-ST-70-61_1510134

b. All materials remaining on the assembled board shall be specified in the bill of materials.

ECSS-Q-ST-70-61_1510135

c. Electronic components, mechanical components, printed boards, selected for assembly shall be compatible with all materials and processes, temperature ratings, used to assemble the product.

ECSS-Q-ST-70-61_1510136

d. External finishes of components, subassemblies, assemblies, and hardware for space flight application shall have minimum 3 % Lead in case of tin/lead finish.

ECSS-Q-ST-70-61_1510137

e. Electrical and electronic components identified as having plated or metallized external surfaces with a tin finish containing more than 97 % tin shall be pretinned with a tin-lead solder in accordance with clause 7.6.

NOTE Tin whisker mitigation (barrier methods such as coating or sleeving) is addressed in the framework of an NRB or to the Approval Authority.

ECSS-Q-ST-70-61_1510138

f. Limited shelf-life items shall be handled and stored in accordance with ECSS-Q-ST-70-22 and in accordance with the material manufacturer's recommendations.

6.2 Solder

6.2.1 Form

ECSS-Q-ST-70-61_1510139

a. For soldering, solder paste, ribbon, wire and preforms shall be used provided that the alloy and flux meet the requirements of this standard.

ECSS-Q-ST-70-61_1510140

b. Alloy for use in solder baths, for degolding, pretinning and wave soldering, shall be supplied without flux and be compliant with the requirements of Table 6-1.

NOTE Bars and ingots are example of procured alloys.

6.2.2 Composition

ECSS-Q-ST-70-61_1510141

a. The solder alloy shall have a composition specified in Table 6-1.

NOTE 1 Complementary information can be found in EN-IEC 61190-1-3 for solder and EN-IEC 61190-1-2 for solder paste.

NOTE 2 The solder alloy used depends upon the application. See Annex H for guidelines for the choice of solder type.

ECSS-Q-ST-70-61_1510142

b. In case of use of any solder not listed in Table 6-1, a verification shall be performed in compliance with clause 13.

ECSS-Q-ST-70-61_1510143

c. The metal purity of solder shall be as specified in Table 6-1.

ECSS-Q-ST-70-61_1510144

Table 6-1: Chemical composition of spacecraft solders

ESA designation	Sn min % - max %	Pb max %	In min % - max %	Sb max %	Ag min % - max %	Bi max %	Cu max %	Fe max %	Zn max %	Al max %	As max %	Cd max %	Other max %
PTH and SMD assembly applications													
63 Tin solder Sn63	62,5-63,5	remainder	-	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
62 Tin Silver loaded Sn62	61,5-62,5	remainder	-	0,05	1,8-2,2	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
60 Tin solder Sn60	59,5-61,5	remainder	-	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
Only PTH assembly applications													
96 Tin solder Sn96	remain	0,10	-	0,05	3,5-4,0	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
Only for SMD assembly applications													
75 Indium Lead In75*	max 0,25	remainder	74,0-76,0	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
70 Indium Lead In70*	0,00-0,10	remainder	69,3-70,7	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
50 Indium Lead In50*	0,00-0,10	remainder	49,5-50,5	0,05	-	0,10	0,05	0,02	0,001	0,001	0,03	0,002	0,08
(*): can be for PTH applications providing successful assembly verification													

6.2.3 Storage and handling of paste purity

ECSS-Q-ST-70-61_1510145

a. Manufacturers' instructions shall be applied for the handling and storage of containers of solder paste purchased premixed.

ECSS-Q-ST-70-61_1510146

b. Refrigerated solder paste shall reach room temperature before opening the container.

ECSS-Q-ST-70-61_1510147

c. Purchased premixed paste shall not be used if the use-by date or shelf life recommended by the manufacturer of the paste or paste constituents has expired.

ECSS-Q-ST-70-61_1510148

d. When relifing is performed on purchased premixed paste, and it passes the specified tests, the relifing shelf life shall be half the initial shelf life according to ECSS-Q-ST-70-22 clause 4.1.4

NOTE As an example, for solder paste, solder ball test and viscosity can be part of relifing.

ECSS-Q-ST-70-61_1510149

e. Tools used for removing solder paste from the container shall not contaminate the paste dispensed or that remaining within.

6.3 Fluxes

6.3.1 Rosin based fluxes

ECSS-Q-ST-70-61_1510150

a. Fluxes shall be selected in accordance with Table 6-2.

NOTE 1 Complementary information for fluxes can be found in ISO 9454-1:2016.

NOTE 2 Flux manufacturers are mainly in compliance with IPC J-STD-004B-AM1 (2011).

ECSS-Q-ST-70-61_1510151

b. For soldering the following fluxes shall be selected:

1. As a baseline, use ROL0 pure rosin flux.
2. When ROL1 flux is used, monitor the effectiveness of subsequent cleaning operations in accordance with clause 11.1.2.

ECSS-Q-ST-70-61_1510152

c. High activated rosin-based fluxes shall be stored separately from pure rosin fluxes and low activated rosin fluxes.

NOTE Example: High activated rosin flux ROH1.

ECSS-Q-ST-70-61_1510153

Table 6-2: Fluxes

	IPC J-STD-004B-AM1 (2011) designation	**Equivalent designation from ISO 9454-1:2016**	**Nature**	**Max composition*** (Weight %)
Pretinning				
Normal wetting	ROL0	1111	Rosin	< 0,05 % halide
	ROL1	1122	Rosin	< 0,5 % halide
Difficult wetting	ROM1	1123	Rosin	0,5 % - 2 % halides
Difficult wetting	ROH1	1124	Rosin	≥ 2,0 % halides
Soldering				
Preferred	ROL0	1111	Rosin	< 0,05 % halide
Requiring cleanliness testing	ROL1	1122	Rosin	< 0,5 % halide
* Maximum values of halide contents are based on IPC, which have higher limits than ISO NOTE: Cleaning is mandatory in any case				

6.4 Solvents

ECSS-Q-ST-70-61_1510154

a. Solvents for the removal of grease, oil, dirt, flux, and flux residues shall be electrically non-conductive and non-corrosive.

ECSS-Q-ST-70-61_1510155

b. Solvents shall be efficient such that flux residues are removed according to clause 11.1.2.

ECSS-Q-ST-70-61_1510156

c. Solvents shall not dissolve or degrade the quality of components or materials.

ECSS-Q-ST-70-61_1510157

d. Solvents shall not remove component identification markings.

ECSS-Q-ST-70-61_1510158

e. Containers of solvents shall be labelled.

ECSS-Q-ST-70-61_1510159

f. Solvents shall be maintained in an uncontaminated condition.

ECSS-Q-ST-70-61_1510160

g. Solvents showing visual evidence of contaminants or decomposition shall not be used.

ECSS-Q-ST-70-61_1510161

h. The following solvents shall be used for cleaning in soldering operations:

1. ethyl alcohol, 99,5 % pure by weight or 95 % pure by volume,
2. isopropyl alcohol, 99 % pure,
3. deionized water at a maximum temperature of 40 °C is used for removing certain fluxes provided that the assembly is thoroughly dried directly after cleaning,
4. any mixture of 6.4h.1, 6.4h.2 and 6.4h.3.

ECSS-Q-ST-70-61_1510162

i. Other solvents that pass a compatibility test programme agreed by the Approval Authority may be used.

ECSS-Q-ST-70-61_1510163

j. Solvents shall be selected such that they dry completely.

6.5 Flexible insulation materials

ECSS-Q-ST-70-61_1510164

a. Materials shall have low outgassing properties in accordance with clause 5.5 of ECSS-Q-ST-70-02.

ECSS-Q-ST-70-61_1510165

b. The following flexible insulation materials may be used in a space environment:

1. ETFE, FEP and PTFE.
2. Polyolefin and PVDF (Kynar®) sleeving for heat-shrinkable wire terminations.
3. Irradiated polyethylene, fluorinated resin, and polyimide.

6.6 Terminals

6.6.1 Materials

ECSS-Q-ST-70-61_1510166

a. Terminals shall be made from one of the following materials:

1. Bronze (copper-tin) alloys.
2. Brass (copper-zinc) alloys.

NOTE It is good practice to use bronze terminals.

ECSS-Q-ST-70-61_1510167

b. When a brass terminal is used it shall be plated with a barrier layer of copper or nickel of 3 μm to 10 μm.

NOTE 1 A barrier layer is necessary on brass items to prevent the diffusion, and subsequent surface oxidation, of zinc.

NOTE 2 It is good practice to use a copper barrier layer on brass terminals because nickel is magnetic Terminals shall be tin lead plated with an alloy containing a minimum of 3 % Lead.

NOTE Example: Hot-dipped or reflowed electro-deposited plating.

6.6.2 Tin, silver, and gold-plated terminals

ECSS-Q-ST-70-61_1510168

a. Terminals with pure tin, silver or gold-plated finish shall not be soldered to PCB.

ECSS-Q-ST-70-61_1510169

b. Gold-plated finishes shall be replaced using one of the methods described in clause 7.6.

ECSS-Q-ST-70-61_1510170

c. The maximum gold thickness of the terminal shall be specified in the procurement specification.

ECSS-Q-ST-70-61_1510171

d. Pure tin and silver finishes shall be pretinned according to clause 7.6.4.

6.7 Wires

ECSS-Q-ST-70-61_1510172

a. Wire shall be made from high-purity copper or copper alloy.

ECSS-Q-ST-70-61_1510173

b. The wire shall have one of the following finishes:
   1. Silver-plating of a minimum 2 μm thickness,
   2. Wire-drawn, fused pure tin,
   3. Enamelled.

ECSS-Q-ST-70-61_1510174

c. Wires shall be stripped of their insulation in accordance with clause 7.5.1.

ECSS-Q-ST-70-61_1510175

d. Wires shall be pretinned in accordance with clause 7.6.4.

6.8 Sculptured flex

ECSS-Q-ST-70-61_1510176

a. Sculptured flex shall be designed in conformance with the requirements of clause 8.7 of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-61_1510177

b. Sculptured flex shall be manufactured and procured according to the requirements of ECSS-Q-ST-70-60.

6.9 Printed circuits substrates

6.9.1 Substrates selection

ECSS-Q-ST-70-61_1510178

a. PCBs shall be designed in conformance with the requirements of clause 14 of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-61_1510179

b. PCBs shall be qualified and procured according to the requirements of ECSS-Q-ST-70-60.

ECSS-Q-ST-70-61_1510180

c. Ceramic substrates shall meet the requirements of ECSS-Q-ST-60-05.

6.9.2 Gold finish on PCBs footprint

ECSS-Q-ST-70-61_1510181

a. Degolding of pads shall be performed in accordance with clause 7.6.

NOTE RF circuits with gold finishes (see Table 10-13 of ECSS-Q-ST-70-60) can have their pads selectively plated with a tin-lead finish.

ECSS-Q-ST-70-61_1510182

b. Soldering to gold finish, ENIG, ENIPIG, ENEPIG, qualified according ECSS-Q-ST-70-60, with tin lead may be performed only when the gold finish is thinner than 0,1 μm and is approved by the Approval Authority.

6.9.3 PCB design requirements for wave and selective wave soldering

ECSS-Q-ST-70-61_1510183

a. When wave soldering assembly process is used, PCB design shall be in compliant with requirement 14.3.3f of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-61_1510184

b. The Design constraint specification should at least, include statements about “solder bridging” and “large heat sinks areas.

NOTE Proposed statements are:

- *“Circuit tracks that are spaced close together should be orientated in line with the pass direction of the solder wave to avoid solder bridging.”*
- *“Avoid large heat sink areas for ground planes and leads closely connected to massive metal components.”*

6.10 Components

6.10.1 General

ECSS-Q-ST-70-61_1510185

a. Components termination materials and their finishes shall be selected in compliance with requirements from clause 3 of ESCC23500.

NOTE ESCC 23500 is only applicable for procured components and the reprocessing operations as degolding and pretinning are out of its scope.

ECSS-Q-ST-70-61_1510186

b. In case of not golden termination finish, the lead finish shall be checked as per ESCC 25500 in accordance with requirement 4.3.7b.1(f) from ECSS-Q-ST-60.

ECSS-Q-ST-70-61_1510187

c. Components with Silver Palladium finish shall not be used.

ECSS-Q-ST-70-61_1510188

d. Cleaning processes shall not damage the component.

ECSS-Q-ST-70-61_1510189

e. Reprocessing shall not damage the component.

ECSS-Q-ST-70-61_1510190

f. The supplier shall verify, based on the available documentation, that the processing conditions do not exceed the values given by the individual component data sheets.

NOTE Examples of processing conditions include maximum temperature to avoid internal melting, thermal shocks, thermal damages, removal of marking ink, degradation of encapsulating plastic.

ECSS-Q-ST-70-61_1510191

g. The supplier may exceed the component manufacturer's mandated processing conditions providing the following conditions are met:

1. dedicated tests at component level showing there is no degradation of these components, and
2. customer approval.

ECSS-Q-ST-70-61_1510192

h. The plating of the component lead shall be such that the lead forming does not induce any crack in the plating.

ECSS-Q-ST-70-61_1510193

i. When components initially designed for insertion-mount application are used for surface mounting, the assembly shall not damage neither the component, its leads nor the substrate to which it is assembled.

ECSS-Q-ST-70-61_1510194

j. Components to be mounted shall be designed for and be capable of withstanding the soldering temperatures of the particular process being used for fabrication of the assembly.

NOTE In case surface mounted components are soldered on both sides of the PCB, double reflow processes can be applied.

6.10.2 Moisture sensitive components

ECSS-Q-ST-70-61_1510195

a. Moisture or process sensitive components as classified by IPC/JEDEC J-STD-020, ECA/IPC/JEDEC J-STD-075 shall be handled in a manner consistent with IPC/JEDEC J-STD-033D.

NOTE Any type of plastic encapsulated components with MSL more than 1(one) particularly some plastic BGAs and tantalum capacitors, are moisture sensitive.

ECSS-Q-ST-70-61_1510196

b. When moisture sensitive components are used, bake out shall be performed in accordance with clause 7.4.

6.11 Adhesives, potting, underfill and conformal coatings

ECSS-Q-ST-70-61_1510197

a. Adhesives shall be dispensable, non-stringing, and have a reproducible dot volume and shape after application.

ECSS-Q-ST-70-61_1510198

b. Adhesives, pottings, underfill and conformal coatings shall conform to the outgassing requirements of ECSS-Q-ST-70-02.

ECSS-Q-ST-70-61_1510199

c. Materials covered by this clause shall be individually assessed in accordance with clause 4.2.11 and 4.2.15 of ECSS-Q-ST-70-71 when flammability requirements are applicable.

ECSS-Q-ST-70-61_1510200

d. No materials that emit acetic acid, ammonia, amines, hydrochloric acid, and other acids shall be used.

NOTE Such compounds can cause stress-corrosion cracking of part leads.

7 Preparations prior to mounting and soldering

7.1 General handling

ECSS-Q-ST-70-61_1510201

a. Operators shall use tools that are fit for the purpose and undamaged prior to use.

ECSS-Q-ST-70-61_1510202

b. ESD-sensitive components shall be handled in accordance with clause 5.4.

ECSS-Q-ST-70-61_1510203

c. During assembly, component termination, terminals, wire ends, and PCB termination areas shall not be touched with bare hands.

ECSS-Q-ST-70-61_1510204

d. After final cleaning, personnel working with PCBs shall wear lint-free gloves or finger cots.

7.2 Storage

7.2.1 Components

ECSS-Q-ST-70-61_1510205

a. Storage facilities shall protect components from contaminants and damage.

ECSS-Q-ST-70-61_1510206

b. Storage boxes and bags shall be made of materials which do not degrade the solderability of the components.

ECSS-Q-ST-70-61_1510207

c. Storage materials shall not contain amines, amides, silicones, sulphur, or polysulphides.

ECSS-Q-ST-70-61_1510208

d. Packaging and containers for ESD-sensitive components shall be in accordance with clause 5.4.

7.2.2 PCBs

ECSS-Q-ST-70-61_1510209

a. Bare PCBs shall be stored in accordance with clause 6.12 of ECSS-Q-ST-70-60.

7.2.3 Materials requiring segregation

ECSS-Q-ST-70-61_1510210

a. Solders not in accordance with clause 6.2 shall be removed from the work area.

ECSS-Q-ST-70-61_1510211

b. Activated fluxes shall be stored in accordance with clause 6.3.1c.

NOTE Example: ROH1 flux.

ECSS-Q-ST-70-61_1510212

c. Solvents that do not conform to clause 6.4 shall be removed from the work area.

NOTE Example: Solvents contaminated with impurities such as inorganic acids.

7.3 Baking conditions of PCBs

ECSS-Q-ST-70-61_1510213

a. An oven, as specified in clause 5.5.9, shall be used to bake out PCBs according to requirement 9.2.2a of ECSS-Q-ST-70-60.

ECSS-Q-ST-70-61_1510214

b. Baking of bare PCBs shall be made according to clause 6.12 of ECSS-Q-ST-70-60.

NOTE 1 An alternative good practice to this requirement is: baking for 4 hours at 65 °C in a vacuum oven capable of <50 hPa.

NOTE 2 To prevent delamination of flex material, it is recommended to perform a step baking starting with a low temperature of +80 °C for a minimum of 8 hours and finish at +120 °C for a minimum of 8 hours.

ECSS-Q-ST-70-61_1510215

c. Baking of populated PCBs shall be made when the PCB has been kept under cleanroom conditions for more than 72 hours.

NOTE 1 Storage of PCBs in dry cabinet pauses the accumulated clean room storage time.

NOTE 2 A temperature of 80 °C for 4 hours can be sufficient as bake out for populated PCB

ECSS-Q-ST-70-61_1510216

d. Baking of populated PCB shall be made at a temperature which does not degrade the components or assembly.

NOTE To limit the bake out operation, which can induce later failure, the PCB can be stored in dry environment after the baking.

7.4 Baking and storage of moisture sensitive components

ECSS-Q-ST-70-61_1510217

a. Moisture or process sensitive components, as classified by IPC/JEDEC J-STD-020, and ECA/IPC/JEDEC J-STD-075, shall be stored, handled, and baked consistent with IPC/JEDEC J-STD-033D.

NOTE 1 This is to counteract the "popcorn" effect in soldering using oven or vapor phase reflow techniques.

NOTE 2 Typical baking conditions are from 6 h to 24 h at 125 °C depending on the MSL classification, except for components delivered in reels for which a lower temperature and longer time are used.

NOTE 3 It is good practice to store components under nitrogen, dry air (20 % RH maximum) or partial vacuum. This practice does not replace baking when required by MSL classification.

ECSS-Q-ST-70-61_1510218

b. Baking of moisture sensitive components shall be in conformance with manufacturers recommendations.

7.5 Preparation of components, wires, terminals, and solder cups

7.5.1 Damage to insulation

ECSS-Q-ST-70-61_1510219

a. The remaining conductor insulation shall not be damaged by the insulation removal process.

ECSS-Q-ST-70-61_1510220

b. Conductors with damaged insulation shall not be used.

NOTE 1 Example: Insulation damage includes nicks, cuts, crushing and charring.

NOTE 2 The operation of mechanical stripping tools can leave slight pressure markings in the remaining conductor insulation. This effect is normal.

ECSS-Q-ST-70-61_1510221

c. The insulation material shall not be charred by thermal stripping.

NOTE Discoloration of the insulation material after thermal stripping is normal.

ECSS-Q-ST-70-61_1510222

d. Insulation shall not be melted into the wire strands.

7.5.2 Damage to conductors and braid

ECSS-Q-ST-70-61_1510223

a. The conductor shall not be damaged by the insulation removal process.

NOTE Example: Conductor damage includes twisting, ringing, nicks, cuts, strand separation (birdcaging) or scores.

ECSS-Q-ST-70-61_1510224

b. Components leads with a maximum reduction of 10 % of initial section due to lead forming may be acceptable provided that it is representative of the verified configuration.

ECSS-Q-ST-70-61_1510225

c. Conductors that are reduced in cross-sectional area by the insulation removal process shall not be used.

ECSS-Q-ST-70-61_1510226

d. A maximum of 10 % of section reduction resulting from insulation removal may be considered acceptable provided agreement from the Approval Authority.

NOTE Section reduction can be due to the pressure of the stripping/forming tooling on the conductor combined with the pulling action. Nicks and cuts are considered as damage

ECSS-Q-ST-70-61_1510227

e. Different wires shall not be twisted together.

ECSS-Q-ST-70-61_1510228

f. Enamel wires used for magnetics or single stranded wires, may be twisted provided minimum bending radius is respected according to clause 9.10.

ECSS-Q-ST-70-61_1510229

g. Plated wires where the base material is exposed other than at the cutting surface, shall not be used.

ECSS-Q-ST-70-61_1510230

h. Insulation shall not have uneven or ragged pieces of insulation, like frays, tails or tags, greater than 50 % of the insulation outside diameter or 1 mm, whichever is larger.

7.5.3 Cleaning before soldering

ECSS-Q-ST-70-61_1510231

a. Before assembly, components, wire, terminal, and connector contacts shall be visually examined for cleanliness, absence of oil films and absence from tarnish or corrosion.

ECSS-Q-ST-70-61_1510232

b. Surfaces to be soldered shall be cleaned using solvents specified in clause 6.4.

ECSS-Q-ST-70-61_1510233

c. Abrasives shall not be used for surface to be soldered.

NOTE Abrasives can include pumice, pumice-impregnated erasers, and emery paper.

7.5.4 Insulation clearance

ECSS-Q-ST-70-61_1510234

a. The maximum insulation clearance, measured from the solder joint, shall be as stated in Table 7-1.

ECSS-Q-ST-70-61_1510235

b. For PTFE-insulated wire, the minimum distance between the insulation and the solder fillet shall be 1 mm.

NOTE The minimum clearance distance for PTFE insulation accommodates cold flow.

ECSS-Q-ST-70-61_1510236

c. The wire insulation shall not be in contact with the solder joint.

ECSS-Q-ST-70-61_1510237

Table 7-1: Clearances for insulation

Wire diameter (American Wire Gauge)	**Conductor diameter** d (mm)	**Insulation clearance** (maximum)
32 to 24	0,200 to 0,510	$4 \times d$
22 to 12	0,636 to 2,030	$3 \times d$
≥ 10	≥ 2,565	$2 \times d$

7.5.5 Wire lay

ECSS-Q-ST-70-61_1510238

a. Disturbed lay in stranded wire conductors shall be restored in original position before soldering.

ECSS-Q-ST-70-61_1510239

b. Restoration of the lay shall be done without contaminating the conductor.

ECSS-Q-ST-70-61_1510240

c. The size of wires shall not be modified.

7.6 Degolding and pretinning

7.6.1 General

ECSS-Q-ST-70-61_1510241

a. Gold plated terminations of component shall be degolded and pretinned.

ECSS-Q-ST-70-61_1510242

b. Degolding for gold finishes of thickness less than 0,1 μm may be omitted subject to agreement by the Approval Authority.

ECSS-Q-ST-70-61_1510243

c. Solder alloy used for degolding and pretinning shall be Sn60, Sn62 or Sn63 solder.

ECSS-Q-ST-70-61_1510244

d. Flux shall be removed by means of a cleaning solvent, in compliance with clause 6.4.

ECSS-Q-ST-70-61_1510245

e. Degolding and pretinning temperatures on component terminations shall not exceed the components manufacturer recommendations.

ECSS-Q-ST-70-61_1510246

f. The supplier may exceed the component manufacturer's mandated processing conditions providing the following conditions are met:

1. dedicated tests at component level showing there is no degradation of these components, and
2. customer approval

ECSS-Q-ST-70-61_1510247

g. For temperature sensitive components, thermal shunts, in accordance with clause 5.5.8.3 shall be used.

ECSS-Q-ST-70-61_1510248

h. The use of thermal shunts shall not disturb or damage the solder joint, component or assembly

ECSS-Q-ST-70-61_1510249

i. Pretinning temperature shall not exceed the temperature used for degolding.

ECSS-Q-ST-70-61_1510250

j. The lead forming of components with glass-to-metal lead seals shall be performed before degolding and pretinning.

ECSS-Q-ST-70-61_1510251

k. The lead forming for glass-to-metal leads may be performed after degolding and pretinning provided demonstration of absence of cracks in the leads after lead forming.

ECSS-Q-ST-70-61_1510252

l. The distance of the degolding and pretinning to the component body shall be compliant with the manufacturer's recommendations or procurement specification.

ECSS-Q-ST-70-61_1510253

m. For glass bead component, the distance of the degolding and pretinning to the component body shall be more than 0,75 mm, in case not specified by the component manufacturer.

ECSS-Q-ST-70-61_1510254

n. Pretinning of ceramic chip capacitors shall not be performed.

7.6.2 Solder baths method for degolding and pretinning of components terminations and terminals

ECSS-Q-ST-70-61_1510255

a. Solder baths used for degolding and pretinning shall be in accordance with Table 7-2.

ECSS-Q-ST-70-61_1510256

b. For the pretinning of component terminations, metallised terminations and terminal posts low activated rosin-based fluxes shall be used.

NOTE ROL0 or ROL1 are types of flux compliant to the requirement.

ECSS-Q-ST-70-61_1510257

c. In case pretinning with low activated rosin-based flux does not give acceptable wetting, moderate rosin-based flux ROM1 may be used except for wires, providing demonstration of sufficient cleanliness.

ECSS-Q-ST-70-61_1510258

d. In case pretinning with moderate rosin-based flux ROM1 does not give acceptable wetting, high activated rosin-based flux ROH1 may be used only for mechanical parts, providing demonstration of sufficient cleanliness.

NOTE ROH1 flux is extremely aggressive and can cause corrosion and damage to electronic materials.

ECSS-Q-ST-70-61_1510259

e. A controlled method shall be established and implemented for the replacement of solder baths, based on either:

1. **Contaminants**: Replace the solder bath alloy when the contaminants limits given in Table 7-2 are exceeded, or
2. **Time**: Establish a schedule of solder-bath replacement with justification of the replacement frequency.

ECSS-Q-ST-70-61_1510260

f. Degolding and pretinning shall be performed according to the following sequence:

1. ROL0 or ROL1 flux is applied to area to be degolded.
2. Surface impurities are removed from the bath surface before use.
3. Gold-plated component terminations and terminals are dipped into degolding solder bath for a time between 2 (two) seconds and 4 (four) seconds.
4. ROL0 or ROL1 flux is applied to degolded area once the lead has cooled down.
5. The fluxed area is dipped into pretinning solder bath for a time between 2 (two) seconds and 4 (four) seconds.
6. The component leads are cooled before cleaning.

NOTE Rapid cooling by contact with cleaning solvents can crack packages or glass-to-metal seals.

ECSS-Q-ST-70-61_1510261

g. The cross-sectional area of terminations shall not be reduced by dissolution into the solder bath below the minimum values of specification.

ECSS-Q-ST-70-61_1510262

Table 7-2: Solder baths parameters for degolding and pretinning

Parameter	Degolding	Pretinning
Use	Gold dissolution	Pretinning
Temperature range (°C)	245 to 280	210 to 280
Time	2 to 5 seconds	2 to 5 seconds
Contaminants limits (weight %)	Au < 1	Cu < 0,25 ; Au < 0,2; (Cu + Au) < 0,3; Zn, Al and Fe: traces.

7.6.3 Solder iron method for degolding and pretinning

7.6.3.1 PCB

ECSS-Q-ST-70-61_1510263

a. For degolding, solder shall be melted onto the conductor using a soldering iron tip with temperature lower than or equal to 330 °C.

ECSS-Q-ST-70-61_1510264

b. Solder shall be wicked-out using copper braid.

ECSS-Q-ST-70-61_1510265

c. For pretinning, solder shall be applied on the PCB conductor using a solder iron tip with temperature lower than or equal to 330 °C.

ECSS-Q-ST-70-61_1510266

d. Pretinning of the PCB pad shall be made after removal of an assembled part prior to new part to be assembled.

7.6.3.2 Components terminations

ECSS-Q-ST-70-61_1510267

a. For degolding, solder shall be melted onto the component termination using a soldering iron tip with temperature either lower than or equal to 330 °C or maximum temperature recommended by the component manufacturer.

ECSS-Q-ST-70-61_1510268

b. Solder shall be wicked-out using copper braid.

ECSS-Q-ST-70-61_1510269

c. For pretinning, solder shall be melted onto the component termination using a soldering iron tip with temperature either lower than or equal to 330 °C or maximum recommended by the component manufacturer

7.6.3.3 Solder cup

ECSS-Q-ST-70-61_1510270

a. For degolding, solder shall be melted inside the solder cup.

ECSS-Q-ST-70-61_1510271

b. The edge of the cup shall be degolded to provide evidence that degolding was performed.

ECSS-Q-ST-70-61_1510272

c. Solder shall be wicked-out using stranded wire or copper braid.

ECSS-Q-ST-70-61_1510273

d. For pretinning, solder shall be applied inside the solder cup.

ECSS-Q-ST-70-61_1510274

e. Excess of solder shall be removed with stranded wires or copper braid.

7.6.4 Pretinning processes

7.6.4.1 Pretinning of pure tin finish component leads

ECSS-Q-ST-70-61_1510275

a. Pure tin component terminations shall be pretinned with full tin lead solder coverage.

ECSS-Q-ST-70-61_1510276

b. Reprocessed pure tin component terminations shall be in compliance with requirements from clauses 7.6.2, 7.6.3.2 from this standard and requirement 8.1a from ECSS-Q-ST-60-13.

ECSS-Q-ST-70-61_1510277

c. Reprocessing process shall be verified by microsectioning and SEM/EDX with respect to alloying and full coverage.

7.6.4.2 Solder bath method for pretinning of stranded wires

ECSS-Q-ST-70-61_1510278

a. The insulation materials shall be removed in accordance with clause 7.5.1.

ECSS-Q-ST-70-61_1510279

b. For pretinning of insulated wires ROL0 flux shall be used.

ECSS-Q-ST-70-61_1510280

c. For pretinning of insulated wires, ROL1 flux may be used provided that ingress of flux under insulation is prevented.

ECSS-Q-ST-70-61_1510281

d. The fluxed area shall be dipped into pretinning solder bath in compliance with Table 7-2 for a time between 3 (three) seconds and 5 (five) seconds.

NOTE Pretinning promotes solderability and prevents untwisting or separation stranded wires.

ECSS-Q-ST-70-61_1510282

e. The cross-section diameter of wires shall not be reduced by dissolution into the solder bath more than 10 % or below the minimum values of wire manufacturer specification.

ECSS-Q-ST-70-61_1510283

f. Solder shall not flow under insulation.

NOTE It is good practice to use antiwicking tools to prevent the solder flow.

7.6.4.3 Solder iron method for pretinning of wires and braids

ECSS-Q-ST-70-61_1510284

a. Wires and braids may be pretinned by applying solder to the wire using a heated soldering-iron tip.

ECSS-Q-ST-70-61_1510285

b. For pretinning of insulated wires ROL0 flux shall be used.

ECSS-Q-ST-70-61_1510286

c. No flux shall be used for pretinning and soldering of braid except the one included in the solder wire.

ECSS-Q-ST-70-61_1510287

d. Solder shall be melted onto the conductor using a heated soldering iron to a maximum temperature of 330 °C.

ECSS-Q-ST-70-61_1510288

e. Solder shall be wicked-out using stranded wire or solder wick.

7.6.4.4 Requirements for pretinning of wires

ECSS-Q-ST-70-61_1510289

a. Solder shall penetrate to the inner strands of stranded wire.

ECSS-Q-ST-70-61_1510290

b. Solder shall not be in contact with the insulation.

NOTE Flow of solder (wicking) beyond the insulation can reduce the flexibility of the wire.

ECSS-Q-ST-70-61_1510291

c. The insulation shall not be damaged by the pretinning.

ECSS-Q-ST-70-61_1510292

d. Cleaning solvent shall not flow under the wire insulation.

NOTE Application using a lint-free cloth can limit the flow of solvent.

7.7 Preparation of the soldering tip

ECSS-Q-ST-70-61_1510293

a. The soldering tip shall be fitted in accordance with the equipment manufacturer's specification.

ECSS-Q-ST-70-61_1510294

b. Deposits and oxidation products shall be removed using a brass or copper metal sponge or moist sponge.

NOTE Build-up of oxidation products can reduce the ability of the tip to transfer heat.

ECSS-Q-ST-70-61_1510295

c. Adherent deposits may be removed using abrasive paper of grain size 600 or finer.

ECSS-Q-ST-70-61_1510296

d. Files shall not be used for dressing plated copper soldering-iron.

ECSS-Q-ST-70-61_1510297

e. Plated tips shall be examined for cracking.

NOTE Cracked platings allow the liquid solder to alloy with and erode the underlying copper, forming intermetallics which reduce heat transfer and lead to unacceptable joints.

ECSS-Q-ST-70-61_1510298

f. Prior to examination for cracked solder tip surface, solder obscuring the surface shall be removed when the iron is hot by wiping the tip with moist, lint-free, sponge material.

ECSS-Q-ST-70-61_1510299

g. Solder tips with cracked platings shall be removed from the soldering area.

ECSS-Q-ST-70-61_1510300

h. Soldering iron tip shall be pretinned before soldering.

NOTE Pretinning prevents oxidation of the tip.

8
Components mounting requirements prior to soldering

8.1 General requirements

ECSS-Q-ST-70-61_1510301

a. The forming of terminations shall be compliant with the component manufacturer's recommendations.

ECSS-Q-ST-70-61_1510302

b. When staking, bonding or underfill are performed before soldering, it shall be performed in accordance with clause 11.2. and clause 11.3

NOTE Staking, bonding or underfill can be applied before or after soldering depending on configuration.

ECSS-Q-ST-70-61_1510303

c. The spacing between conductive elements shall not be reduced below the minimum electrical spacing specified in clauses 13.8, 13.9, 13.10 and 14.3 of ECSS-Q-ST-70-12.

NOTE Some surface mounted components that are not bonded to the PCB can self-align during the soldering process. It is the registration after soldering that is important.

8.2 Mounting of through hole components

8.2.1 General

ECSS-Q-ST-70-61_1510304

a. Through hole components shall be mounted in plated through holes except as specified in clause 8.2.8.3.

ECSS-Q-ST-70-61_1510305

b. Distance between the bottom of the component body and the mounting surface shall be less than 3,5 mm.

NOTE 1 Axial components can be mounted in contact with PCB surface when stress relief is not negated by the solder joint.

NOTE 2 Mechanical support can be necessary independently of the weight of the device.

ECSS-Q-ST-70-61_1510306

c. For components with stress relief, the distance between the bottom of the component body and the mounting surface may be up to 5 mm.

ECSS-Q-ST-70-61_1510307

d. Soldered terminations shall not be cut after the soldering operation.

NOTE Component leads and wires are cut and shaped before soldering.

ECSS-Q-ST-70-61_1510308

e. The component mounting shall be adapted so that the solder joints do not come in contact with the component body or welded area.

ECSS-Q-ST-70-61_1510309

f. The component mounting shall be adapted so that the solder joints do not negate the stress relief.

8.2.2 Heavy components

ECSS-Q-ST-70-61_1510310

a. Components weighing more than 5g shall be supported by either one of the following methods:

1. adhesive compounds in accordance with clause 6.11, or
2. mechanical methods.

NOTE For example: lacing.

ECSS-Q-ST-70-61_1510311

b. The support method shall not impose stresses that result in functional degradation or damage to the part or assembly.

ECSS-Q-ST-70-61_1510312

c. The support method shall not impair stress relief designs.

8.2.3 Metal-case components

ECSS-Q-ST-70-61_1510313

a. Metal-case components shall be electrically insulated using space-approved materials when they are mounted over conductors on the external layer of the PCB, in close vicinity of another metal-case component or in contact with a conductive material from another component.

ECSS-Q-ST-70-61_1510314

b. Metal-cased components shall not be mounted over soldered connections.

ECSS-Q-ST-70-61_1510315

c. Component identification marks shall not be obscured by the insulation.

NOTE For example, the serial numbers.

8.2.4 Glass-encased components

ECSS-Q-ST-70-61_1510316

a. Glass-encased components shall be enclosed with sleeving when epoxy material is used for staking, conformal coating or encapsulating.

NOTE Epoxy material cannot be applied directly to the glass.

ECSS-Q-ST-70-61_1510317

b. Glass-encased components may be enclosed in resilient transparent sleeving or in heat-shrinkable sleeving.

NOTE Heating and shrinkage of sleeving can damage glass-encased components.

8.2.5 Stress relief of components with bendable leads

ECSS-Q-ST-70-61_1510318

a. Stress relief shall be incorporated into leads to be soldered and conductors as well as interfacial connections except for requirement 8.2.5b and requirements from clause 8.2.6.

NOTE 1 Stress relief provides freedom of movement for component leads or conductors between points of constraint.

NOTE 2 Stresses can arise between points of constraint due to mechanical loading or temperature variations.

NOTE 3 Examples of stress relief methods are shown in Figure 8-3 and Figure 8-8.

ECSS-Q-ST-70-61_1510319

b. The assembly of TO-39, and CKR-06 packages shall be performed in accordance with Figure 8-1when assembled without stress relief.

ECSS-Q-ST-70-61_1510320

c. TO-39 and CKR-06 packages shall be adhesively staked in accordance with Figure 8-1.

NOTE The use of a filler (silica powder) can prevent excessive flow of adhesive.

ECSS-Q-ST-70-61_1510321

d. TO-39 and CKR-06 packages assembled in configuration presented in Figure 8-1 may be used without assembly verification provided mechanical fixation.

ECSS-Q-ST-70-61_1510322

e. Underfill, bonding or potting of PTH packages as presented in Figure 8-2 may be used if verified according to clause 13.

ECSS-Q-ST-70-61_1510323

f. Stress relief designs shall not damage the assembly.

NOTE Long lead lengths or large loops between constraint points can vibrate and damage the assembly.

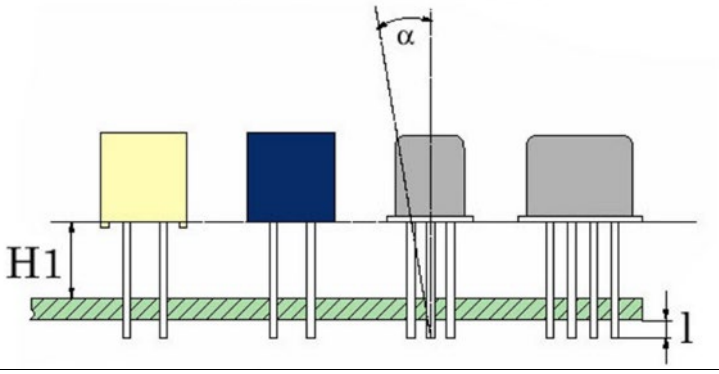
ECSS-Q-ST-70-61_1510324

g. Leads shall not be temporarily constrained against spring-back force during soldering.

NOTE Residual stresses are produced in the lead material or solder joint.

ECSS-Q-ST-70-61_1510325

h. Solder fillets shall not impair stress relief bends.



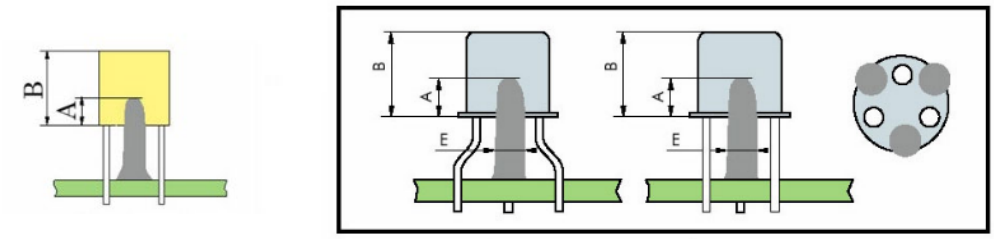
Mounting without spacer: 2,4 mm ≤ H1 ≤ 3 mm

Mounting with spacer: 2 mm ≤ H1 ≤ 3,5 mm

l: see Figure 8-6

$\alpha \leq 10°$

Dimensional limits



Preferred A > = 1/3 B

a) Adhesively staked TO package

b) Adhesively staked CKR06

ECSS-Q-ST-70-61_1510326

Figure 8-1: Assembly of TO-39 and CKR06

ECSS-Q-ST-70-61_1510327

Figure 8-2: TO package with underfill

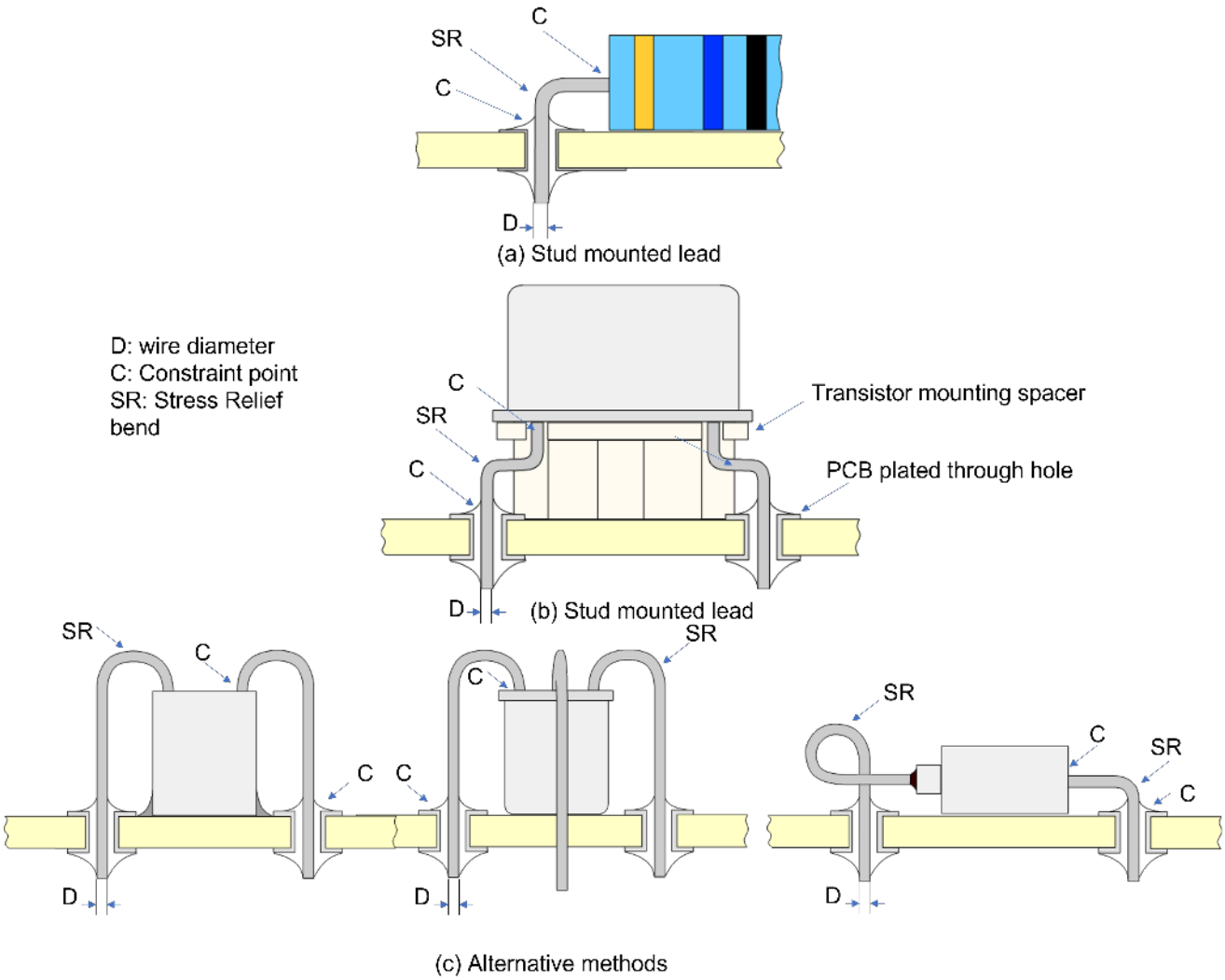


Figure 8-3: Methods for incorporating stress relief with components having bendable leads

8.2.6 Stress relief of components with non-bendable leads

ECSS-Q-ST-70-61_1510328

a. Stress relief for components with non-bendable leads mounted in contact with the PCB or adhesively bonded to the PCB shall use wire extensions according to Figure 8-4.

NOTE Bending can damage components when lead diameters are large, or components have delicate seals or where lead-material composition makes bending impracticable.

ECSS-Q-ST-70-61_1510329

b. Dual in Line Package components shall assembled such that tapered portions of the leads are clear of solder.

NOTE To achieve acceptable stand-off, a shim can be used

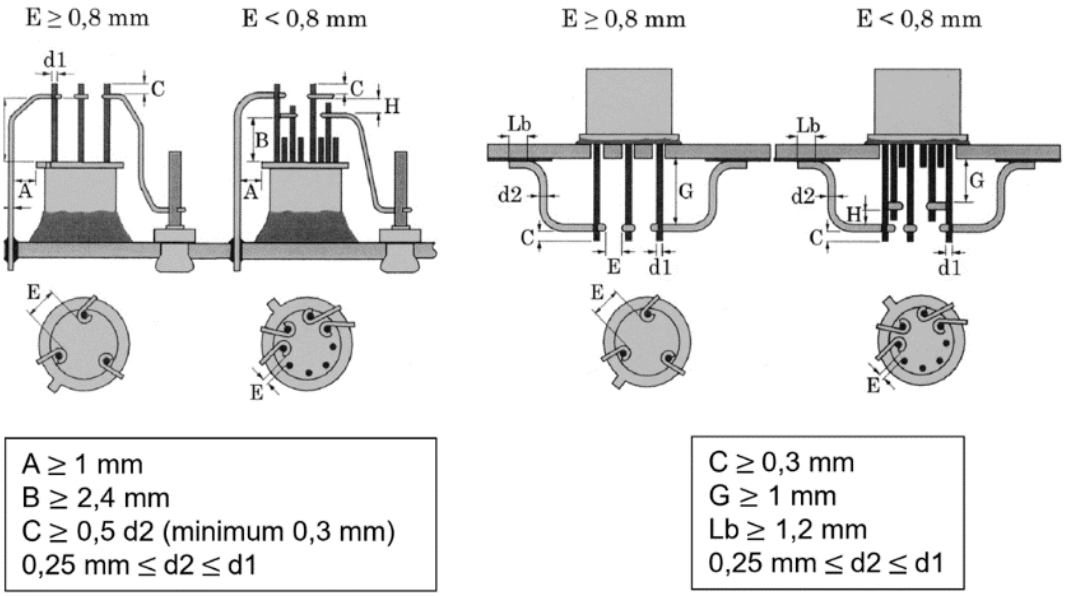
ECSS-Q-ST-70-61_1510330

c. Dual in Line Package components with more than 24 leads shall be assembly verified in accordance with clause 13.

ECSS-Q-ST-70-61_1510331

d. Components sensitive to vibrations and shock tests shall not be assembled as described in requirement 8.2.6a.

NOTE Examples of such sensitive components are: relays, oscillators, crystals. ECSS-E-HB-32-25A is providing a list of components known as sensitive to vibration and shock.



ECSS-Q-ST-70-61_1510332

Figure 8-4: Methods for attaching wire extensions to non-bendable leads

8.2.7 Bending of component leads

ECSS-Q-ST-70-61_1510333

a. During bending, component leads shall be supported to avoid axial stress and damage to seals or internal bonds.

ECSS-Q-ST-70-61_1510334

b. The inside radius of a bend shall not be less than one time the lead diameter.

ECSS-Q-ST-70-61_1510335

c. The distances between the bends and the end seals at either end of an axial component shall be similar.

ECSS-Q-ST-70-61_1510336

d. The minimum distance from the bend to the end seal shall be two times the lead diameter for round leads in accordance with Figure 8-5(a).

ECSS-Q-ST-70-61_1510337

e. Where the component lead is welded the minimum distance to the bend shall be measured from the weld in accordance with Figure 8-5(b).

NOTE Example: Tantalum capacitors.

ECSS-Q-ST-70-61_1510338

f. Bending tools shall not impinge on the weld.

ECSS-Q-ST-70-61_1510339

g. Leads of dual-in-line and other multileaded components may be mechanically re-aligned with each other, prior to assembly provided that the lead to package connection is not subjected to plastic deformation.

NOTE Dedicated tool can be used to avoid any deformation in plastic area of the lead to package connection.

ECSS-Q-ST-70-61_1510340

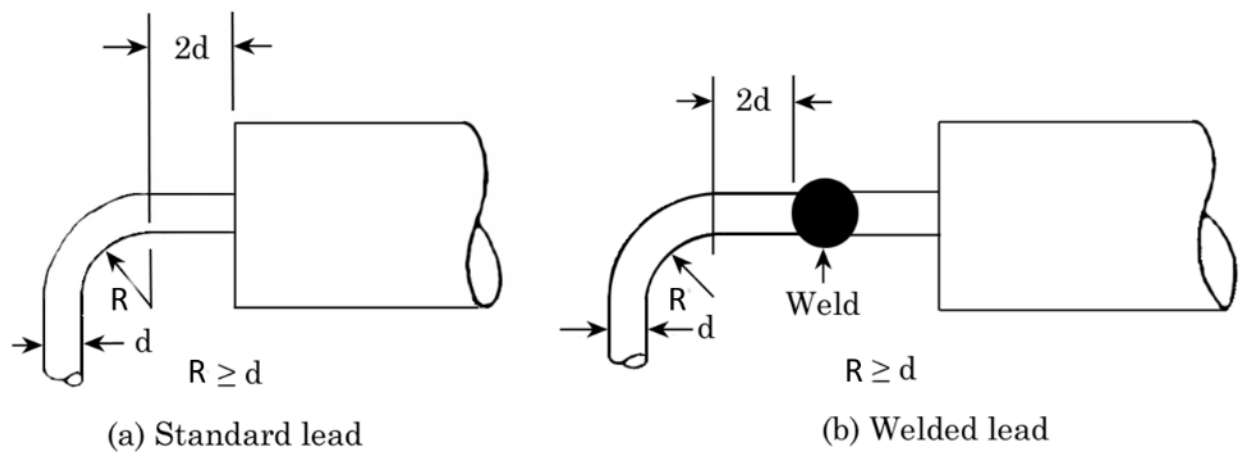
h. Re-alignment of leads described in requirement 8.2.7g shall be documented in PID.

ECSS-Q-ST-70-61_1510341

i. Lead forming shall be symmetrical.

ECSS-Q-ST-70-61_1510342

j. Formed leads shall not be re-bent.



ECSS-Q-ST-70-61_1510343

Figure 8-5: Minimum lead bend

8.2.8 Lead attachment to PCBs

8.2.8.1 General

ECSS-Q-ST-70-61_1510344

a. Direct connection of through hole component leads to PCB shall be performed by stud or clinched lead configuration.

NOTE Component leads can be connected with wire extensions with stress relief.

ECSS-Q-ST-70-61_1510345

b. Soldered terminations shall be visible for inspection after soldering.

8.2.8.2 Stud leads

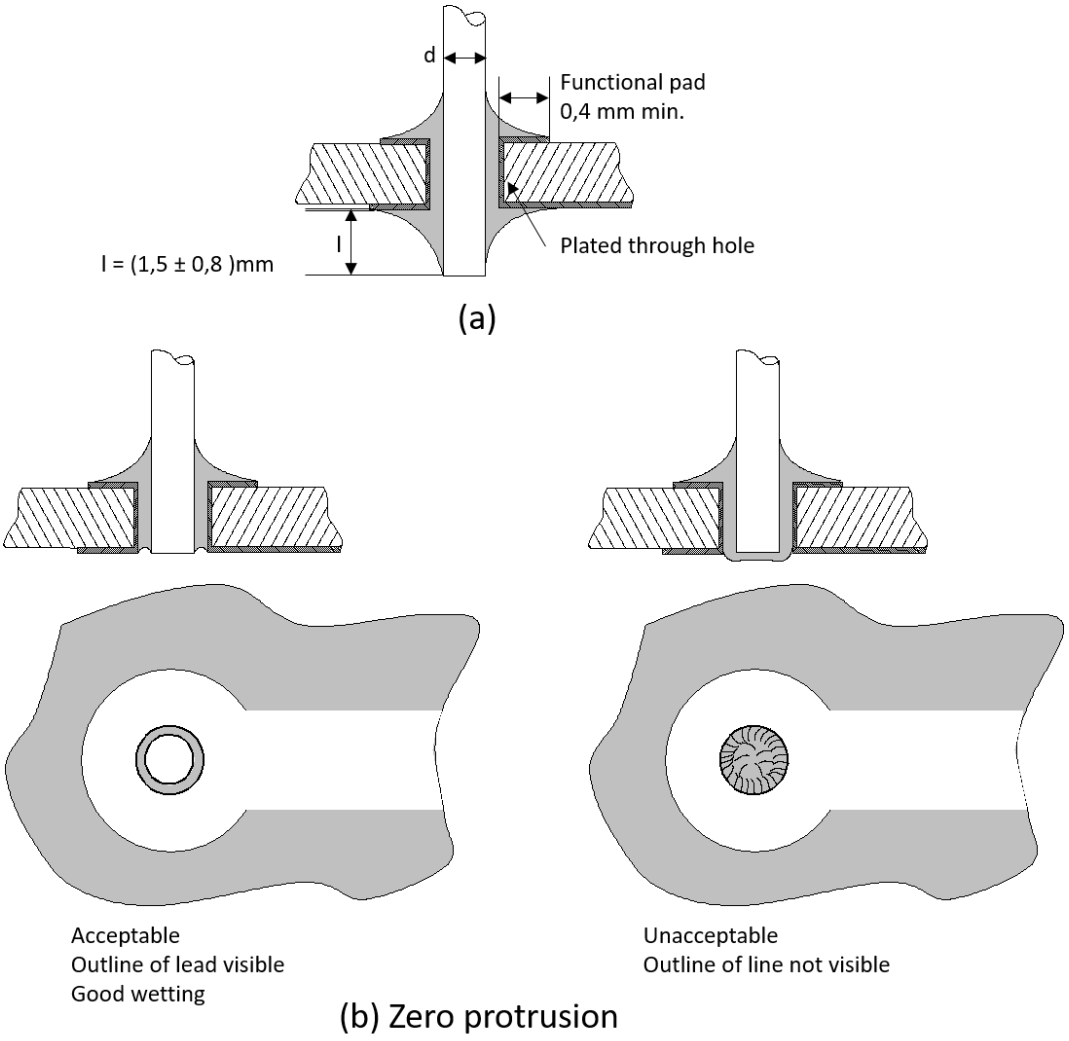
ECSS-Q-ST-70-61_1510346

a. For PCB thickness less than 2,2 mm, the leads shall protrude beyond the PCB surface by 1,5 mm ± 0,8 mm, as illustrated in Figure 8-6(a).

ECSS-Q-ST-70-61_1510347

b. For components with short leads and PCB thickness greater than or equal to 2,2 mm, the protrusion may be zero, provided that all the following conditions are met:

1. the outline of the lead is visible on the solder side,
2. there is wetting between the lead and the pad around the entire circumference on solder side according to Figure 8-6(b),
3. on the component side, the PCB pad shows solder flow-through and a solder fillet between the lead and the pad on the entire circumference of the lead.



ECSS-Q-ST-70-61_1510348

Figure 8-6: Stud leads

ECSS-Q-ST-70-61_1510349

c. For components with procured short leads soldered in plated through holes of thick PCBs negative protrusion shall not be acceptable, unless all the following conditions are met:

1. the negative lead protrusion does not exceed 10% of the PCB thickness measured between external laminates.
2. the leads are pretinned before soldering, for optimal wetting,
3. additional heating from the component side, by means of an extra soldering iron or other preheating system, is applied,
4. on the component side, the PCB pad shall show a solder flow-through and a solder fillet between the lead and the pad on the entire circumference of the lead.
5. X-ray inspection is carried out after soldering to check the maximum amount of voids is compliant with requirement 12.4a.

NOTE Examples of solder flow and voids with X-ray inspection are given in Figure F-1.

8.2.8.3 Clinching of components in non-plated through holes

ECSS-Q-ST-70-61_1510350

a. Non-bendable leads shall not be clinched.

ECSS-Q-ST-70-61_1510351

b. Clinching shall be performed in accordance with Figure 8-8 and Table 8-1.

ECSS-Q-ST-70-61_1510352

c. Components assembled in non-plated through holes by clinching shall be assembly verified in accordance with clause 13.

NOTE Assembly method is defined as SMT configuration with regards to verification.

NOTE It is good practice to stake or bond the component with adhesive

ECSS-Q-ST-70-61_1510353

d. For non-plated holes, TO-39 component clinched with stress relief as presented in Figure 8-8 may be mounted without assembly verification.

ECSS-Q-ST-70-61_1510354

e. The lead shall not be forced to lie flat during soldering

NOTE Component leads can spring-back when clinched.

ECSS-Q-ST-70-61_1510355

f. The lead shall not be in contact with the PCB at hole corner.

ECSS-Q-ST-70-61_1510356

g. The clinching shall be performed such that:

1. the lead extends through and overlap the solder pad,
2. the lead is bent to contact the solder pad
3. the lead is bent in the direction of the longest dimension of the solder pad, and
4. the area of the solder-pad permits a solder fillet to be formed.

ECSS-Q-ST-70-61_1510357

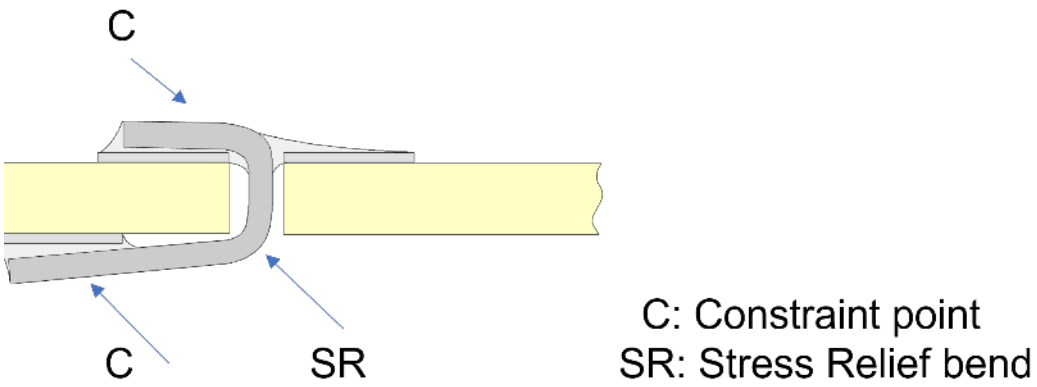
h. No portion of the soldered lead termination shall protrude beyond the pad.

ECSS-Q-ST-70-61_1510358

i. For lapped ribbon leads, one side of the lead may be flush with the edge of the solder pad

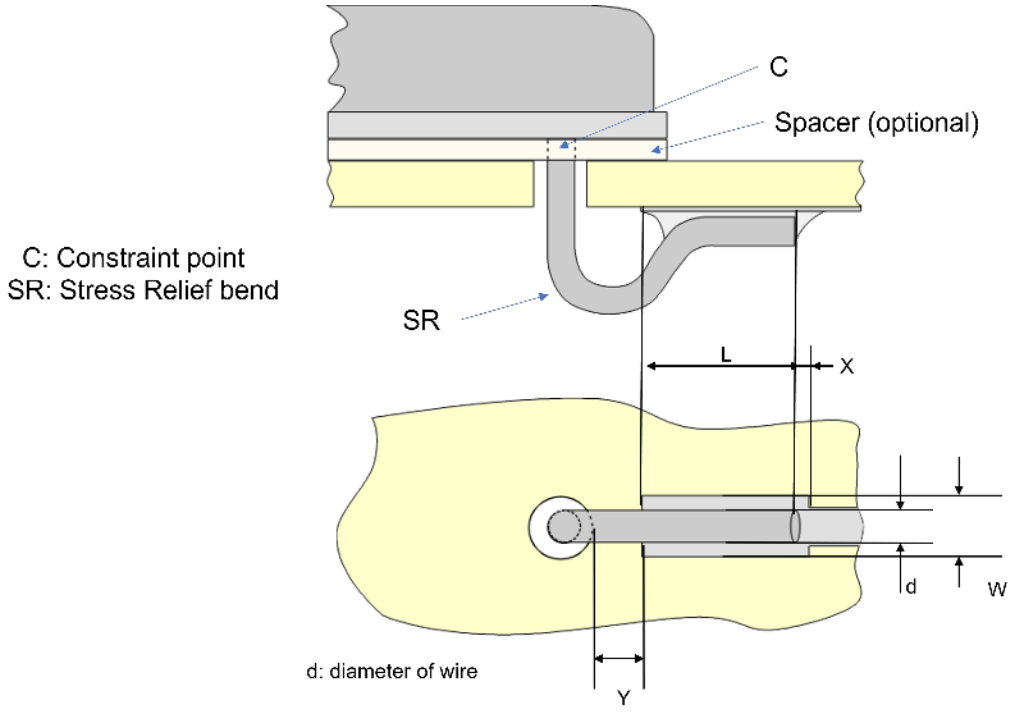
ECSS-Q-ST-70-61_1510359

j. For non-plated holes, wires used to connect opposite sides of a PCB shall be clinched with stress relief as presented in Figure 8-7.



ECSS-Q-ST-70-61_1510360

Figure 8-7: Wires used to connect opposite sides of a PCB



ECSS-Q-ST-70-61_1510361

Figure 8-8: Clinching with stress relief for component in non-plated hole

ECSS-Q-ST-70-61_1511127

Table 8-1: Dimensions and tolerances for clinching component in non-plated hole

Parameter	Dimension	Dimension limits
Lead diameter	d	
Lap connection	L	4d or 2 mm whichever is smaller
Minimum distance to footprint edge	X	0,5 d with 0,25 mm min
Minimum distance to hole edge	Y	3d
Pad width	W	1,5d min

8.2.9 Mounting of through hole connectors to PCBs

ECSS-Q-ST-70-61_1510362

a. PCB connectors shall be supplied with either:
   1. pre-formed leads supporting stress relief bends, or
   2. straight, resin moulded connector.

ECSS-Q-ST-70-61_1510363

b. Connectors shall be of a configuration incorporating either male or female quick-disconnect contacts and stress relief provision for the soldered

connection of each individual contact when such connections are completed

NOTE It is good practice to implement a stand-off between solder fillet and component body to insure stress relief.

ECSS-Q-ST-70-61_1510364

c. Connectors outside of what is covered by requirement 8.2.9a may be used providing successful assembly verification in accordance with clause 13.

ECSS-Q-ST-70-61_1510365

d. Degolding and pretinning of leads, in accordance with clause 7.6, shall be performed before mechanical fixing of connectors to the PCB.

ECSS-Q-ST-70-61_1510366

e. Before soldering, the operator shall verify that there will be no contact between the solder fillet to be formed and the gold plating.

ECSS-Q-ST-70-61_1510367

f. Connector leads shall protrude through the board in accordance with clause 8.2.8.2.

8.2.10 Mounting of swage terminals to PCBs

ECSS-Q-ST-70-61_1510368

a. The solder area shall be pretinned in compliance with clauses 7.6.2 or 7.6.3.

ECSS-Q-ST-70-61_1510369

b. Swage-type terminals, designed to have the terminal shoulder soldered to printed conductors, shall be secured to the external layer of a PCB by a roll swage in accordance with Figure 8-9(a).

ECSS-Q-ST-70-61_1510370

c. Swage-type terminals that are mounted in a plated-through hole shall be secured to the PCB by an elliptical funnel swage in accordance with Figure 8-9(b).

NOTE An elliptical funnel swage enables complete filling of the plated-through hole with solder.

ECSS-Q-ST-70-61_1510371

d. The PCB shall not be damaged by the swaging process.

ECSS-Q-ST-70-61_1510372

e. After swaging, the terminal shall be inspected for circumferential splits or cracks.

ECSS-Q-ST-70-61_1510373

f. After swaging, the terminal shall be free from circumferential splits or cracks.

ECSS-Q-ST-70-61_1510374

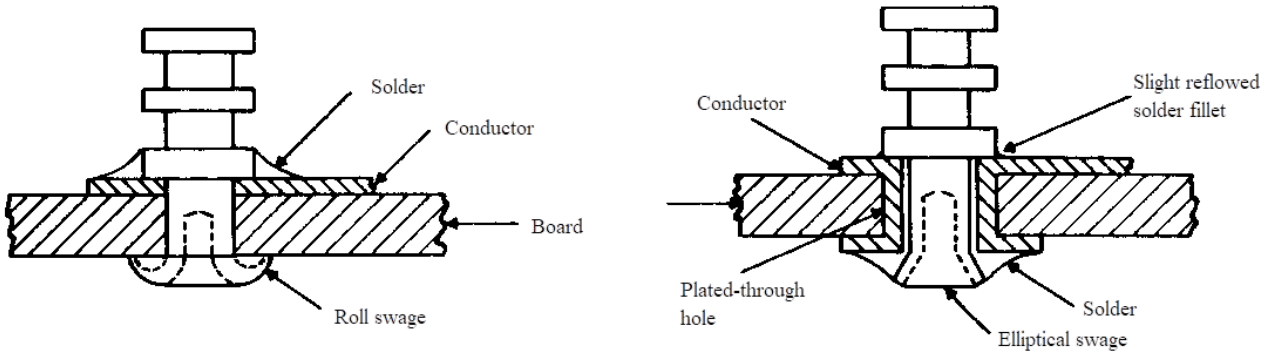
g. After swaging, the terminal may have a maximum of three radial splits or cracks, provided that the splits or cracks do not extend beyond the swaged area of the terminal and are a minimum of 90° apart.

ECSS-Q-ST-70-61_1510375

h. Terminals shall be soldered from swage side and solder flow such that a solder fillet is visible on the opposite side of the terminal.

ECSS-Q-ST-70-61_1510376

i. Terminals shall be soldered using Sn96 to avoid solder to melt whilst wire is soldered on the terminal.



ECSS-Q-ST-70-61_1510377

Figure 8-9: Types of terminal swaging

8.2.11 Mounting of components to terminals

ECSS-Q-ST-70-61_1510378

a. Degree of wrap, routing and connection to terminals shall be in accordance with clauses 9 and 10.

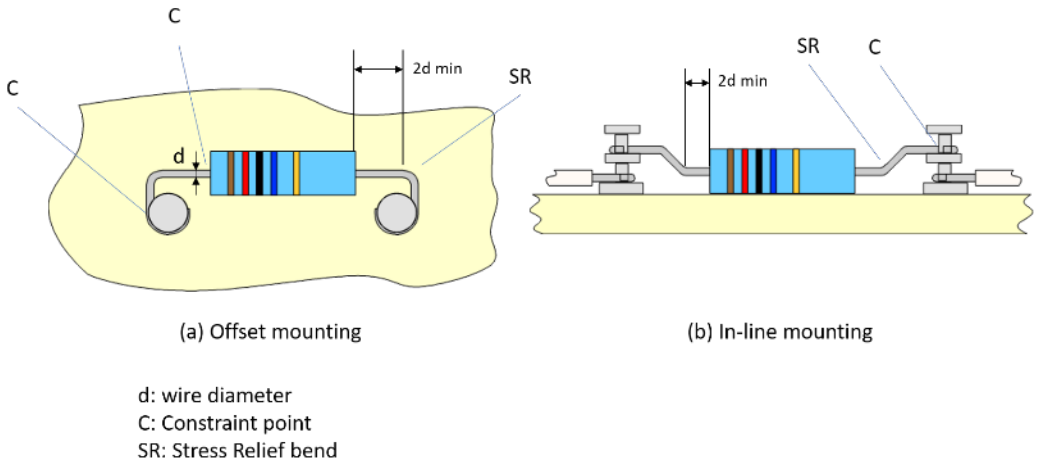
ECSS-Q-ST-70-61_1510379

b. The lead length between the component and the terminals shall be similar at both ends, except where component package shapes dictate offset positioning.

NOTE Example: Top hat diodes with flanges.

ECSS-Q-ST-70-61_1510380

c. Stress relief shall be provided in accordance with Figure 8-10.



ECSS-Q-ST-70-61_1510381

Figure 8-10: Method of stress relieving components attached to terminals

8.3 Mounting of surface mount components

8.3.1 General

ECSS-Q-ST-70-61_1510382

a. When CTE mismatch exists between components and substrate, the supplier shall take it into account with the mounting technology.

NOTE 1 Pure eutectic tin-lead solder or indium-lead solder provide better stress relief due to their ductility than those with additional elements, as antimony, gold.

NOTE 2 Leadless components with end-cap terminations, metallization, can have some stress relief (such as additional foil or wire leads, possibly attached by welding or soldered connection.

NOTE 3 A solder stand-off can assist stress relief. In this situation, the CTE mismatch strain is taken up by the ductile solder.

ECSS-Q-ST-70-61_1510383

b. Surface mounting of components shall be parallel to the board surface.

ECSS-Q-ST-70-61_1510384

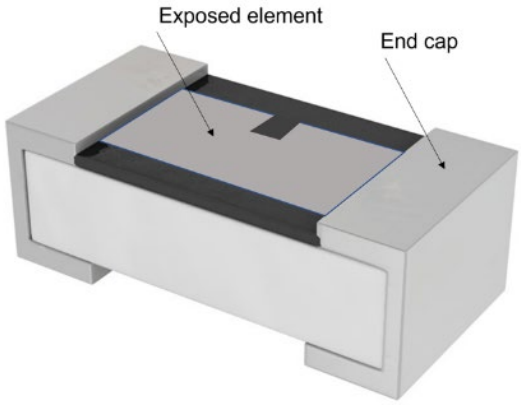
c. The active element of chip resistors, as illustrated in Figure 8-11, shall be mounted with that surface facing away from the printed circuit board or substrate.

ECSS-Q-ST-70-61_1510385

d. The active element of chip resistors, may be mounted with the active surface facing the printed circuit board or substrate for required electrical performance provided successful assembly verification according to clause 13.

ECSS-Q-ST-70-61_1510386

e. Ceramic chip capacitors may be mounted on the side providing the ratio width:height is less than 1,25:1.



ECSS-Q-ST-70-61_1510387

Figure 8-11: Exposed element

8.3.2 Lead forming

ECSS-Q-ST-70-61_1510388

a. The leads of leaded surface mount components shall be formed to their final configuration prior to mounting.

ECSS-Q-ST-70-61_1510389

b. Forming shall not degrade the solderability or cause cracks or loss of plating adhesion to the leads.

ECSS-Q-ST-70-61_1510390

c. Forming shall not cause mechanical damage to the leads or attachment seals.

ECSS-Q-ST-70-61_1510391

d. A maximum of 10 % of section reduction of the lead may be accepted provided that it is representative of the verified configuration and agreed by the Approval Authority.

ECSS-Q-ST-70-61_1510392

e. Leads of gull-wing packages, flat-packs and other multileaded components may be mechanically re-aligned with each other, provided

that the lead to package connection is not subjected to plastic deformation and agreed by Approval Authority.

NOTE Dedicated tool can be used to avoid any deformation in plastic area of the lead to package connection.

ECSS-Q-ST-70-61_1510393

f. Re-alignment of leads described in 8.3.1d shall be documented in PID.

ECSS-Q-ST-70-61_1510394

g. Lead forming shall be symmetrical.

ECSS-Q-ST-70-61_1510395

h. Formed leads shall not be re-bent.

8.3.3 Inspection of solder paste deposition

ECSS-Q-ST-70-61_1510396

a. The solder paste deposited on each solder footprint shall be inspected for registration and coverage prior to mounting the components.

ECSS-Q-ST-70-61_1510397

b. The inspection shall be performed on the whole surface of the PCB with a microscope or a magnifying tool with a magnification of 4x as a minimum.

ECSS-Q-ST-70-61_1510398

c. Inspection may be performed automatically providing proof of repeatability.

NOTE Solder Paste Inspection (SPI) is an example of automatic technic..

ECSS-Q-ST-70-61_1510399

d. The components shall be mounted in solder paste prior to reflow soldering.

9
Attachment of conductors to terminals, solder cups and cables

9.1 General

ECSS-Q-ST-70-61_1510400

a. A conductor shall be wrapped onto a terminal in the same direction as the final curvature of the wire.

ECSS-Q-ST-70-61_1510401

b. Gold-plated terminals and solder cups shall have the gold removed in the conductor attachment area and be pretinned in accordance with clause 7.6.2 and clause 7.6.3.3.

ECSS-Q-ST-70-61_1510402

c. The degolding and pretinning shall be such that the solder joint is not in contact with the gold.

ECSS-Q-ST-70-61_1510403

d. Conductors terminating at solder connections shall incorporate stress relief.

ECSS-Q-ST-70-61_1510404

e. Wicking shall be controlled.

NOTE 1 Anti-wicking tools can be used for pretinning the stranded wires.

NOTE 2 It is good practice to solder one wire per slot.

ECSS-Q-ST-70-61_1510405

f. Terminals and solder cup sizes shall be selected to match the size of conductors in accordance with the manufacturer's data sheet.

ECSS-Q-ST-70-61_1510406

g. The size of terminals or solder cups shall not be modified.

ECSS-Q-ST-70-61_1510407

h. Insulation clearance shall be in compliance with clause 9.2.2b.

NOTE The clearance distance denotes the shortest distance from wire insulation to terminal edge or solder joint whichever is the smallest."

9.2 Wire termination

9.2.1 Breakouts from cables

ECSS-Q-ST-70-61_1510408

a. The length of individual wires routed from a common cable to equally spaced terminals shall be uniform including wire ends and stress-relief bends.

NOTE Uniform lengths prevent stress concentration in any one wire.

9.2.2 Insulation clearance

ECSS-Q-ST-70-61_1510409

a. Where characteristic impedance or circuit parameters are not affected, the insulation clearance values stated in clause 7.5.4 shall apply.

ECSS-Q-ST-70-61_1510410

b. Where characteristic impedance or circuit parameters are affected, the insulation clearance requirements may be modified provided that sufficient insulation to surrounding conductive elements is kept.

ECSS-Q-ST-70-61_1510411

c. The modification implemented in requirement 9.2.2b shall be documented in the process procedures.

NOTE Example: High-voltage circuits or RF coaxial line terminations.

9.3 Turret and straight-pin terminals

ECSS-Q-ST-70-61_1510412

a. Side route connections shall be made as shown in Figure 9-1(a).

1. For side route connections, conductors shall be wrapped around the post as shown in Figure 9-1(b):Figure 9-1a minimum of 1/2 turn.
2. a maximum of 3/4 turn.

ECSS-Q-ST-70-61_1510413

b. For side route connections to turret terminals, all conductors shall be confined to the guide slots.

ECSS-Q-ST-70-61_1510414

c. For side route connections, conductors shall not project beyond the base of the terminal.

ECSS-Q-ST-70-61_1510415

d. Wires shall not be wrapped over other wires.

ECSS-Q-ST-70-61_1510416

e. More than one wire may be installed in a single slot of a terminal post provided that

1. the combined diameters of the wires are less than the height of the slot, and
2. the contour of each wire is visible.

NOTE it is good practice to solder one wire per slot

ECSS-Q-ST-70-61_1510417

f. Wires terminating at terminals that do not have a mechanical shoulder or turret shall not be attached closer than one conductor diameter to the top of the terminal.

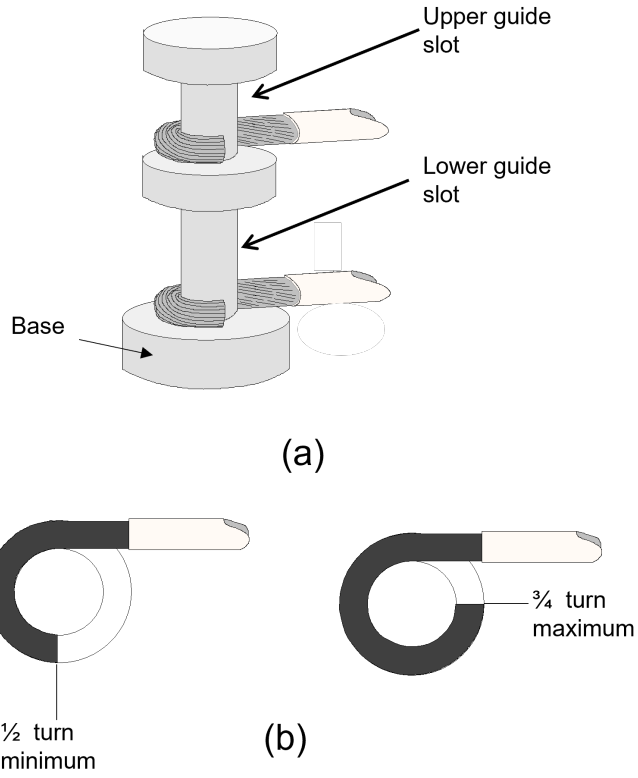
ECSS-Q-ST-70-61_1510418

g. Insulation clearance shall be in compliance with clause 9.2.2.

NOTE The clearance distance denotes the shortest distance from wire insulation to terminal edge or solder joint whichever is the smallest.”

ECSS-Q-ST-70-61_1510419

h. The solder joints to turret terminals shall meet the solder fillet requirements as illustrated in Figure E-2 and Figure E-3 according to twin or single conductor configuration.



ECSS-Q-ST-70-61_1510420

Figure 9-1: Side route connections to turret terminals

9.4 Bifurcated terminals

9.4.1 General

ECSS-Q-ST-70-61_1510421

a. Top, side or bottom routes, or combinations thereof, shall be used.

ECSS-Q-ST-70-61_1510422

b. Top route and side route shall not be used together on the same terminal.

9.4.2 Bottom route

ECSS-Q-ST-70-61_1510423

a. Bottom route connections shall be as shown in Figure 9-2(b) and (c).

ECSS-Q-ST-70-61_1510424

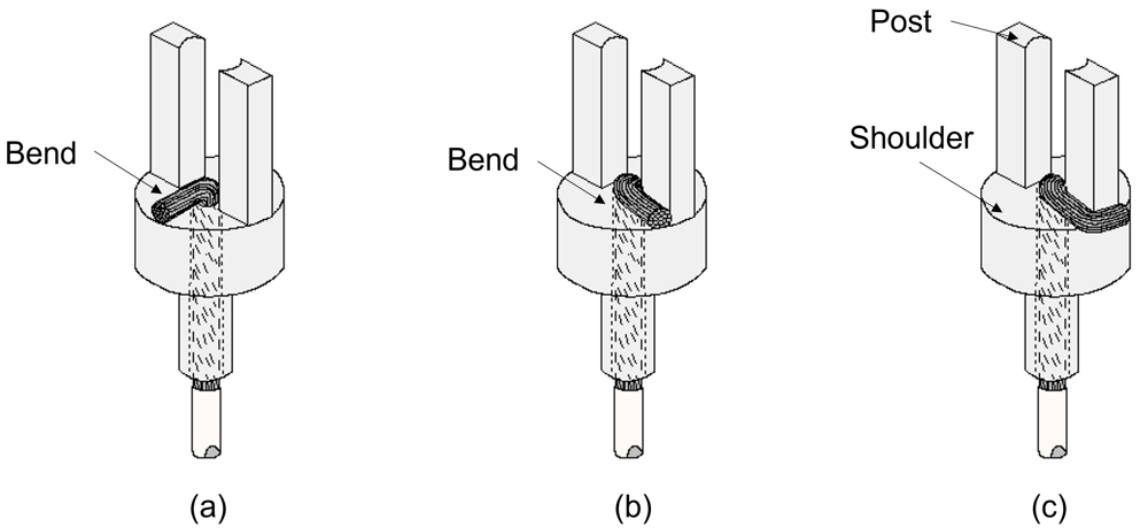
b. The conductor shall enter the terminal from the bottom, pass through the side slot at the top, and be wrapped as for the side route, as shown in Figure 9-1(b).

ECSS-Q-ST-70-61_1510425

c. Conductors may project beyond the diameter of the base, see Figure 9-2(c), provided that clearances, environmental and electrical characteristics are not compromised.

ECSS-Q-ST-70-61_1510426

d. The solder joints to bifurcated terminals shall meet the solder fillet requirements as illustrated in Figure E-4.



ECSS-Q-ST-70-61_1510427

Figure 9-2: Bottom route connections to bifurcated terminal

9.4.3 Side route

ECSS-Q-ST-70-61_1510428

a. Side route connections shall be as shown in Figure 9-3.

ECSS-Q-ST-70-61_1510429

b. The conductor shall enter the mounting slot perpendicular to the posts.

ECSS-Q-ST-70-61_1510430

c. When more than one conductor is connected to a terminal, the direction of bend of each additional conductor shall alternate, see Figure 9-3(b) and (d) with the contour of each wire visible.

ECSS-Q-ST-70-61_1510431

d. Side-route connections shall not project above the top of the terminal.

ECSS-Q-ST-70-61_1510432

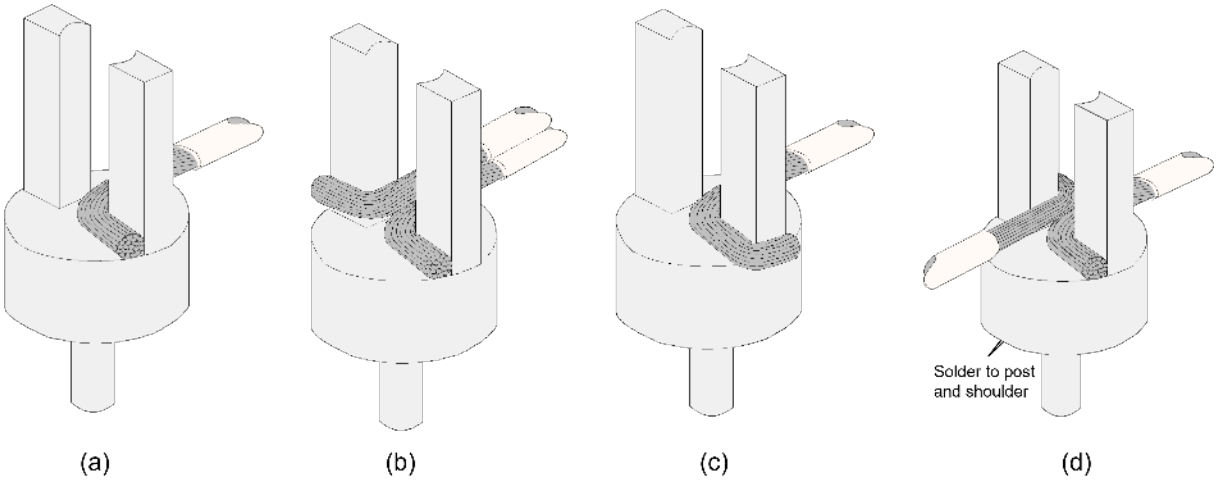
e. Conductors may project beyond the diameter of the base, see Figure 9-3(c), provided that clearances, environmental and electrical characteristics are not compromised.

ECSS-Q-ST-70-61_1510433

f. Conductors shall be wrapped a minimum of ¼ turn, as shown in Figure 9-3(a), to a maximum of ½ turn, as shown in Figure 9-3(c) around the post.

ECSS-Q-ST-70-61_1510434

g. The solder joints to bifurcated terminals shall meet the solder fillet requirements as illustrated in Figure E-4.



ECSS-Q-ST-70-61_1511128

Figure 9-3: Side-route connection to bifurcated terminal

9.4.4 Top route

ECSS-Q-ST-70-61_1510435

a. The top route shall not be used where side entry is possible.

ECSS-Q-ST-70-61_1510436

b. Top route connections shall be as shown in Figure 9-4.

ECSS-Q-ST-70-61_1510437

c. Conductors shall be inserted between the vertical posts to the depth of the shoulder, except for combined top and bottom routes as per clause 9.4.5.

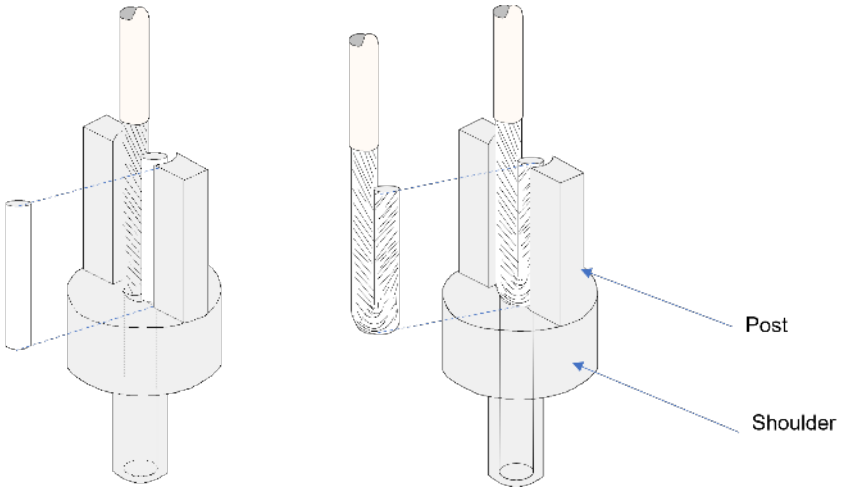
ECSS-Q-ST-70-61_1510438

d. Conductors which do not fill the gap, as shown in Figure 9-4, shall be either:

1. accompanied by a tinned filler solid or stranded wire, such that the combined diameters fill the gap, or
2. bent double, provided that the combined diameters fill the gap.

ECSS-Q-ST-70-61_1510439

e. The solder joints to bifurcated terminals shall meet the solder fillet requirements as illustrated in Figure E-4.



ECSS-Q-ST-70-61_1510440

Figure 9-4: Top route connection to bifurcated terminal

9.4.5 Combination of top and bottom routes

ECSS-Q-ST-70-61_1510441

a. The bottom route conductor shall be installed before the top route conductor.

ECSS-Q-ST-70-61_1510442

b. The top route conductor shall be inserted to contact the bottom route conductor.

9.4.6 Combination of side and bottom routes

ECSS-Q-ST-70-61_1510443

a. The bottom route conductor shall be installed before the side route conductor.

9.5 Hook terminals

ECSS-Q-ST-70-61_1510444

a. Connections to hook terminals shall be as shown in Figure 9-5.

ECSS-Q-ST-70-61_1510445

b. The bend to attach conductors to hook terminals shall be:

1. a minimum of 1/2 turn,
2. a maximum of 3/4 turn.

ECSS-Q-ST-70-61_1510446

c. Protrusion of conductor ends shall not damage insulation sleeving.

ECSS-Q-ST-70-61_1510447

d. Where more than one conductor is attached to a terminal, the direction of bend of each conductor shall alternate as shown in Figure 9-5(b).

ECSS-Q-ST-70-61_1510448

e. When more than one conductor is attached to terminal, the conductors shall be at different angles to allow formation of separate solder joints as shown in Figure 9-5(b).

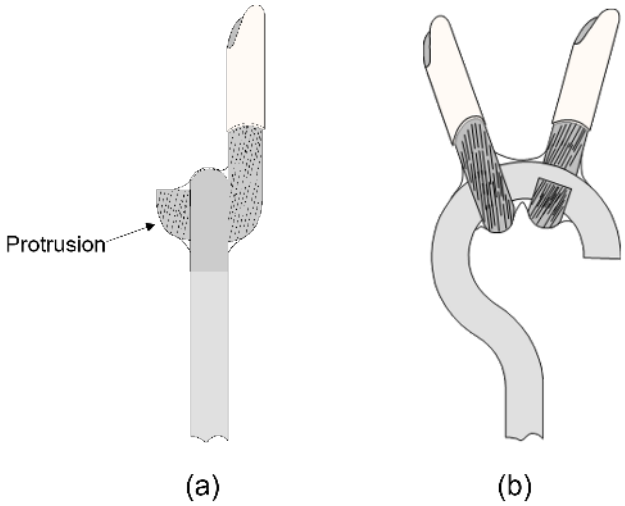
ECSS-Q-ST-70-61_1510449

f. Insulation clearance shall be in compliance with clause 9.2.2.

NOTE The clearance distance denotes the shortest distance from wire insulation to terminal edge or solder joint whichever is the smallest."

ECSS-Q-ST-70-61_1510450

g. The solder joints to hook terminals shall meet the solder fillet requirements as illustrated in Figure E-5.



ECSS-Q-ST-70-61_1510451

Figure 9-5: Connections to hook terminals

9.6 Pierced terminals

ECSS-Q-ST-70-61_1510452

a. Connections to pierced terminals shall be as shown in Figure 9-6.

ECSS-Q-ST-70-61_1510453

b. The bend to attach conductors to pierced terminals shall be:

1. a minimum of 1/4 turn,
2. a maximum of 3/4 turn.

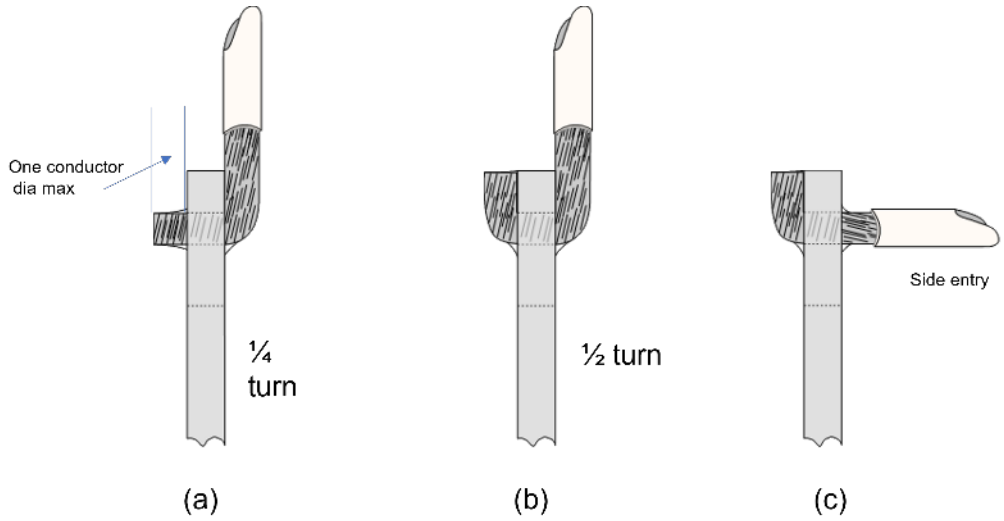
ECSS-Q-ST-70-61_1510454

c. Protrusion of conductor ends shall not damage insulation sleeving.

ECSS-Q-ST-70-61_1510455

d. Insulation clearance shall be in compliance with clause 9.2.2.

NOTE The clearance distance denotes the shortest distance from wire insulation to terminal edge or solder joint whichever is the smallest."



ECSS-Q-ST-70-61_1510456

Figure 9-6: Connections to pierced terminals

9.7 Solder cups for connector

ECSS-Q-ST-70-61_1510457

a. Conductors shall enter the solder cup as shown in Figure 9-7.

ECSS-Q-ST-70-61_1510458

b. Conductors shall be bottomed in the cup.

ECSS-Q-ST-70-61_1510459

c. Conductors shall be in contact with the inner wall of the cup.

ECSS-Q-ST-70-61_1510460

d. Multiple conductors may be inserted provided that each is in contact with the full height of the inner wall of the cup with contour of each wire visible.

ECSS-Q-ST-70-61_1510461

e. Flux shall not be trapped within the solder cup.

ECSS-Q-ST-70-61_1510462

f. Conductors shall be centred in the terminal and parallel within the contact.

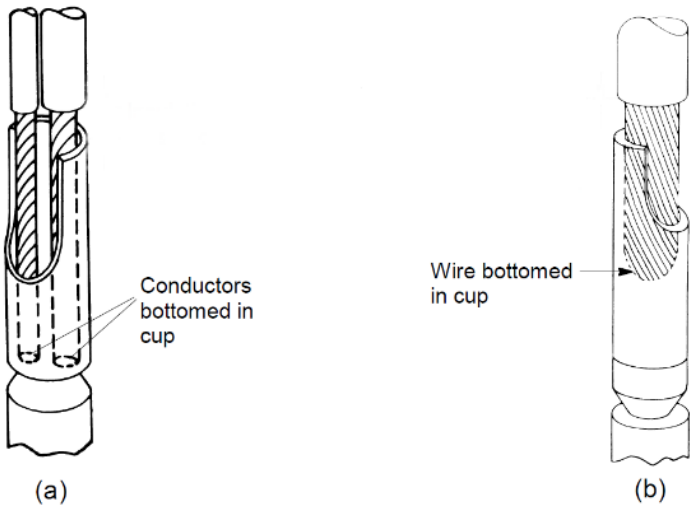
ECSS-Q-ST-70-61_1510463

g. The solder joints to cup terminals shall meet the solder fillet requirements as illustrated in Figure E-6.

ECSS-Q-ST-70-61_1510464

h. Insulation clearance shall be in compliance with clause 9.2.2.

NOTE The clearance distance denotes the shortest distance from wire insulation to terminal edge or solder joint whichever is the smallest."



ECSS-Q-ST-70-61_1510465

Figure 9-7: Connections to solder cups (connector type)

9.8 Insulation sleeving

ECSS-Q-ST-70-61_1510466

a. Electrical connections shall be insulated.

NOTE For example with coating, potting, insulation grommets or insulating sleeving.

ECSS-Q-ST-70-61_1510467

b. Heat-shrinkable sleeving shall provide electrical insulation and mechanical support to the finished interconnection.

ECSS-Q-ST-70-61_1510468

c. Interconnection methods shall not use fluxed solder preforms within heat-shrinkable sleeves.

ECSS-Q-ST-70-61_1510469

d. Fluorocarbon sleeves shall not be used.

NOTE Fluorocarbon sleeves have high shrinkage temperatures that can damage or reflow soldered connections.

ECSS-Q-ST-70-61_1510470

e. Insulation sleeving shall be transparent and heat shrinkable.

ECSS-Q-ST-70-61_1510471

f. If insulation sleeving is not transparent, inspection of the solder joint shall be done before shrinking the sleeve in place.

ECSS-Q-ST-70-61_1510472

g. A component shall not move within the sleeving when the sleeving is mechanically supported.

ECSS-Q-ST-70-61_1510473

h. The heat-shrinkable insulation sleeving shall be centred over the cleaned and inspected interconnection.

ECSS-Q-ST-70-61_1510474

i. The sleeving shall be cut to a length that covers the finished soldered joint and extends over the remaining insulation of each conductor for a distance of 5 mm ±2 mm.

ECSS-Q-ST-70-61_1510475

j. The minimum overlap between the sleeving and the wire may be shorter than 5 mm ±2 mm. providing minimum overlap is two times the outer wire diameter.

ECSS-Q-ST-70-61_1510476

k. The cut sleeving shall be placed over one of the wires to be joined prior the soldered connection made.

ECSS-Q-ST-70-61_1510477

l. The sleeving shall be shrunk using heated gas or radiant energy.

ECSS-Q-ST-70-61_1510478

m. Heat shrinking of the sleeving shall not damage the assembly.

ECSS-Q-ST-70-61_1510479

n. Heat shall not be applied for more than 8 seconds.

ECSS-Q-ST-70-61_1510480

o. The heat shrinking temperature shall not exceed the maximum temperature recommended by the manufacturer.

ECSS-Q-ST-70-61_1510481

p. The heat-shrinking temperature shall not exceed 140 °C at solder joint location.

ECSS-Q-ST-70-61_1510482

q. The minimum distance between hot air blower and shrink sleeving shall be documented by the manufacturer to comply with requirement 9.8o and 9.8p.

ECSS-Q-ST-70-61_1510483

r. PTFE materials shall not be heated above 250 °C.

NOTE Poisonous gases can be liberated above this temperature.

ECSS-Q-ST-70-61_1510484

s. Flux entrapment within the sleeve shall not be accepted.

NOTE Flux residues can be detected by visual inspection.

9.9 Wire and cable interconnections

9.9.1 General

ECSS-Q-ST-70-61_1510485

a. Soldered wire interconnection methods shall enable the removal of flux and flux residue.

ECSS-Q-ST-70-61_1510486

b. Soldered wire interconnection methods shall enable visual inspection of the interconnection and surrounding materials.

ECSS-Q-ST-70-61_1510487

c. After soldering, conductors shall be covered with heat-shrinkable sleeving in compliance with clause 9.8.

ECSS-Q-ST-70-61_1510488

d. Enamelled wires with polyimide insulation which have shown susceptibility to cracks shall be heated prior to cleaning to release residual stresses after forming to prevent cracking when cleaning in solvents.

NOTE 1 It is good practice to use a temperature of 125°C for a duration of 2,5 hours.

NOTE 2 When used in magnetics parts, tempering can be part of screening process at component level.

9.9.2 Preparation of wires

ECSS-Q-ST-70-61_1510489

a. Wire insulation shall be removed using insulation strippers in accordance with clause 5.5.6.

ECSS-Q-ST-70-61_1510490

b. Wire insulation clearances shall be in accordance with clause 7.5.4.

ECSS-Q-ST-70-61_1510491

c. Pretinning shall be in accordance with clause 7.6.4.

9.9.3 Preparation of shielded wires and cables

ECSS-Q-ST-70-61_1510492

a. The area of exposed shield shall be either:
   1. at the end termination of the wire or cable, or
   2. at any position along the length of a wire or centre splice cable.

ECSS-Q-ST-70-61_1510493

b. The insulation jacket as illustrated in Figure 9-8 (a) shall be removed for:
   1. a minimum length of 5 mm,
   2. a maximum length of 12 mm.

ECSS-Q-ST-70-61_1510494

c. The insulation jacket shall be scored and removed using a sharp cutting tool.

   NOTE Example: a scalpel.

ECSS-Q-ST-70-61_1510495

d. The preparation process shall not damage the exposed shield material in accordance with clauses 7.5.1 and 7.5.2.

ECSS-Q-ST-70-61_1510496

e. The shield material shall be of good wettability.

ECSS-Q-ST-70-61_1510497

f. The shield material shall not be pretinned.

ECSS-Q-ST-70-61_1510498

g. The shield material shall be cleaned using a solvent in accordance with clause 6.4

9.9.4 Pre-assembly of wires

ECSS-Q-ST-70-61_1510499

a. Conductors shall be secured to prevent disturbance during soldering and solidification using one, or a combination of, the following methods:
   1. A holding fixture that clamps the wires ensuring correct alignment.
   2. Rings of heat-shrinkable sleeving positioned over the ends of the wire insulations, see Figure 9-8(b) and (c).

ECSS-Q-ST-70-61_1510500

b. The conductors to be joined shall lie parallel and in contact.

ECSS-Q-ST-70-61_1510501

c. A concave fillet of solder shall be present between the terminal and the sides of the conductor.

ECSS-Q-ST-70-61_1510502

d. The contour of the conductor shall be visible after soldering.

ECSS-Q-ST-70-61_1510503

e. Terminals with more than one wire shall have each wire in contact with and soldered to the terminal.

ECSS-Q-ST-70-61_1510504

f. Conductors may be preformed when the cable insulation prevents a parallel lay.

ECSS-Q-ST-70-61_1510505

g. The bending radius of the wire shall be as a minimum 2 times the diameter of the wire except for polyimide insulated wire for which the minimum bending radius is 10 times the diameter.

ECSS-Q-ST-70-61_1510506

h. Bending tools for the preforming of conductors shall be in accordance with clause 5.5.4.

ECSS-Q-ST-70-61_1510507

i. Wires shall be spliced using lap joints.

ECSS-Q-ST-70-61_1510508

j. For shield terminations, the conductor of the grounding wire shall be positioned on the exposed shield.

ECSS-Q-ST-70-61_1510509

k. Insulation overlap shall not be greater than the diameter of the largest conductor of the interconnection as illustrated in Figure E-9.

ECSS-Q-ST-70-61_1510510

l. The solder joints to shielded cables shall meet the solder fillet requirements as illustrated in Figure E-8.

ECSS-Q-ST-70-61_1510511

m. The solder joints to shielded wires shall meet the solder fillet requirements as illustrated in Figure E-9 and Figure E-10.

ECSS-Q-ST-70-61_1510512

n. The solder joint shall have a mechanical aid such as:

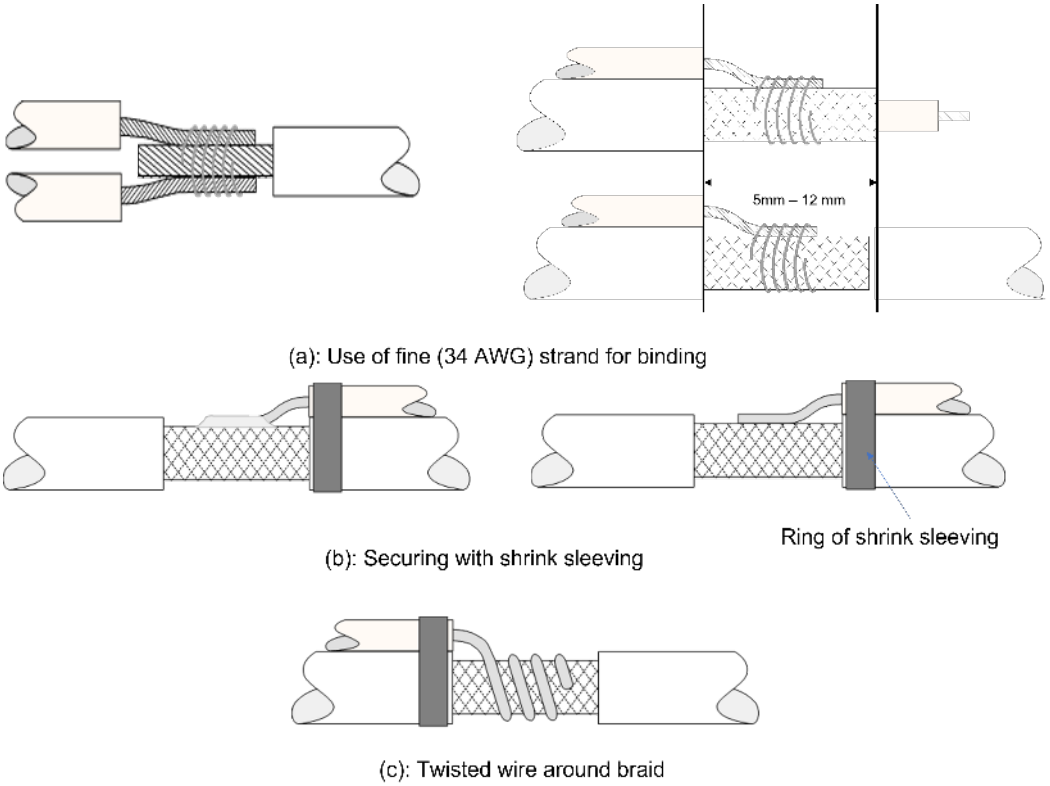
1. A strand of binding wire, wrapped a minimum of 5 turns, as shown in Figure 9-8(a) or
2. A twist-splice around the braid, see Figure 9-8(c) or
3. A shrinkable sleeve that maintain the two connections to be made.

ECSS-Q-ST-70-61_1510513

o. The minimum solder connection shall be 5 to 8 mm when no binding wire is used

ECSS-Q-ST-70-61_1510514

p. The minimum solder connection shall be 2 mm when binding wire is used.



ECSS-Q-ST-70-61_1510515

Figure 9-8: Methods for securing wires

9.10 Connection of wires to PCBs

ECSS-Q-ST-70-61_1510516

a. Wires shall be soldered to PCB terminations using lap joints or plated-through holes in accordance with Figure 9-9 and Table 9-1.

ECSS-Q-ST-70-61_1510517

b. Stress relief shall be provided.

ECSS-Q-ST-70-61_1510518

c. For PTFE-insulated wire, the minimum distance between the insulation and the solder fillet shall be minimum 1 mm.

ECSS-Q-ST-70-61_1510519

d. The soldered lap connection length L shall be minimum 4d or 2 mm whichever is the smaller as defined in Table 9-1.

ECSS-Q-ST-70-61_1510520

e. Wires shall be supported at maximum 30 mm from stress relief present after the solder joint location and then at intervals not exceeding 50 mm.

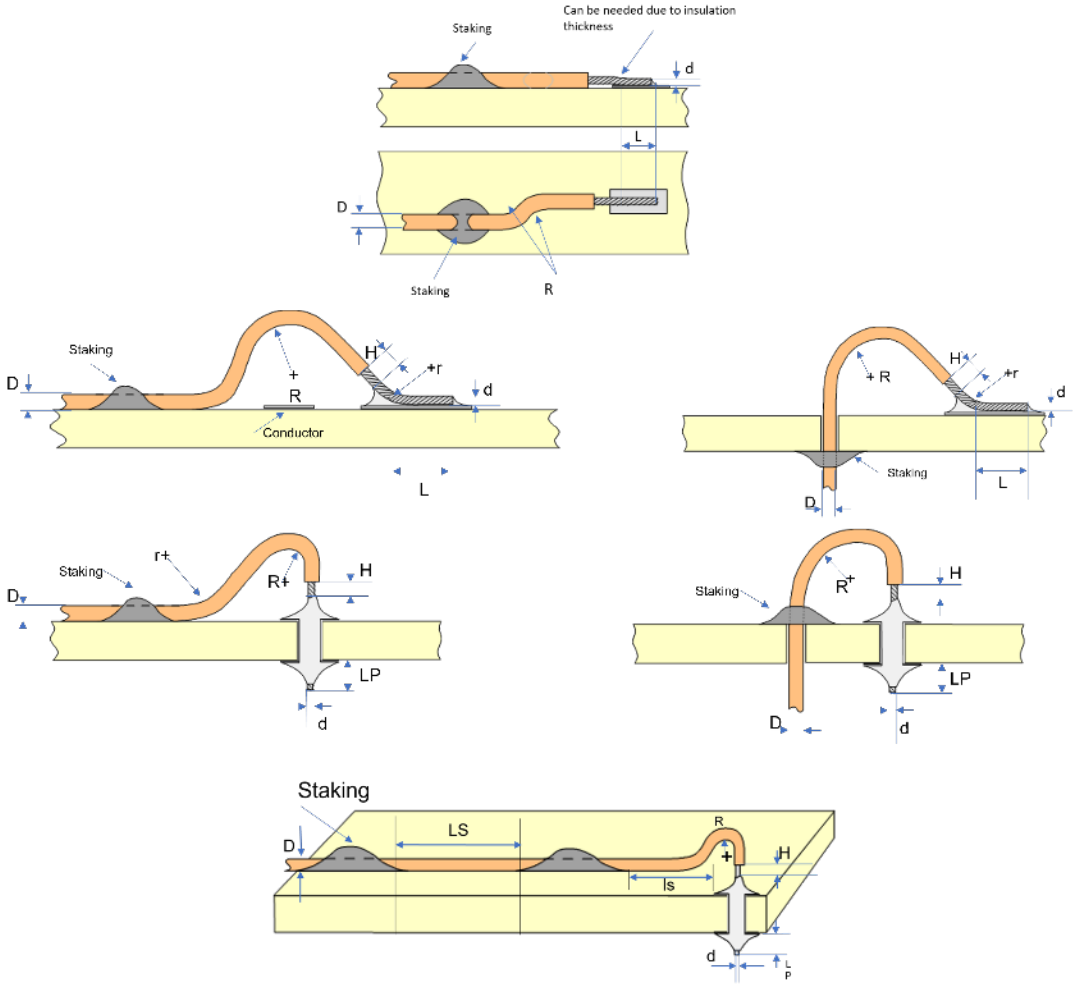
ECSS-Q-ST-70-61_1510521

f. Wire support shall be provided by staking, conformal coating or lacing.

ECSS-Q-ST-70-61_1510522

g. The wire shall be embedded in the conformal coating.

NOTE As long as the conformal coating is covering a wire, the staking or lacing is not necessary.



ECSS-Q-ST-70-61_1510523

Figure 9-9: Connection of solid or stranded wires to PCBs

ECSS-Q-ST-70-61_1510524

Table 9-1: Dimensions for connections of solid or stranded wires to PCBs

Parameter	Dimension	Dimension limits
Wire bend radius	r	≥ 2 d
Conductor bend radius	R	≥ 2 D general case ≥ 10 D for polyimide wire
Insulation clearance	H	1 mm min and according to req. 7.5.4a
Soldered lap connection length	L	4d or 2 mm whichever is the smaller
Lead protrusion through board	LP	1,5 mm ± 0,8 mm
Distance between first staking point and soldered connection to PCB	ls	≤30 mm
Distance between supporting points	LS	≤50 mm
Conductor diameter	d	min AWG 33 for solid wire min AWG 30 for stranded wire
Outer wire diameter	D	

9.11 Connection of coaxial cables to PCBs

ECSS-Q-ST-70-61_1510525

a. Coaxial cables shall be soldered to PCB terminations using plated-through holes or surface mount pads, in accordance with Figure 9-10 and Table 9-2.

ECSS-Q-ST-70-61_1510526

b. Stress relief shall be provided.

ECSS-Q-ST-70-61_1510527

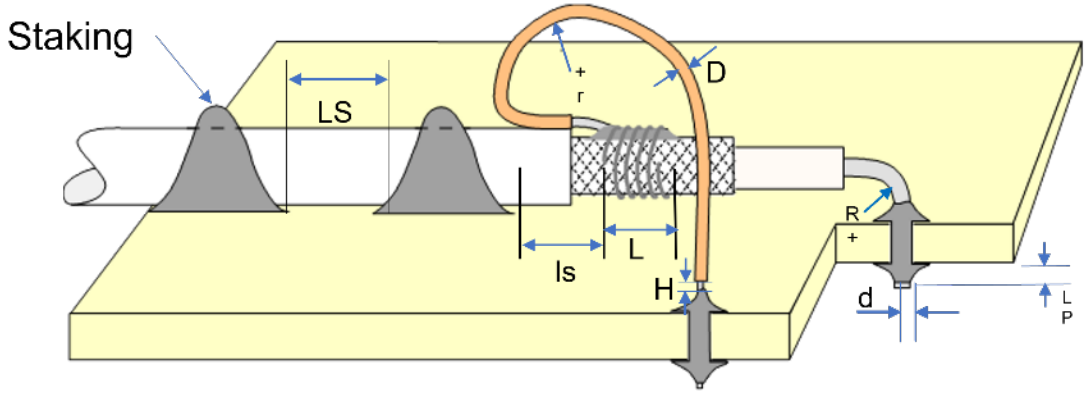
c. Coaxial cables shall be supported at maximum 30 mm from the solder and then at intervals not exceeding 50 mm.

ECSS-Q-ST-70-61_1510528

d. Coaxial cables support shall be provided by staking.

ECSS-Q-ST-70-61_1510529

e. Solder of wire over the shielding shall be made without additional flux



ECSS-Q-ST-70-61_1510530

Figure 9-10: Connection of coaxial cables to PCBs

ECSS-Q-ST-70-61_1510531

Table 9-2: Dimensions for connections of coaxial cables to PCBs

Parameter	Dimension	Dimension limits
Wire bend radius	r	≥ 5 d
Conductor bend radius	R	≥ 5 D
Insulation clearance	H	1 mm minimum and according to requirement 7.5.4a
Soldered connection length for wire to shielding braid	L	2 mm minimum with 5 turns of binding wire
Lead protrusion through board	LP	1,5 mm ± 0,8 mm
Distance between first staking point and soldered connection to PCB	ls	≤30 mm
Distance between supporting points	LS	≤50 mm
Inner cable conductor diameter	d	
Shielding wire diameter	D	min AWG 33 for solid wire min AWG 30 for stranded wire

10
Assembly to terminals and to PCBs

10.1 Overview

Assembly consists of soldering and solderless technologies.

Soldering technologies are characterized by components or wires that are soldered onto terminals or the PCB with a solder alloy using a soldering process for example solder iron, wave or reflow soldering.

Pressfit connectors are not covered by this standard.

Some components can be assembled without using a soldering process - solderless technology.

Both technologies can co-exist on the same board. In this case, solderless process is the last assembly operation.

10.2 General soldering conditions

10.2.1 General

ECSS-Q-ST-70-61_1510532

a. Solders and fluxes shall be selected in accordance with respectively clause 6.2 and clause 6.3

ECSS-Q-ST-70-61_1510533

b. Anti-wicking tool in accordance with clause 5.5.8.4 shall be used to restrict wicking of flux or solder under the wire insulation.

ECSS-Q-ST-70-61_1510534

c. Different solder joints on same component shall be homogenous in volume.

NOTE Figure 10-4 to Figure 10-16 show minimum and maximum height values on the same component drawing for illustration purpose.

ECSS-Q-ST-70-61_1510535

d. During soldering of leadless components with soldering iron, the soldering tip shall not be in contact with the termination.

ECSS-Q-ST-70-61_1510536

e. The solder fillet shall not be in contact with any remaining gold-plated area on the termination.

ECSS-Q-ST-70-61_1510537

f. Soldering to gold with tin/lead alloys shall not be performed except the cases specified in the requirements, 6.9.2b.

ECSS-Q-ST-70-61_1510538

g. Configurations not compliant with clause 8.2 may be accepted provided successful verification according to clause 13 and acceptance from the Approval Authority

ECSS-Q-ST-70-61_1510539

h. All configurations from clause 10.4, clause 10.6 and clause 10.7 shall be demonstrated by verification in compliance with requirements from clause 13.

ECSS-Q-ST-70-61_1510540

i. Configurations not compliant with clause 10.4, clause 10.6 or clause 10.7 may be accepted provided successful verification according to clause 13 and acceptance from the Approval Authority.

ECSS-Q-ST-70-61_1510541

j. The shape and fillet height of the solder joint on the flight hardware shall be representative of what has been verified.

ECSS-Q-ST-70-61_1510542

k. The solder fillet criteria shall be identified in the workmanship document of the company and listed in the PID.

ECSS-Q-ST-70-61_1510543

l. Verified acceptance criteria shall be documented and used as pass/fail criteria for FM.

10.2.2 Positioning

ECSS-Q-ST-70-61_1510544

a. There shall be no relative motion between conductors and terminals during soldering or solder solidification.

ECSS-Q-ST-70-61_1510545

b. Conductors shall not be temporarily constrained against spring-back force during solder solidification, to prevent residual stresses in the solder joints, leads and terminals.

NOTE Residual stresses are produced in the lead material or solder joint.

ECSS-Q-ST-70-61_1510546

c. Components shall not be mounted on flexible substrates.

NOTE See definition of flexible PCB in ECSS-Q-ST-70-60.

ECSS-Q-ST-70-61_1510547

d. Components shall not be stacked nor bridge the space between other components or terminals.

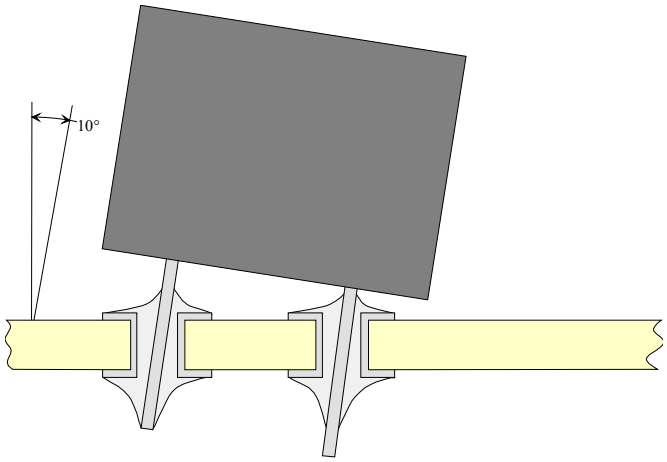
ECSS-Q-ST-70-61_1510548

e. Positioning of components shall not reduce the specified minimum electrical clearance to adjacent tracks or other metallized elements in conformance with clause 14.3.2 of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-61_1510549

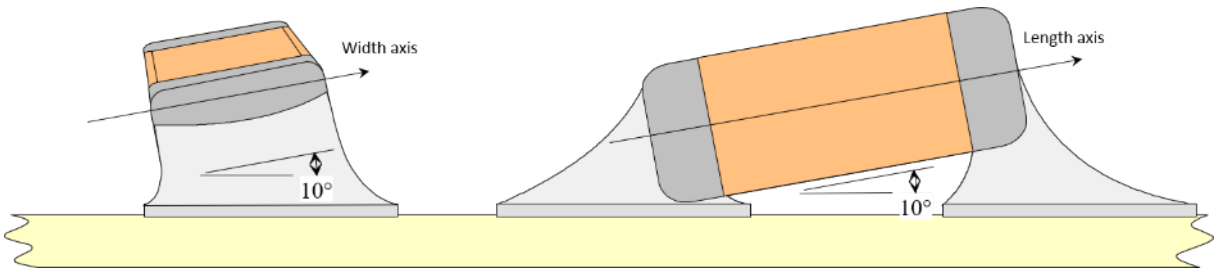
f. Maximum tilt limit shall not exceed 10° as shown in Figure 10-1 and Figure 10-2 except in the case defined in requirement 10.2.2g.

NOTE Tilt is the angle between the PCB plane and the component axis both along length and width.



ECSS-Q-ST-70-61_1510550

Figure 10-1: Maximum tilt for assembled PTH component



ECSS-Q-ST-70-61_1510551

Figure 10-2: Maximum tilt for assembled SMD component

ECSS-Q-ST-70-61_1510552

g. For assembly sensitive components, the maximum tilt shall be defined based on the assembly verification results and not exceed 10°

ECSS-Q-ST-70-61_1510553

h. All leaded components shall be mounted with all leads soldered on a terminal area to provide mechanical strength.

ECSS-Q-ST-70-61_1510554

i. The component positioning shall be such that visual inspection can be undertaken.

ECSS-Q-ST-70-61_1510555

j. If visual inspection of a fully populated assembly is not possible, the assembly and inspection shall be made in steps enabling visual inspection.

10.2.3 Application of flux

ECSS-Q-ST-70-61_1510556

a. External flux shall be used for soldering with the exception of some cases such as soldering on a shielding, pointing of leads of bonded components, assembly of some detectors if cleaning is not possible.

ECSS-Q-ST-70-61_1510557

b. The quantity of flux used shall be such that the solder joint is in accordance with clause 12.

ECSS-Q-ST-70-61_1510558

c. When flux-cored solder is used, it shall be positioned such that the flux flows and covers the components to be joined as the solder melts.

ECSS-Q-ST-70-61_1510559

d. When an external liquid flux is used in conjunction with flux-cored solders, the fluxes shall be compatible.

ECSS-Q-ST-70-61_1510560

e. When external flux is used, liquid flux shall be applied to the surfaces to be joined prior to the application of heat.

10.2.4 Flux controls for wave-soldering equipment

ECSS-Q-ST-70-61_1510561

a. A controlled method shall be established and implemented for wave-soldering machines such that the flux is not contaminated with remaining residues from previous works.

ECSS-Q-ST-70-61_1510562

b. All fluxes properties shall be controlled, and results recorded prior to soldering.

NOTE For example, specific gravity.

ECSS-Q-ST-70-61_1510563

c. Dross (oxides) from the solder bath shall be removed so that dross does not mix with the liquid solder.

NOTE Automatic or manual processes are acceptable, provided that the dross does not come in contact with the PCB assembly during any portion of the soldering process.

ECSS-Q-ST-70-61_1510564

d. Dross removal material that melt, dissolve or alloy with the liquid solder and flux shall not be used.

10.2.5 Soldering temperatures

ECSS-Q-ST-70-61_1510565

a. For soldering of electronic components, the soldering-tip temperature shall be between 280 °C and 340 °C except for the cases specified in requirements 10.2.5c, 10.2.5h and 10.2.5p.

NOTE 1 Based on the component manufacturer's recommendations, solder iron can be substituted by applying, for instance, hot air to avoid thermal shock.

NOTE 2 Ceramic chip capacitors type II are highly prone to cracks in the ceramic. It has been demonstrated that the risk of cracks at completion of a verification programme is reduced by application of gentle soldering conditions where the thermal shock is minimized. It is therefore good practice to:

- Preheat the components to max 120 °C; before soldering
- Preheat the PCB to max 100°C before soldering. Lower if there is adhesive in the area to be preheated;
- Handle the preheated capacitors with thermally insulated tweezer tips;
- Soldering tip temperature of max 260 °C;
- Soldering duration of max 5 seconds;
- If the PCB pads are connected to high thermal mass it might be necessary to increase the soldering temperature to allow proper solder joint formation without increase of the duration.

ECSS-Q-ST-70-61_1510566

b. The soldering temperature may be increased in case the PCB pads are connected to high thermal mass, for component that request assembly verification, provided successful assembly verification in accordance with clause 13.

ECSS-Q-ST-70-61_1510567

c. For PTH connections, the maximum soldering temperature shall be set to, depending on the substrate:

1. Epoxy: 330 °C.
2. Polyimide: 340 °C

ECSS-Q-ST-70-61_1510568

d. For PTH, a soldering tip temperature up to 380 °C may be used for polyimide PCBs with heat sinks, wide tracks, or ground planes.

ECSS-Q-ST-70-61_1510569

e. A soldering tip temperature lower than 280 °C may be used for thermal sensitive components.

ECSS-Q-ST-70-61_1510570

f. Thermal shunts, as specified in clause 5.5.8.3, shall be used during soldering to protect thermally-sensitive components.

NOTE Example: Conductors, insulation, previously soldered connections and a non-exhaustive list of thermal sensitive components is given hereafter:

- PS Capacitors according to MIL-PRF-49470
- CSR Tantalum Capacitors according to MIL-PRF-39003
- CRH capacitors according to MIL-PRF-83421
- Filters according to MIL-PRF-28861
- Coils according to MIL-PRF-39010
- Resistor Networks according to MIL-PRF-55342
- Thermistors according to MIL-PRF-23648
- Thermistors according to GSFC spec. S-311-P-18.

ECSS-Q-ST-70-61_1510571

g. The use of thermal shunts shall not disturb or damage the solder joint, component or assembly.

ECSS-Q-ST-70-61_1510572

h. In order to improve solder flow, by order of preference, the following actions shall be taken into account:

1. Select proper solder tip and solder equipment power,

2. Introduce preheating of assembly,
3. Increase preheating temperature,
4. Increase solder temperature.

ECSS-Q-ST-70-61_1510573

i. The soldering iron tip shall be pretinned in accordance with clause 7.7.

ECSS-Q-ST-70-61_1510574

j. The soldering iron tip shall heat the joint area to the solder liquidus temperature in a time between 1 second and 2 seconds.

ECSS-Q-ST-70-61_1510575

k. The soldering iron tip shall maintain the soldering temperature at the joint throughout the soldering operation.

ECSS-Q-ST-70-61_1510576

l. The heated soldering iron tip shall be applied to the PCB pad.

ECSS-Q-ST-70-61_1510577

m. If the thermal dissipation in the PCB is too high during plated through hole soldering, additional heating may be used to be able to achieve an acceptable solder joint on the component side.

NOTE 1 Too high thermal dissipation can be due to high thermal masses or locally adjacent heat sinks.

NOTE 2 Additional heating can be applied by pre-heating of the PCB or application of heat to both sides of the plated-through hole simultaneously.

ECSS-Q-ST-70-61_1510578

n. Additional heating shall not damage the components or materials.

ECSS-Q-ST-70-61_1510579

o. The process of additional heating shall be documented.

ECSS-Q-ST-70-61_1510580

p. Soldering temperatures on component terminations shall not exceed the manufacturer recommendations.

ECSS-Q-ST-70-61_1510581

q. The supplier may exceed the component manufacturer's mandated processing conditions providing the following conditions are met:

1. successful assembly verification in accordance with clause 13,
2. dedicated tests at component level showing there is no degradation of these components, and
3. customer approval.

ECSS-Q-ST-70-61_1510582

r. Components unable to withstand machine soldering temperatures shall be hand soldered in a subsequent operation according to clause 10.3.1.

NOTE To mount component by hand soldering at very low temperature can degrade reliability of component and PCB by increasing the duration of soldering necessary to obtain an acceptable solder joint.

10.2.6 Soldering of conductors in terminals

10.2.6.1 Soldering of conductors onto terminals except cup terminals

ECSS-Q-ST-70-61_1510583

a. A concave fillet of solder shall be present between the terminal and the sides of the conductor.

ECSS-Q-ST-70-61_1510584

b. The contour of the conductor shall be visible after soldering.

ECSS-Q-ST-70-61_1510585

c. Terminals with more than one wire shall have each wire in contact with and soldered to the terminal.

NOTE The size of the terminal is selected to fit the number of wires to be soldered. The number of wires is limited so that the contour of the wire is visible and each wire has its own solder joint.

10.2.6.2 Soldering of conductors onto cup terminals

ECSS-Q-ST-70-61_1510586

a. The solder shall form a fillet between the conductor and the cup entry slot.

ECSS-Q-ST-70-61_1510587

b. The fillet shall follow the contour of the cup opening.

ECSS-Q-ST-70-61_1510588

c. The wire shall be in contact with the bottom of the cup to ensure that the solder length is sufficient.

10.3 Soldering of components, terminals, and wires into PCB through holes

10.3.1 General

ECSS-Q-ST-70-61_1510589

a. Soldering of component and wires into plated through holes shall be performed with soldering iron or wave soldering or selective wave soldering.

ECSS-Q-ST-70-61_1510590

b. Solder wire shall be applied only from the solder side of a plated through hole.

ECSS-Q-ST-70-61_1510591

c. Soldering of components into plated through holes may be performed by pin-in-paste method, provided the following conditions are met:

1. Solder fillets are compliant to clause 10.3.3.
2. Successful verification programme according to clause 13 has been carried out, where the repeatability of the pin-in-paste process is also demonstrated.

NOTE 1 It is good practice to define process design guidelines for solder volume as a function of both pin geometry and volume of plated through hole, so that proper filling of the hole can be achieved.

NOTE 2 If solder paste volume is not sufficient, solder preforms can also be added.

ECSS-Q-ST-70-61_1510592

d. Solder may be applied on the component side of a plated through hole in case pin-in-paste when the method according to requirement 10.3.1c is used.

10.3.2 Solder fillets for wires and terminations

ECSS-Q-ST-70-61_1510593

a. The molten solder shall flow around the termination and over the PCB pad.

ECSS-Q-ST-70-61_1510594

b. Solder amount shall be such that the contour of the wire is visible after soldering.

ECSS-Q-ST-70-61_1510595

c. Soldering of wires shall be performed with stress relief.

ECSS-Q-ST-70-61_1510596

d. If the wire bends from the PCB pad, the lap termination shall have a heel fillet.

10.3.3 Solder fillets for component leads in plated or non-plated through holes

ECSS-Q-ST-70-61_1510597

a. On the solder side, the molten solder shall flow around the termination and over the PCB pad.

ECSS-Q-ST-70-61_1510598

b. On the solder side, leads shall protrude through the board in accordance with clause 8.2.8.2.

ECSS-Q-ST-70-61_1510599

c. On the component side, the PCB pad shall show solder flow-through and a solder fillet between the lead and the pad for a minimum of 75 % of the circumference of the lead as illustrated in Figure 10-3(a).

ECSS-Q-ST-70-61_1510600

d. Absence of component side wetting, due to high thermal dissipation, may be accepted when acceptable solder wetting is visible inside the plated-through hole, on the hole barrel and on the lead, and the solder flow-through is minimum 90 % of PTH (laminate to laminate) as illustrated in Figure 10-3(b).

ECSS-Q-ST-70-61_1510601

e. In case requirement 10.3.3d cannot be verified by visual inspection, the solder joint may be accepted provided X-ray inspection is carried out and conforms to the following two criteria:

1. compliance to requirement 12.4a, and
2. the solder flow through is minimum 90 %.

NOTE 1 Solder wetting is difficult to assess with X-ray, therefore voids are taken into account.

NOTE 2 Examples of minimum acceptable solder flow through and maximum voids during X-ray are shown in Figure F-1.

ECSS-Q-ST-70-61_1510602

f. If the solder flow-through is less than 90 %, the component assembly shall be verification tested in compliance with requirements from clause 13.

ECSS-Q-ST-70-61_1510603

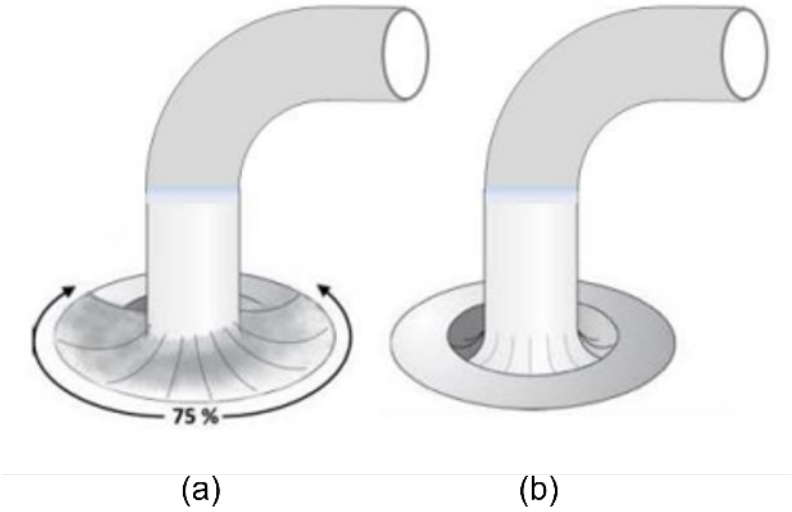
g. The solder joints to stud terminals shall meet the solder fillet requirements as illustrated in Figure E-1.

ECSS-Q-ST-70-61_1510604

h. The solder fillets for clinched leads shall meet the visual workmanship standards as illustrated in Figure E-2.

ECSS-Q-ST-70-61_1510605

i. The solder fillet for clinched leads shall be in accordance with the visual criteria for gull-wing leads in accordance with clause 10.4.10.



ECSS-Q-ST-70-61_1510606

Figure 10-3: Minimum acceptable wetting on component side

10.4 Soldering of surface mount components

10.4.1 General

ECSS-Q-ST-70-61_1510607

a. The footprint shall be such that
   1. the entire termination of the component lies on its associated footprint on the finished board.
   2. the requirements per component type from clause 10.4.2 to 10.4.14 can be fulfilled.
   3. the pad size permits the assembly of hand soldering, when applicable, without touching the component.

      NOTE 1 to item 3: It is good practice to increase the pad size to facilitate wires soldering in case of modifications.

      NOTE 2 to item 3: It is good practice to take into account the surrounding components on the PCB to allow access to the solder pad with the solder tip.

ECSS-Q-ST-70-61_1510608

b. The component shall be centred on its footprints such as the minimum termination contact length is fulfilled.

ECSS-Q-ST-70-61_1510609

c. Solder fillet shall be present on the four sides of the lead.

ECSS-Q-ST-70-61_1510610

d. Solder fillet shall show acceptable wetting on all visible sides.

NOTE Some components do not have solder fillet on the sides because of the manufacturing process: for example exposed leadframe as for L-shape Inwards package.

ECSS-Q-ST-70-61_1510611

e. On lap terminations where one side of a conductor is flush with the edge of the termination pad, a fillet of solder shall be present along at least 3 (three) of the four sides of the lead and evidence of acceptable wetting on the side without solder fillet.

ECSS-Q-ST-70-61_1510612

f. The entire component termination shall be wetted.

ECSS-Q-ST-70-61_1510613

g. In case of mounting with artificial stand-off, the minimum solder stand-off shall be repeatable within ± 50 μm.

NOTE The stand-off enables adequate cleaning beneath the assembled LCCC and enhances solder fatigue life.

10.4.2 Rectangular and square end-capped or end-metallized leadless chip

ECSS-Q-ST-70-61_1510614

a. There shall be no discernible discontinuities in the solder coverage of the terminal areas of components.

ECSS-Q-ST-70-61_1510615

b. Solder shall not encase any portion of the body of the component following reflow.

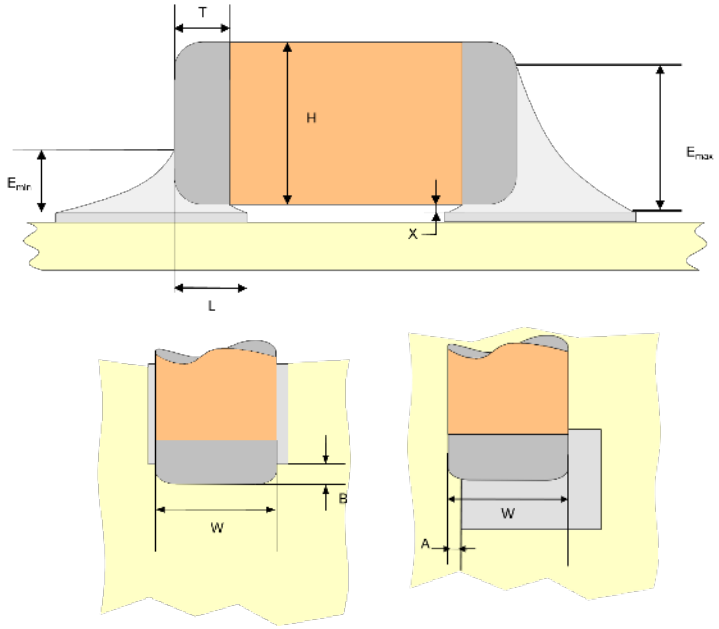
ECSS-Q-ST-70-61_1510616

c. The solder joints to these components shall meet the dimensional and solder fillet requirements of Figure 10-4 and Table 10-1.

NOTE 1 Ceramic chip capacitors or resistors, ceramic resistor arrays and metallic chip components such as CSM2512 or resistors with metallic terminations such as SMS 2512, ferrites, thermistors and fuses, are all examples of components in this group.

NOTE 2 Convex solder fillet can cause additional stress in the component terminations, therefore convex solder fillets are not recommended. Especially for ceramic chip capacitors it has been demonstrated that a lower wetting height reduces the risk of cracks in the ceramic at the completion of verification.

NOTE 3 Manual soldering, especially with artificial stand-off can make it difficult to fulfil maximum side overhang and minimum termination contact lengths.



ECSS-Q-ST-70-61_1510617

Figure 10-4: Mounting of rectangular and square end-capped and end-metallized components

ECSS-Q-ST-70-61_1510618

Table 10-1: Dimensional and solder fillet for rectangular and square end capped components

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W Not permitted for assembly sensitive component
End overhang	B	Not permitted
Minimum termination contact length	L	0,75 × T on one end of the component only 100 % for assembly sensitive components
Minimum fillet height	E_{min}	X + 0,3 × H or X + 0,5 mm whichever is less
Minimum fillet width	W-A	100% × W or minimum 90% in case of overhang
Maximum fillet height*	E_{max}	*: only for chip capacitor $E_{max} \leq H$
Solder Stand-off (elevation)	X	Present
Maximum tilt limit	in accordance with requirement 10.2.2f	
Termination width	W	
Component height	H	
Termination length	T	

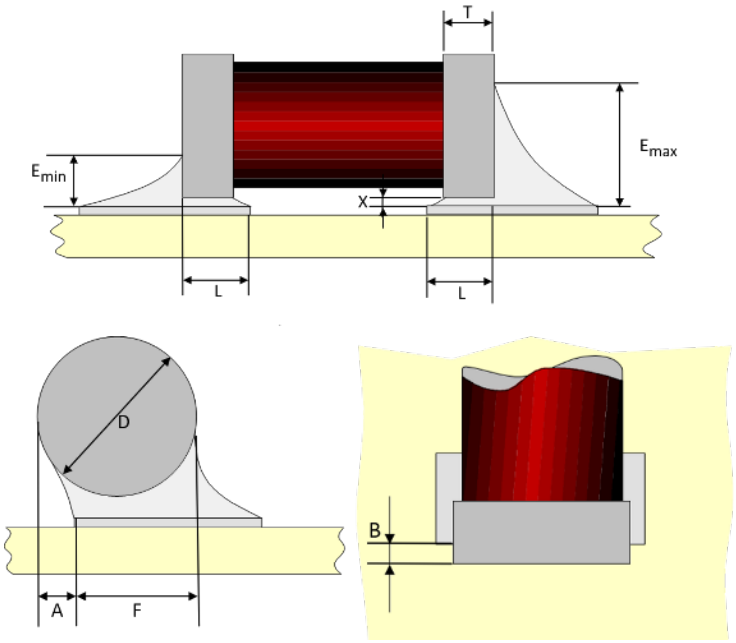
10.4.3 Cylindrical and square end-capped components with cylindrical or oval body

ECSS-Q-ST-70-61_1510619

a. Solder joints to components having cylindrical terminations shall meet the dimensional and solder fillet requirements of Figure 10-5 and Table 10-2.

ECSS-Q-ST-70-61_1510620

b. Solder joints to components having square terminations shall meet the dimensional and solder fillet requirements of Figure 10-6 and Table 10-3.



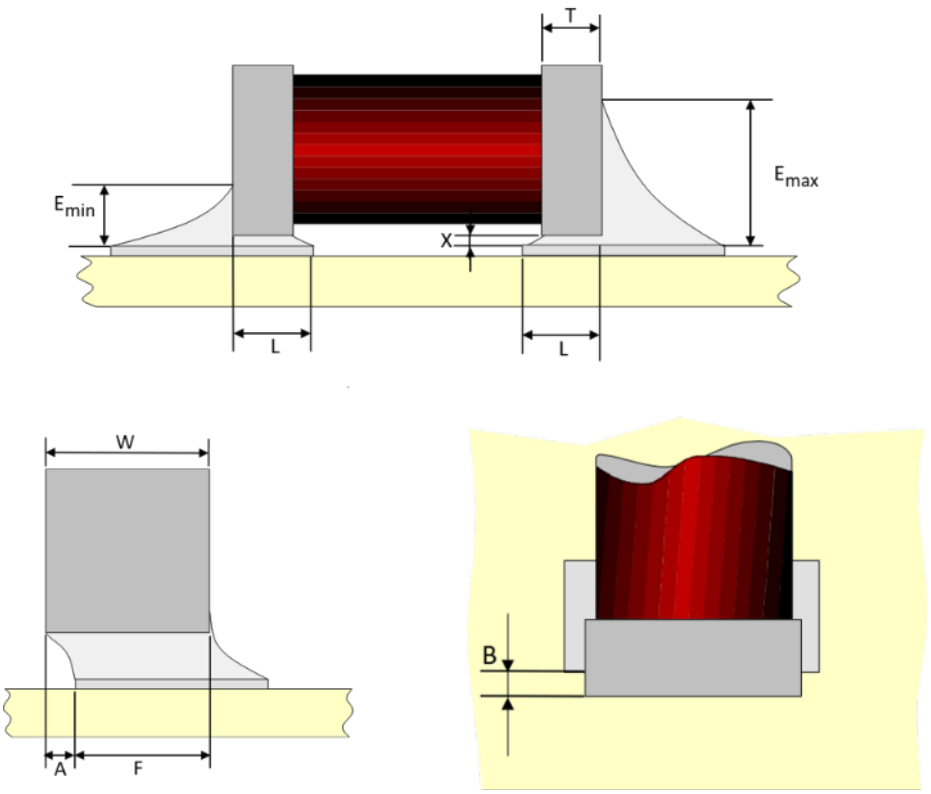
ECSS-Q-ST-70-61_1510621

Figure 10-5: Mounting of cylindrical end-capped components

ECSS-Q-ST-70-61_1510622

Table 10-2: Dimensional and solder fillet for cylindrical end-capped components

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,25 × D (diameter)
End overhang	B	Not permitted
Minimum fillet width	F	0,5 × D
Minimum fillet height	E_{min}	X + 0,3 × D or X + 1,0 mm whichever is less
Maximum fillet height	E_{max}	D
Minimum termination contact length	L	0,75 × T on one end of the component only 100% for assembly sensitive components
Stand-off (elevation)	X	Present
Maximum tilt limit	in accordance with requirement 10.2.2f	
Termination diameter	D	
Termination length	T	



ECSS-Q-ST-70-61_1510623

Figure 10-6: Mounting of square end-capped components

ECSS-Q-ST-70-61_1510624

Table 10-3: Dimensional and solder fillet for square end-capped components

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,25 × W (square width)
End overhang	B	Not permitted
Minimum fillet width	F	0,75 × W
Minimum fillet height	E_{min}	X + 0,3 × W or X + 1,0 mm whichever is less
Maximum fillet height	E_{max}	W
Minimum termination contact length	L	0,75 × T on one end of the component only 100% for assembly sensitive components
Stand-off (elevation)	X	Present
Maximum tilt limit	in accordance with requirement 10.2.2f	
Termination length	T	
Termination width	W	

10.4.4 Bottom terminated chip components

ECSS-Q-ST-70-61_1510625

a. Devices having metallized terminations on the bottom side only shall meet the dimensional and solder fillet requirements of Figure 10-7 and Table 10-4.

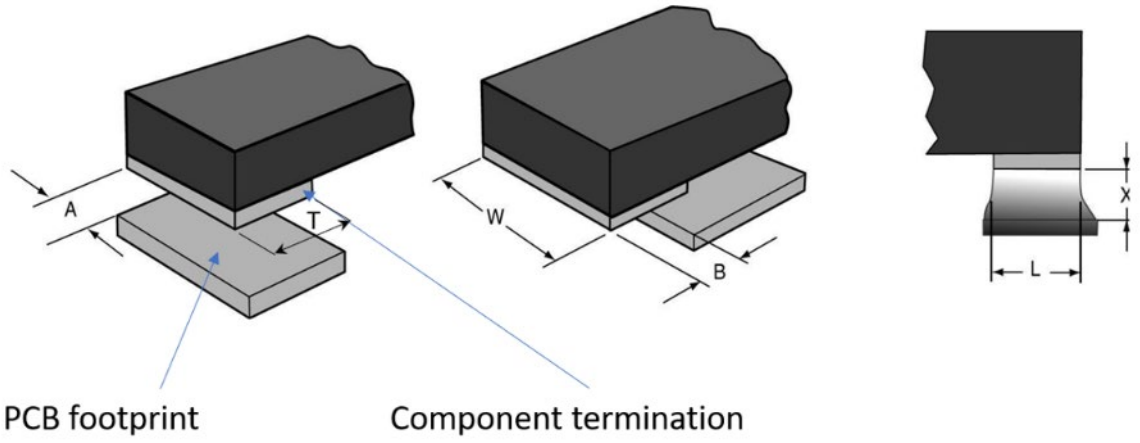
NOTE Examples of components from this family are SMD coils.

ECSS-Q-ST-70-61_1510626

b. Solder fillet shall show acceptable wetting on all visible sides.

ECSS-Q-ST-70-61_1510627

c. Assembly shall be inspected with X-ray according to criteria defined in requirement 12.4a when solder fillet is not visible.



ECSS-Q-ST-70-61_1510628

Figure 10-7: Mounting of bottom terminated chip component

ECSS-Q-ST-70-61_1510629

Table 10-4: Dimensional and solder fillet for bottom terminated chip components

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W Not permitted for assembly sensitive component
End overhang	B	Not permitted
Minimum termination contact length	L	0,75 × T on one end of the component only Entire termination for assembly sensitive components
Minimum fillet width	W-A	100% × W or minimum 90% in case of overhang
Solder Stand-off (elevation)	X	Present
Maximum tilt limit	in accordance with requirement 10.2.2f	
Termination width	W	
Termination length	T	

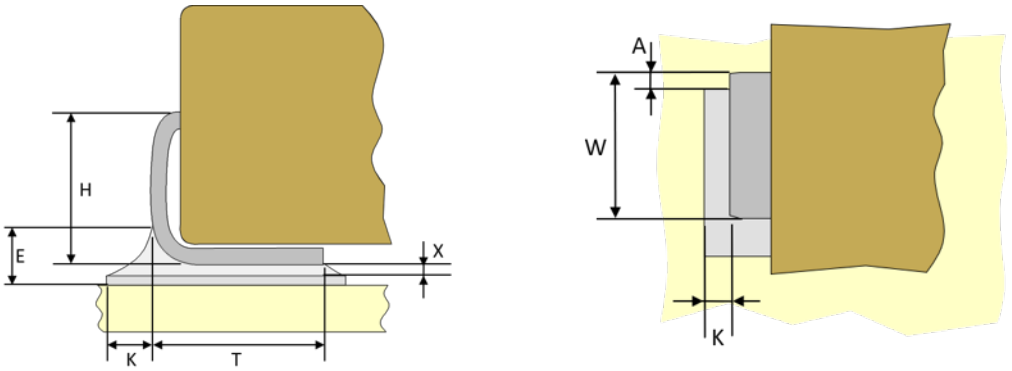
10.4.5 L-Shape inwards components

ECSS-Q-ST-70-61_1510630

a. Components having L-shape inwards terminals shall meet the dimensional and solder fillet requirements of Figure 10-8 and Table 10-5.

ECSS-Q-ST-70-61_1510631

b. Solder fillet shall show acceptable wetting on all visible sides.



ECSS-Q-ST-70-61_1510632

Figure 10-8: Mounting of components with "L-shape inwards" leads

ECSS-Q-ST-70-61_1510633

Table 10-5: Dimensional and solder fillet for "L-shape inwards" components

Parameter	Dimension	Dimensions limits
Maximum side overhang	A	0,1 × W
Minimum heel fillet height	E	(0,25 x H) +X or X +1mm whichever is less
Minimum fillet width	W-A	100%xW or minimum 90% in case of overhang
Minimum distance to footprint edge	K	0,2 mm
Minimum termination contact length	L	0,75 × T on one end of the component only 100% of T for assembly sensitive components
Stand-off (elevation)	X	Present
Lead height	H	
Lead width	W	
Termination length	T	

10.4.6 Leadless component with plane termination

ECSS-Q-ST-70-61_1510634

a. Leadless components with plane termination shall meet the dimensional and solder fillet requirements of Figure 10-9 and Table 10-6.

NOTE Leadless components with plane termination can have a metallic plane or non-metallic plane termination.

ECSS-Q-ST-70-61_1510635

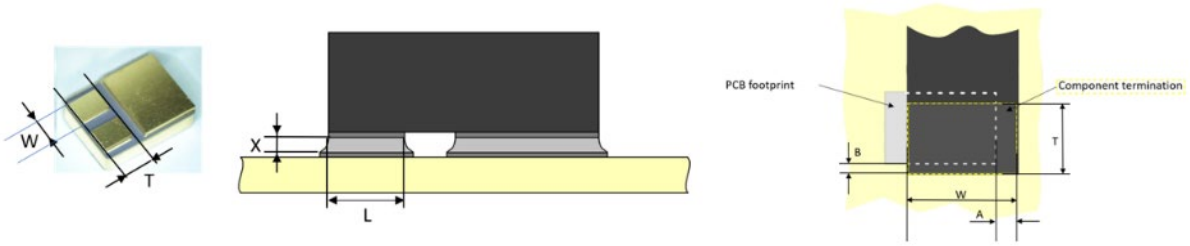
b. Solder fillet shall show acceptable wetting on all visible sides.

ECSS-Q-ST-70-61_1510636

c. Assembly shall be inspected with X-ray according to criteria defined in requirement 12.4a when solder fillet is not visible.

ECSS-Q-ST-70-61_1510637

d. When either thermal or electrical ground performances are requested, terminal plane shall be inspected with X-ray according to criteria defined in requirement 12.4a.



ECSS-Q-ST-70-61_1510638

Figure 10-9: Mounting of leadless component with plane termination

ECSS-Q-ST-70-61_1510639

Table 10-6: Dimensional and solder fillet for leadless component with plane termination

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W providing minimum insulation distance remains acceptable. Not permitted for assembly sensitive component
End overhang	B	Not permitted
Minimum termination contact length	L	Entire termination of component T
Minimum fillet width	W-A	100% × W or minimum 90% in case of overhang
Solder Stand-off (elevation)	X	Present
Maximum tilt limit	in accordance with requirement 10.2.2f	
Termination width	W	
Termination length	T	

10.4.7 Leaded component with plane termination

ECSS-Q-ST-70-61_1510640

a. Leaded components with plane termination shall meet the dimensional and solder fillet requirements of Figure 10-10 and Table 10-7.

ECSS-Q-ST-70-61_1510641

b. Solder fillet shall be present on the visible edge of the terminal plane.

ECSS-Q-ST-70-61_1510642

c. Terminal plane shall be inspected with X-ray according to criteria defined in requirement 12.4a.

ECSS-Q-ST-70-61_1510643

Figure 10-10: Mounting of leaded components with plane termination

ECSS-Q-ST-70-61_1510644

Table 10-7: Dimensional and solder fillet for leaded components with plane termination

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum distance to footprint edge at toe	B	0,20 mm
Minimum distance to footprint edge at heel	K	0,5 × W
Minimum heel fillet height	E	X + T
Minimum fillet width	W-A	100% × W or minimum 90% in case of overhang
Solder Stand-off	X	Present
Lead thickness	T	
Lead width	W	

10.4.8 Leadless castellated ceramic chip carrier components

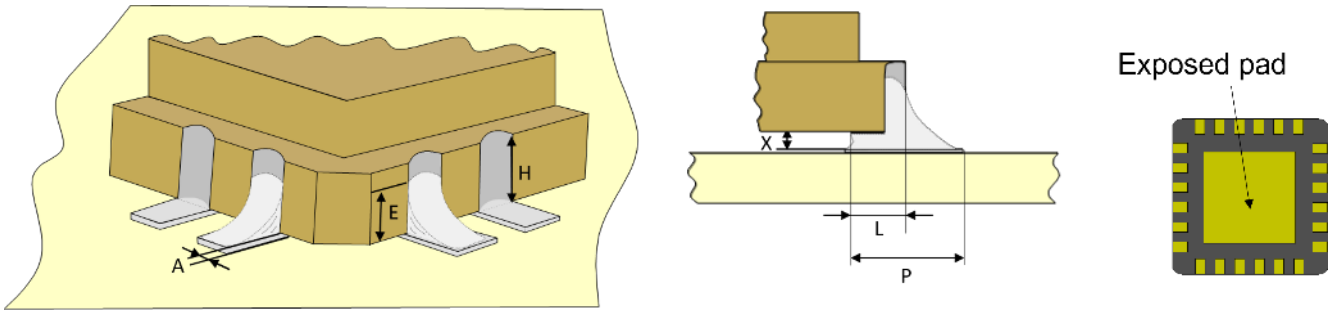
ECSS-Q-ST-70-61_1510645

a. Solder joints to leadless castellated ceramic chip carrier terminations shall meet the dimensional and solder fillet requirements of Figure 10-11 and Table 10-8.

NOTE It can be difficult to assess the wetting in X-ray, but solder joints with deviating shape or amount compared to the neighbouring connections indicate that a closer look is needed.

ECSS-Q-ST-70-61_1510646

b. Exposed pad shall be inspected with X-ray according to criteria defined in requirement 12.4a.



ECSS-Q-ST-70-61_1510647

Figure 10-11: Mounting of leadless castellated ceramic chip carrier components

ECSS-Q-ST-70-61_1510648

Table 10-8: Dimensional and solder fillet for leadless castellated ceramic chip carrier components

Parameter	Dimension	Dimension limits
Maximum side overhang	A	Not permitted
Minimum fillet height	E	0,75 × H
Minimum fillet width	-	100% termination width
Solder Stand-off (elevation)	X	Present
Minimum termination contact length	L	Entire termination of component
Castellation metallisation height	H	
Pad length	P	

10.4.9 No lead Quad Flat Pack

ECSS-Q-ST-70-61_1510649

a. Solder joints formed to QFN shall meet the dimensional and solder fillet requirements of Figure 10-12 and Table 10-9.

NOTE Presence or absence of external solder fillet is depending on package technology.

ECSS-Q-ST-70-61_1510650

b. Solder fillet shall show acceptable wetting on all visible sides.

ECSS-Q-ST-70-61_1510651

c. Heel solder fillet shall be present.

ECSS-Q-ST-70-61_1510652

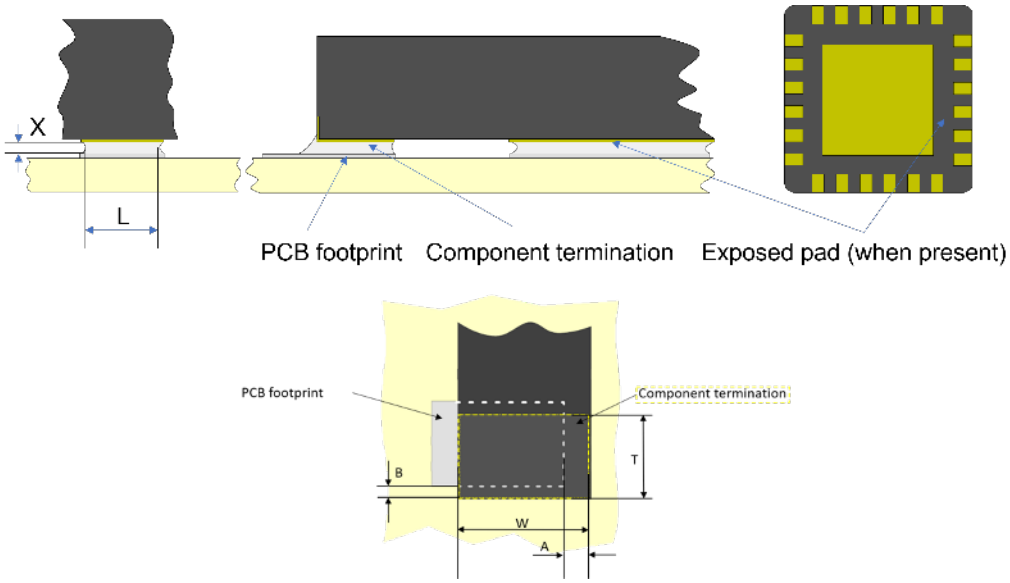
d. Assembly shall be inspected with X-ray according to criteria defined in requirement 12.4a when solder fillet is not visible.

ECSS-Q-ST-70-61_1510653

e. When either thermal or electrical ground performances are requested, exposed pad shall be inspected with X-ray according to criteria defined in requirement 12.4a.

ECSS-Q-ST-70-61_1510654

f. X-ray inspection may be omitted providing justification and approval of Approval Authority.



ECSS-Q-ST-70-61_1510655

Figure 10-12 Mounting of QFN

ECSS-Q-ST-70-61_1510656

Table 10-9: Dimensional and solder fillet for QFN components

Parameter	Dimension	Dimension limits
Maximum side overhang	A	Not permitted
End overhang	B	Not permitted
Minimum termination contact length	L	Entire termination of component
Solder Stand-off (elevation)	X	Present
Solder fillet height	H	In compliance with verification results
Minimum fillet width	W-A	100% × W
Maximum tilt limit	in accordance with requirement 10.2.2f	
Termination width	W	
Termination length	T	

10.4.10 Flat pack and gull-wing leaded components with round, rectangular, ribbon leads

ECSS-Q-ST-70-61_1510657

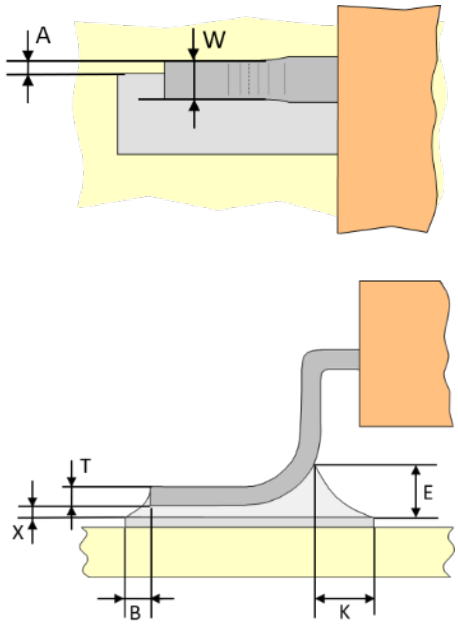
a. Solder joints formed to flat pack and gull-wing leaded components with round, rectangular, ribbon leads shall meet the dimensional and solder fillet requirements of Figure 10-13 and Table 10-10.

ECSS-Q-ST-70-61_1510658

b. Solder fillet shall be present on the four sides of the lead.

ECSS-Q-ST-70-61_1510659

c. When exposed pad is soldered, it shall be inspected with X-ray according to criteria defined in requirement 12.4a.



ECSS-Q-ST-70-61_1510660

Figure 10-13: Mounting of gull-wing leaded components with round, rectangular, ribbon leads

ECSS-Q-ST-70-61_1511129

Table 10-10: Dimensional and solder fillet for gull-wing leaded components with round, rectangular, ribbon leads

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum distance to footprint edge at toe	B	0,20 mm
Minimum distance to footprint edge at heel	K	0,5 × W
Minimum heel fillet height	E	X + T
Minimum fillet width	W-A	100% × W or minimum 90% in case of overhang
Solder Stand-off	X	Present
Lead thickness	T	
Lead width	W	

10.4.11 Components with “J” leads

ECSS-Q-ST-70-61_1510661

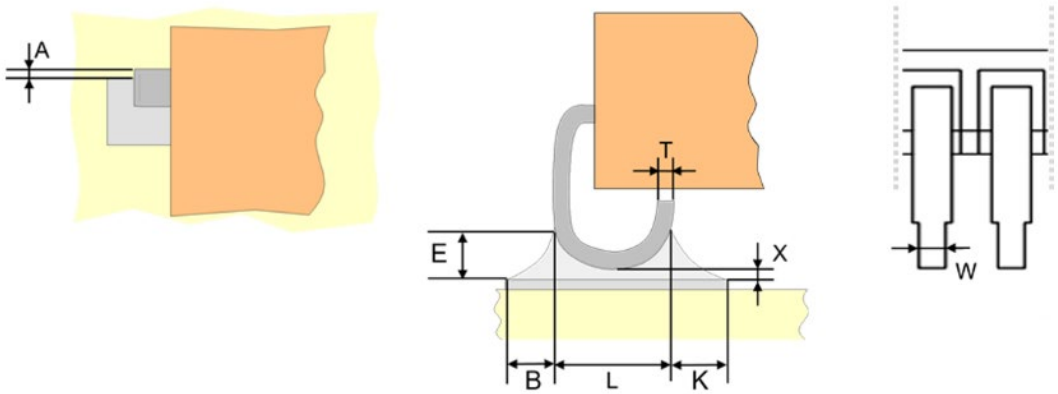
a. Solder joints formed to “J” and “V” shaped leads shall meet the dimensional and solder fillet requirements of Figure 10-14 and Table 10-11.

ECSS-Q-ST-70-61_1510662

b. The fillet of solder along the lead shall extend up to a minimum distance of half the lead thickness or diameter.

ECSS-Q-ST-70-61_1510663

c. When exposed pad is soldered, it shall be inspected with X-ray according to criteria defined in requirement 12.4a.



ECSS-Q-ST-70-61_1510664

Figure 10-14: Mounting of component with “J” leads

ECSS-Q-ST-70-61_1510665

Table 10-11: Dimensional and solder fillet for components with “J” leads

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum termination contact length	L	100% on the pad
Minimum heel fillet height	Eh	X+T
Minimum toe fillet height	Ef	X+T
Minimum fillet width	W-A	100% × W or minimum 90% in case of overhang
Minimum distance to footprint edge at toe	B	0,20 mm or 0,5 × W whichever is the smaller
Minimum distance to footprint edge at heel	K	0,20 mm or 0,5 × W whichever is the smaller
Minimum stand-off	X	Present
Lead thickness	T	
Lead width	W	

10.4.12 Components with ribbon terminals without stress relief

ECSS-Q-ST-70-61_1510666

a. Solder joints formed shall meet the dimensional and solder fillet requirements of Figure 10-15 and Table 10-12.

NOTE When component dimensions allow, it is good practice to have a minimum termination contact length L of three times the lead width W.

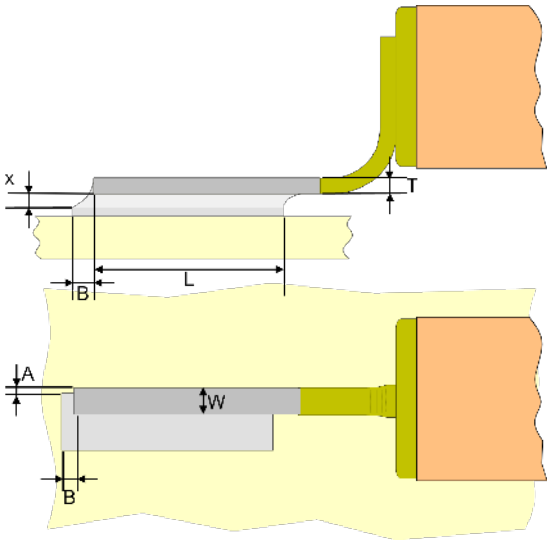
ECSS-Q-ST-70-61_1510667

b. The degolding and pretinning zone shall be larger than the PCB footprint without reducing the clearance distance of the component.

NOTE The aim is to prevent soldering to gold plated surfaces.

ECSS-Q-ST-70-61_1510668

c. The fillet of solder along the lead shall extend up the side of the lead to a minimum distance of half the lead thickness or diameter.



ECSS-Q-ST-70-61_1510669

Figure 10-15: Mounting of components without stress relief

ECSS-Q-ST-70-61_1510670

Table 10-12: Dimensional and solder fillet for components with ribbon terminals without stress relief

Parameter	Dimension	Dimensions limits
Maximum side overhang	A	0,1 × W
Minimum distance to footprint edge at toe	B	0,20 mm
Minimum fillet width	W-A	100% × W or minimum 90% in case of overhang

Parameter	Dimension	Dimensions limits
Stand-off	X	Present
Minimum termination contact length	L	Fully soldered lap connection
Maximum tilt limit	in accordance with requirement 10.2.2f	
Lead thickness	T	
Lead width	W	

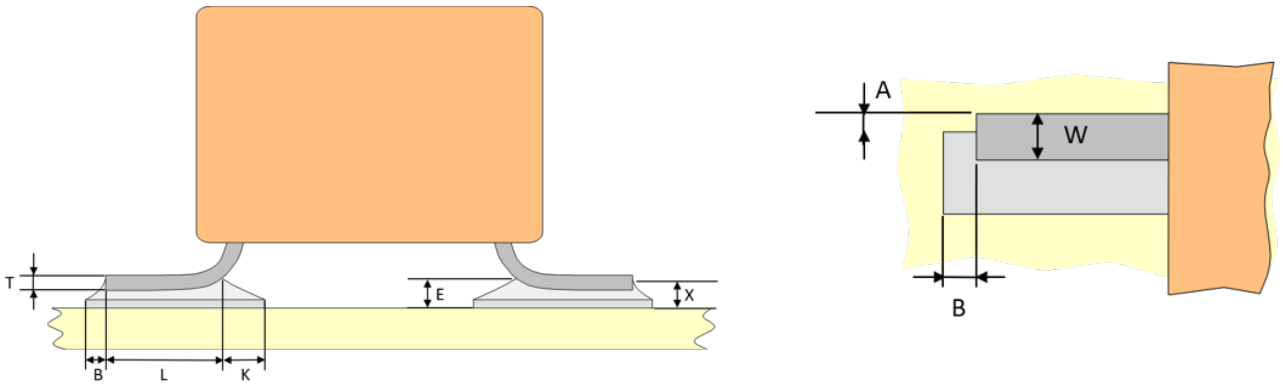
10.4.13 Stacked modules components with leads protruding vertically from bottom

ECSS-Q-ST-70-61_1510671

a. Stacked module components shall meet the dimensional and solder fillet requirements of Figure 10-16 and Table 10-13.

ECSS-Q-ST-70-61_1510672

b. Solder fillet shall be present on the four sides of the lead.



ECSS-Q-ST-70-61_1510673

Figure 10-16: Mounting of stacked module components with leads protruding vertically from bottom

ECSS-Q-ST-70-61_1510674

Table 10-13: Dimensional and solder fillet for stacked module components with leads protruding vertically from bottom

Parameter	Dimension	Dimension limits
Maximum side overhang	A	0,1 × W
Minimum distance to footprint edge at toe	B	0,20 mm
Minimum distance to footprint edge at heel	K	0,5 × W
Minimum termination contact length	L	Entire termination of component
Minimum heel fillet height	E	Wetting solder visible in the heel fillet, X+ 0,5T
Minimum fillet width	W-A	100% × W or minimum 90% in case of overhang
Solder Stand-off	X	Present
Lead thickness	T	
Lead width	W	

10.4.14 Area array devices

ECSS-Q-ST-70-61_1510675

a. The connections of area array devices shall meet the dimensional and solder fillet requirements of Figure 10-17 and Table 10-14.

ECSS-Q-ST-70-61_1510676

b. The outer rows shall be visually inspected.

ECSS-Q-ST-70-61_1510677

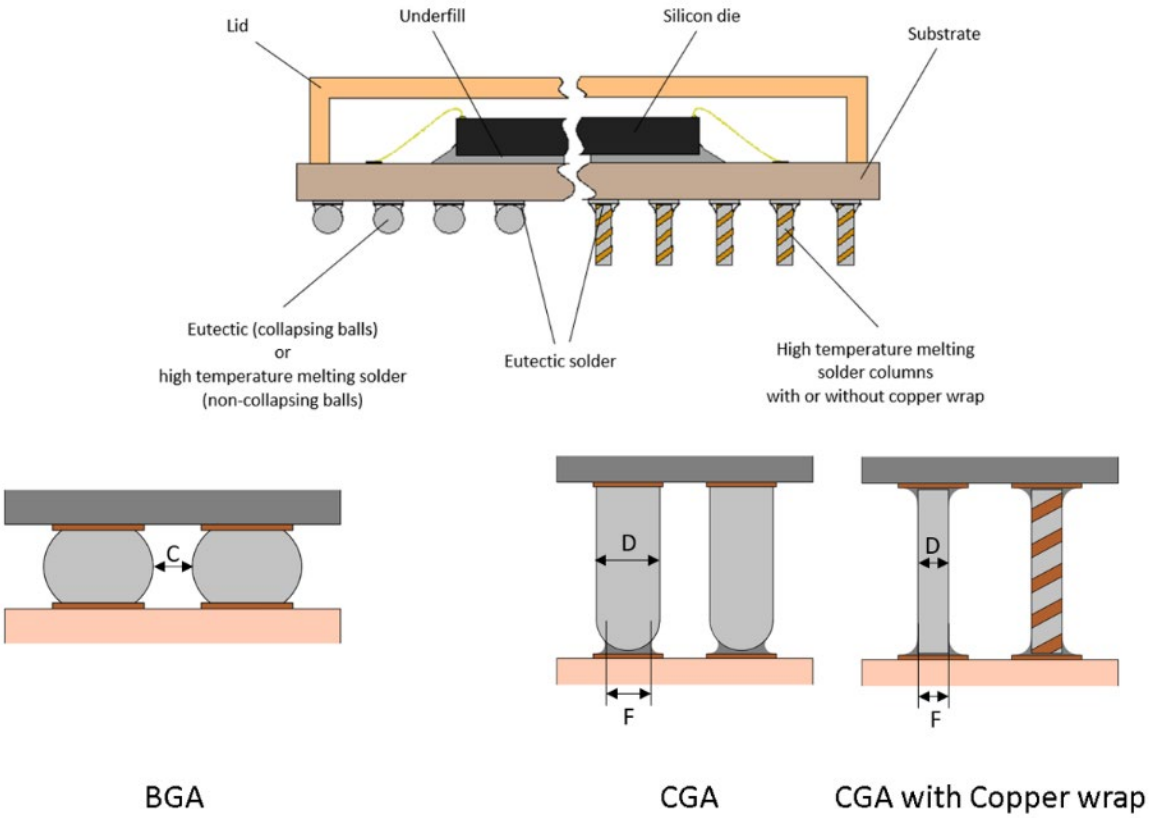
c. Solder joints shall be inspected with X-ray according to criteria defined in requirement 12.4a.

NOTE 1 As it is impossible to visually inspect solder joints to area array components, reliability of these components cannot be assured by inspection and rework. Even using X-Ray techniques, some types of defect are difficult to detect. Therefore, reliability of these solder joints can only be assured by robust process control.

NOTE 2 Examples of typical area array components are shown in Figure 10-17.

ECSS-Q-ST-70-61_1510678

d. X-ray techniques shall be used to verify the acceptable wetting, the absence of bridge, solder balls and minimum electrical clearance.



ECSS-Q-ST-70-61_1510679

Figure 10-17: Typical configuration of ceramic grid array component

ECSS-Q-ST-70-61_1510680

Table 10-14: Dimensional and solder fillet for area array devices

	Parameter	Dimension	Dimension limits
General	Wetting	-	All connections show evidence of contact and wetting to its solder land.
	Solder balls	-	No solder balls
BGA	Electrical clearance	C	Electrical clearance is not violated and $C \geq 0{,}1$ mm
CGA	Column tilting	-	Maximum 10°
	Misalignment	-	No footprint overhang
	Minimum fillet width	F	CGA with rounded bottom column: $F \geq 0{,}5 \times D$ CGA with flat bottom column: $F \geq 1{,}0 \times D$
	Column diameter	D	

10.5 Rework and repair

10.5.1 Removal of solder on unpopulated PCB

ECSS-Q-ST-70-61_1510681

a. Removal of solder shall be performed after the board has been submitted to bake out in compliance with clause 7.3.

ECSS-Q-ST-70-61_1510682

b. Rework of plated through holes in PCBs may be performed up to maximum 25 % per component position with a maximum of 3 (three) times for the same plated through hole.

NOTE 1 Plated through holes can be blocked from PCB manufacturer in case of small hole dimensions.

NOTE 2 See also ECSS-Q-ST-70-60 requirement 10.6.3g.

NOTE 3 "3 times" includes rework after assembly.

ECSS-Q-ST-70-61_1510683

c. The number and location of reworks performed according to 10.5.1b shall be recorded in the traveller sheet of the board.

ECSS-Q-ST-70-61_1510684

d. For unpopulated PCB, in case more that 25 % per component position are reworked, the removal of solder shall be classified as a repair and be performed in accordance with ECSS-Q-ST-70-28.

10.5.2 Rework, repair and modifications

ECSS-Q-ST-70-61_1510685

a. Any rework, repair or modifications shall be in accordance with ECSS-Q-ST-70-28 with the exceptions of all requirements of clause 10.5.1 and requirements 10.5.2b to 10.5.2h.

NOTE The deviation to ECSS-Q-ST-70-28 comes from the fact that the complexity of electronic components has evolved since the publication of ECSS-Q-ST-70-28. In particular the number of component leads and their density on the board have increased drastically.

ECSS-Q-ST-70-61_1510686

b. Retinnning of PCB pads after component removal shall be done in accordance with requirement 7.6.3.1d.

ECSS-Q-ST-70-61_1510687

c. Rework of soldered PCB assemblies shall be done when the solder joint does not meet the criteria of clause 12.

ECSS-Q-ST-70-61_1510688

d. The total number of solder reworks, including the ones done prior to soldering according to requirement 10.5.1b shall not exceed three times per PCB pad, except in case for epoxy substrates covered by requirement 10.5.2e.

NOTE 1 Epoxy and flex rigid PCB are sensitive to thermal stress induced by rework.

NOTE 2 For reworking, the solder can be completely removed from the termination.

NOTE 3 In case of high thermal mass, it is good practice to have a preheating of components and PCB.

ECSS-Q-ST-70-61_1510689

e. For epoxy substrates, the total number of solder reworks or repair, including the ones done prior to soldering according to requirement 10.5.1b shall not exceed two times per PCB pad.

NOTE This means it is allowed to perform either two reworks or one rework and one repair.

ECSS-Q-ST-70-61_1510690

f. The number of reworked solder joints shall not exceed 10 % of the total number of solder joints on a board with the exception specified in requirements 10.5.2g and 10.5.2h.

ECSS-Q-ST-70-61_1510691

g. For boards smaller than 25 cm^2 the number of reworked solder joints shall not exceed 25 % of the total number of solder joints on a board.

ECSS-Q-ST-70-61_1510692

h. For components with more than one hundred terminations, the number of reworked solder joints shall not exceed 25 % of the total number of solder joints of the component.

ECSS-Q-ST-70-61_1510693

i. Type II ceramic chip capacitors shall not be reworked.

ECSS-Q-ST-70-61_1510694

j. Wiring of chip capacitors type II soldered on its footprint as identified in the ECSS-Q-ST-70-28C shall not be performed due to possible thermal shock.

ECSS-Q-ST-70-61_1510695

k. Wiring of a chip capacitor type II soldered on its footprint may be acceptable provided that the assembly of the capacitor and the wiring is done in a single operation.

ECSS-Q-ST-70-61_1510696

l. Wiring a chip capacitor type II bonded on PCB as described in clause I.3.7 of ECSS-Q-ST-70-28 shall not be performed.

ECSS-Q-ST-70-61_1510697

m. Ceramic chip capacitors with flexible terminations shall not be reworked.

ECSS-Q-ST-70-61_1510698

n. Ceramic chip capacitors with flexible terminations may be reworked providing the use of an appropriate procedure that avoids any thermal shock and is successfully verified according to clause 13 and approved by Approval Authority.

ECSS-Q-ST-70-61_1510699

o. Wiring a tantalum capacitor bonded on PCB as described in clause I.3.7 of ECSS-Q-ST-70-28 shall not be performed.

10.6 High-voltage connections

ECSS-Q-ST-70-61_1510700

a. Soldered joints shall be performed such to avoid Corona discharge.

ECSS-Q-ST-70-61_1510701

b. Soldered joints for corona suppression shall be performed in two stages with an intermediate inspection:

1. The first soldering stage produces a standard soldered connection in accordance with clause 12,
2. This connection is inspected for compliance with clauses 12.2 and 12.3,
3. The joint then has additional solder alloy added,
4. The second soldering stage produces a final joint, as shown in Figure 10-18, having:
   (a) smooth convex fillets,
   (b) no discontinuities,
   (c) no severe changes in contour,
   (d) no sharp edges or points.

NOTE High voltage applications are described in ECSS-E-HB-20-05.

ECSS-Q-ST-70-61_1510702

Figure 10-18: High voltage connection

10.7 Solderless components

ECSS-Q-ST-70-61_1510703

a. Solderless connection configuration shall be identified in the DCL.

ECSS-Q-ST-70-61_1510704

b. Solderless connection configuration shall be identified during the assembly MPCB.

ECSS-Q-ST-70-61_1510705

c. Acceptance criteria for the assembly shall be proposed by the supplier based on the design and assembly verification results.

NOTE It is good practice to perform X Ray inspection.

ECSS-Q-ST-70-61_1510706

d. No overhang shall be permitted.

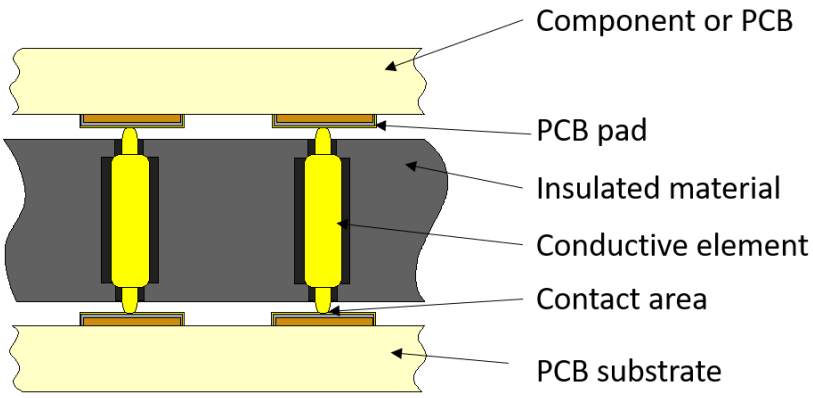


Figure 10-19: Solderless assembly configuration

11
Post soldering process requirements

11.1 Cleaning of PCB assemblies

11.1.1 General

ECSS-Q-ST-70-61_1510707

a. When the solder has solidified and cooled, flux and residue shall be removed using a solvent in accordance with clause 6.4.

ECSS-Q-ST-70-61_1510708

b. Contamination of electrical contact surfaces by the dissolved flux residues shall be prevented.

NOTE 1 Non hermetic components such as connectors, switches and solderless contacts can be degraded by such contamination.

NOTE 2 The protection can be performed using a mask.

NOTE 3 Examples of electrical contact surfaces are those in switches, potentiometers, or connectors.

ECSS-Q-ST-70-61_1510709

c. When insulated wires are on a board, local cleaning shall be performed in such a manner that avoids penetration of solvent under wire insulation and prevents its entry into the interior of components.

ECSS-Q-ST-70-61_1510710

d. Flux and residue shall be removed within a maximum period of 8 hours after soldering operations.

NOTE 1 It is good practice to remove flux residues directly after the soldering operation because even rosin fluxes are difficult to remove after longer ageing.

NOTE 2 Longer period can be considered with a successful SIR test presented to Approval Authority.

ECSS-Q-ST-70-61_1510711

e. All fluxes, machine oils and ionisable contaminants on the assembly shall be removed within one hour of the wave soldering operation.

ECSS-Q-ST-70-61_1510712

f. PCB assemblies shall not be immersed in cleaning solvents for more than 30 minutes for each cleaning operation.

NOTE Long immersion times can promote galvanic corrosion between adjacent metallic surfaces.

ECSS-Q-ST-70-61_1510713

g. Ultrasonic cleaning shall not be used for PCBs populated with components.

11.1.2 Verification of cleanliness

ECSS-Q-ST-70-61_1510714

a. The verification of the PCB cleanliness shall be performed for the following cases:
   1. for the first verification programme performed by a company or
   2. if the conditions of Table 13-1 request it.

      NOTE Demonstration of cleanliness on a larger package such as AAD can be done by breaking off the package body of one of the verification samples after assembly and cleaning. Inspection is done under magnification to detect any flux residues to replace the SIR test.

ECSS-Q-ST-70-61_1510715

b. The supplier shall demonstrate the cleanliness level for each combination of substrate material type, flux type, soldering process and cleaning process.

ECSS-Q-ST-70-61_1510716

c. The cleanliness verification shall be done for a flight representative production flow.

   NOTE 1 A typical production flow can include collective assembly, automatic cleaning machine, manual soldering as well as manual cleaning.

   NOTE 2 It is recommended to include extra test samples with a subset of the process flow, for example only collective or only manual soldering with associated cleaning, for failure investigation in case of non-conformances. It is also good practice to include reference bare PCB samples which have only been cleaned and baked.

ECSS-Q-ST-70-61_1510717

d. The effectiveness of the cleaning shall be verified with the following tests:
   1. Sodium chloride (NaCl) equivalent ionic contaminants test in accordance with clause 11.1.4.
   2. Surface Insulation Resistance (SIR) test in accordance with clause 11.1.3.

      NOTE On FM boards, the effectiveness of the cleaning can be verified by using a UV lamp from 300 nm - 400 nm range.

11.1.3 Surface Insulation Resistance (SIR) testing

ECSS-Q-ST-70-61_1510718

a. SIR test shall be implemented at first verification and after any process changes according to Table 13-1 or due to the introduction of components for which cleanliness testing is considered worst case and not covered by previous analysis.

ECSS-Q-ST-70-61_1510719

b. Surface Insulation Resistance (SIR) testing shall be performed in accordance with IPC-TM-650 Test method 2.6.3.7, with the following modifications:

1. The test PCBs consist of same PCB material type and surface finish and solder mask, if applicable, as the flight boards.
2. The test patterns are as minimum compliant to IPC-B-36.
3. The SIR test board pattern is adapted to the product design with test patterns representing the components of finest pitch and components with lowest stand-off to the PCB.
4. The SIR test boards is populated for process and product representativity.
5. The minimum number of SIR test boards is one.
6. The SIR test sample is submitted to a flight representative production flow with regards to all handling, cleaning, baking and soldering operations.
7. The test boards are visually inspected in accordance with flight representative procedures.
8. The duration of the testing is as a minimum 168 hours,
9. The SIR is measured every 20 minutes during the complete duration of the test.

NOTE 1 to item 3: Fine-pitch and low stand-off components are of highest risk in case of electromigration.

NOTE 2 to item 3: For the same component width, longer chips are more difficult to clean. For the same component length, wider chips are more difficult to clean.

NOTE 3 to item 4: Commercial plastic components can be used as long as the pitch and stand-off is representative.

ECSS-Q-ST-70-61_1510720

c. The applied voltage during test may be modified from IPC-TM-650 Test method 2.6.3.7 to be representative of flight hardware.

ECSS-Q-ST-70-61_1510721

d. The acceptance criteria for SIR testing shall be as follows:

1. the surface insulation resistance exceeds 100 MΩ during the complete testing,
2. the conductor spacing is not reduced,
3. dendrites are absent,
4. No corrosion of the conductors is visible.

NOTE Minor discoloration of one pole of the comb pattern conductors is acceptable.

11.1.4 Sodium chloride (NaCl) equivalent ionic contaminants testing

ECSS-Q-ST-70-61_1510722

a. Sodium chloride (NaCl) equivalent ionic contaminants shall be measured as follows:

1. Use a solution of 75 % isopropyl alcohol and 25 % deionized water for the sodium chloride (NaCl) equivalent ionic contaminants test.
2. Calibrate the equipment using a sodium chloride solution of known quantity and composition.

ECSS-Q-ST-70-61_1510723

b. Testing shall be performed according to the equipment manufacturer's specification.

ECSS-Q-ST-70-61_1510724

c. The minimum number of test boards for sodium chloride NaCl equivalent ionic contaminants testing shall be one.

ECSS-Q-ST-70-61_1510725

d. The test boards shall be visually inspected in accordance with flight representative procedures.

ECSS-Q-ST-70-61_1510726

e. The cleanliness test values shall be as follows:

1. Starting resistivity: greater than 20×10^6 Ω cm.
2. Ending value: The sodium chloride (NaCl) ionic contaminants equivalence value be less than 0,70 μg/cm^2 of PCB surface area.

11.1.5 Monitoring of cleanliness

ECSS-Q-ST-70-61_1510727

a. The effectiveness of the post soldering cleaning process employed for PCB assemblies shall be monitored using a sodium chloride (NaCl) equivalent ionic contaminants test in accordance with clause 11.1.4.

NOTE The aim of the monitoring is to demonstrate that the verified cleanliness level is maintained.

ECSS-Q-ST-70-61_1510728

b. Cleanliness monitoring may be omitted for solder assemblies using only pure rosin (ROL0) fluxes as defined in Table 6-2.

ECSS-Q-ST-70-61_1510729

c. For fluxes, other than pure rosin (ROL0), cleanliness testing shall be done in case one or more of the following conditions are met:

1. at maximum intervals of six months,
2. following a change in flux materials,
3. following a change in process parameters,
4. following actions affecting cleanability.

NOTE Statistical control methods can be used to control continuous solvent cleaning processes.

ECSS-Q-ST-70-61_1510730

d. The supplier shall implement and maintain records of test results.

NOTE The records can aid early detection of a trend towards nonconformance.

ECSS-Q-ST-70-61_1510731

e. When a test result is unacceptable, a major NCR shall be issued in accordance with ECSS-Q-ST-10-09.

11.2 Staking and bonding

ECSS-Q-ST-70-61_1510732

a. Adhesive shall be selected in conformance with clause 6.11.

ECSS-Q-ST-70-61_1510733

b. Adhesive shall be mixed and cured in accordance with the manufacturer's recommendations.

ECSS-Q-ST-70-61_1510734

c. The process of mixing and applying the adhesive shall be documented by a written procedure or by configured drawings which define the location of the adhesive, the shape and the spread area.

ECSS-Q-ST-70-61_1510735

d. All PTH components weighing more than 5 g shall be staked.

NOTE 1 Staking and bonding can be applied before or after soldering depending on configuration.

NOTE 2 Staking of heavy components can be omitted when verified.

ECSS-Q-ST-70-61_1510736

e. All SMD weighing more than 5 g should be staked.

NOTE 1 This is to minimize shock and vibration loading on the leads.

NOTE 2 The adhesive compound can be applied either before or after soldering in conformance with the supplier's process identification document.

ECSS-Q-ST-70-61_1510737

f. Staking and bonding shall be performed on clean surfaces.

NOTE Some surfaces can be prepared to enhance the adhesion for instance. by mechanical abrasion.

ECSS-Q-ST-70-61_1510738

g. Staking and bonding shall not be performed on fused tin lead unless the tin lead surface is limited to < 25 % by area of the bonding surface and demonstrated by verification as specified in clause 13.

NOTE Fused tin lead can be locally removed by wicking, using a copper braid.

ECSS-Q-ST-70-61_1510739

h. The adhesive shall not extend onto the solder footprints.

ECSS-Q-ST-70-61_1510740

i. Spread of staking and bonding material onto surrounding areas may be accepted providing the staking and bonding shape is in accordance with the assembly verification.

ECSS-Q-ST-70-61_1510741

j. The adhesive shall not negate the stress relief of the component or terminations.

NOTE Stress relief can be negated if staking is in contact with neighbouring leads

ECSS-Q-ST-70-61_1510742

k. Staking and bonding material shall not be in contact with surrounding components or terminals.

ECSS-Q-ST-70-61_1510743

l. Epoxy staking and bonding material shall not be in contact with glass bodied components.

NOTE It is good practice to use a sleeve between glass body and adhesive material.

11.3 Conformal coating, potting and underfill

ECSS-Q-ST-70-61_1510744

a. Conformal coating shall be selected in conformance with clause 6.11.

ECSS-Q-ST-70-61_1510745

b. Pottings, underfill and conformal coatings shall not negate stress-relief of component leads or connecting wires.

NOTE Underfill can be applied before or after soldering depending on configuration.

ECSS-Q-ST-70-61_1510746

c. Pottings, underfill and conformal coatings shall not have adverse effects upon materials used on the substrate, or components attached thereon.

NOTE This is particularly important at low service temperatures.

ECSS-Q-ST-70-61_1510747

d. The conformal coating shall be applied such that any defect identified in clause 12.3 are prevented.

12
Final inspection

12.1 General

ECSS-Q-ST-70-61_1510748

a. Each soldered connection shall be visually inspected.

NOTE 1 Annex F includes examples of acceptable and unacceptable workmanship for SMDs.

NOTE 2 Annex E includes examples of acceptable and unacceptable workmanship for PTHs.

ECSS-Q-ST-70-61_1510749

b. Components and conductors shall not be physically moved prior or during visual inspection.

ECSS-Q-ST-70-61_1510750

c. The substrate, solder joint, components and component position, shall be inspected in accordance with:

1. clause 10.4 for SMDs,
2. clauses 8.2, 9 and 10.2.6 for PTHs,
3. clause 10.6 for high-voltage connections,
4. clause 10.7 for solderless interconnections.

ECSS-Q-ST-70-61_1510751

d. The assembly shall be visually inspected in two steps with the following methodology:

1. Visual inspection of the assembly is aided by magnification appropriate to the size of the connections between 4x and 10x.
2. Detailed inspection is performed with a minimum magnification 20x.

ECSS-Q-ST-70-61_1510752

e. Additional magnification shall be used to resolve suspected anomalies or defects up to 40x.

ECSS-Q-ST-70-61_1510753

f. X-ray inspection shall be applied when there are hidden solder joints that are not visually accessible.

NOTE X-ray rejection criteria are defined in clause 12.4.

12.2 Visual acceptance criteria

ECSS-Q-ST-70-61_1510754

a. Acceptance criteria for visual inspection shall be as follows:
   1. a clean, smooth satin to bright undisturbed solder joint surface,
   2. solder fillets between conductor and termination areas,
   3. visible contour of wires and leads such that their presence, direction of bend and termination end can be determined,
   4. complete wetting as evidenced by a low contact angle between the solder and the joined surfaces,
   5. acceptable amount and distribution of solder,
   6. absence of any of the defects specified in clause 12.3,
   7. stress relief,
   8. exposed base metal at the ends of cut leads in the soldered connection,
   9. exposed base metal on sides of tracks and soldering pads on substrate,
   10. haloing at PCB edge and non-plated holes in accordance with Table 10-45 of ECSS-Q-ST-70-60,
   11. wire soldered on its entire lap contact.

   NOTE Illustrations of criteria are given in Annex E and Annex F.

12.3 Visual rejection criteria

ECSS-Q-ST-70-61_1510755

a. The following nonconformances shall be cause for rejection:
   1. charred, burned or melted insulation of components,
   2. conductor pattern separation from circuit board,
   3. burns on base materials,
   4. continuous discolouration between two conductor patterns,
   5. excessive solder including peaks, icicles and bridging, see Annex E for PTH components,
   6. contaminated solder joints including flux, lint and extraneous material,
   7. flux residue, solder splatter, solder balls, or other foreign matter on circuitry, beneath components or on adjacent areas,
   8. dewetting,
   9. insufficient solder,
   10. pits, holes or voids,
   11. granular or disturbed solder joints,
   12. fractured or cracked solder connection,

13. cut, nicked, gouged or scraped conductors or conductor pattern,
14. incorrect conductor length,
15. incorrect direction of clinch or lap termination on a PCB,
16. damaged conductor pattern,
17. soldered joints made directly to gold-plated terminals, unless in compliance with requirement 6.9.2b or 7.6.1b,
18. cold solder joints,
19. component body embedded within solder fillet,
20. open solder joints,
21. probe marks present on the soldered joint or on the metallization of chip components caused by electrical testing after assembly,
22. glass seal not in compliance to MIL-STD-883 Method 2009.8,
23. impaired stress relief,
24. measling,
25. delamination,
26. exposed base metal except criteria specified 12.2a.8,
27. cracks detected in glass diodes outside the relevant component procurement standard,
28. bent connector pins outside the relevant component procurement specification,
29. modified component leads shape after assembly even if still within that defined in procurement standard of the item,
30. damage of the lead, component or PCB beyond that defined in the procurement standard of the item,
31. reduced insulation between leads down to unacceptable value as per ECSS-Q-ST-70-12 clause 14.3.2,
32. degraded insulation material of the connector in contact area,
33. bubble or void in the conformal coating or potting that are bridging conductive elements,
34. bubble, void or delamination in conformal coating and potting between high voltage conductors,
35. lack of conformal coating specified on drawing,
36. not specified and continuous adhesive forming a bridge in contact with terminals, component body or solder joints,
37. excessive degolding,
38. insufficient degolding,
39. direct bonding on glass component body with epoxy,
40. separation of adhesive from the contact surface,
41. separation of conformal coating from the surface,
42. presence of cracks in the ceramic of components or cover of component.

43. any FOD trapped into or under conformal coating on circuitry, beneath components or on adjacent areas.

NOTE 1 Example to item 4: measling, delamination, halo effect.

NOTE 2 Example to item 20: tombstoning.

NOTE 3 to item 21: it is good practice to include flying probe testing in the flow of verification when flying probe testing is commonly performed on FM, for acceptance of the probe marks.

NOTE 4 to item 24: the minimum insulation distance can be found in ECSS-Q-ST-70-12 for assessment of measling criticality.

NOTE 5 Examples to item 30:

- End cap metallization peeling cracks in component, missing metallization are examples of damage.
- Cracks in ceramics mainly occur in chip capacitors, and leadless component with thermal plane termination.

12.4 X-ray rejection criteria

ECSS-Q-ST-70-61_1510756

a. The following non-conformances while performing X-ray inspection, with equipment defined in clause 5.5.19, shall be cause for rejection:

1. bridges and other unintended metallic materials,
2. poor or no wetting of the solder,
3. cumulative voids greater than 25 % by area of the solder joint,
4. cumulative voids greater than the maximum allowed for specific applications,
5. a single void which traverses either length or width of the terminal and exceed 10 % of the total area.

NOTE 1 to item 11: Solder balls are a typical example of unintended metallic material.

NOTE 2 to item 2: It can be difficult to assess the wetting in X-ray, but solder joints with deviating shape or amount compared to the neighbouring connections indicate that a closer look is needed.

NOTE 3 to item 3: The amount of voids can be manually estimated from an X-ray image, without exact quantification by image processing.

NOTE 4 to item 4: Specific applications can be RF, thermal dissipation or electrical grounding. The minimum coverage requirement might need

adaptation for these cases based on the specific design.

NOTE 5 to item 4: The amount of voids is highly depending on the PCB footprint design, quality of surface finishes on both PCB and component, as well as the soldering process including solder paste.

NOTE 6 Manual soldering, especially with artificial stand-off can make it difficult to fulfil maximum side overhand and minimum termination contact lengths.

ECSS-Q-ST-70-61_1510757

b. For area array components the criteria and dimensions outside the limits given in Table 10-14 shall be met in addition to the requirements of 12.4a.

ECSS-Q-ST-70-61_1510758

c. Any deviation to requirement 12.4a.3 shall be demonstrated by verification in compliance with requirements from clause 13 and accepted by Approval Authority.

ECSS-Q-ST-70-61_1510759

d. The maximum dose during X-ray inspection shall be less than 5 % of the eligible dose of the most sensitive component according to its specification.

12.5 Warp and twist of populated boards

ECSS-Q-ST-70-61_1510760

a. The PCB assembly shall be supported during handling and transportation in order to avoid any mechanical stress on the assembly or component damage.

NOTE Mechanical support can be provided by spacer or frame.

ECSS-Q-ST-70-61_1510761

b. The PCB shall not be forced during any operation to compensate warp and twist.

NOTE Shims or spacers can be used to accommodate warp and twist during integration.

12.6 Inspection records

ECSS-Q-ST-70-61_1510762

a. The result of the final inspection shall be recorded in the manufacturing traveller.

ECSS-Q-ST-70-61_1510763

b. For wave soldering process, a soldering log as specified in clause 13.2.4 shall be put in place.

13 Verification procedure

13.1 Verification approval procedure

13.1.1 Request for verification

ECSS-Q-ST-70-61_1510764

a. The supplier shall provide the following items to the Approval Authority:
   1. A letter from the supplier signed by the contact person and the quality assurance organization of the supplier describing his experience in assembly and making the request for verification.
   2. A verification programme in compliance with clause 13.1.4.
   3. 1 (one) technology sample in compliance with clause 13.1.2.

ECSS-Q-ST-70-61_1510765

b. In the frame of a project, the supplier shall provide a RFA Part1 (Request for Approval).

13.1.2 Technology sample

13.1.2.1 Description of technology sample

ECSS-Q-ST-70-61_1510766

a. Technology sample shall be made when introducing a new assembly process or new supplier.

ECSS-Q-ST-70-61_1510767

b. The supplier shall provide 1 (one) technology sample of flight representative board showing the Flight assembly process capability with components of typical complexity and illustrated in space quality workmanship standards.

NOTE Examples of solder joints quality according to space industry are presented in Annex F and Annex E.

ECSS-Q-ST-70-61_1510768

c. Technology sample shall include areas with and without conformal coating if used.

ECSS-Q-ST-70-61_1510769

d. The supplier shall provide a listing of the assembly procedures.

ECSS-Q-ST-70-61_1510770

e. Approval Authority may waive the needs of technology sample.

13.1.2.2 Evaluation of technology sample

ECSS-Q-ST-70-61_1510771

a. The technology sample shall be assessed by Approval Authority or by a test house recognized by Approval Authority.

ECSS-Q-ST-70-61_1510772

b. The assessment of the technology sample shall include visual inspection report.

ECSS-Q-ST-70-61_1510773

c. Approval Authority may request microsectioning.

ECSS-Q-ST-70-61_1510774

d. Approval Authority shall inform the supplier on the result of inspection of the technology sample.

ECSS-Q-ST-70-61_1510775

e. After examination, the technology sample examination report shall be sent to the supplier.

ECSS-Q-ST-70-61_1510776

f. Approval Authority shall inform the supplier on acceptance regarding the start of the next stages of the approval process.

13.1.3 Audit of assembly processing

ECSS-Q-ST-70-61_1510777

a. Provided the technology sample specified in 13.1.2 is acceptable, Approval Authority shall audit the assembly facility at a time when the assembly line is in operation.

ECSS-Q-ST-70-61_1510778

b. The findings of the audit shall remain confidential between Approval Authority and the supplier.

ECSS-Q-ST-70-61_1510779

c. The audit of the supplier's assembly line shall be performed prior to the start of a verification programme.

ECSS-Q-ST-70-61_1510780

d. The Approval Authority shall submit to the supplier a copy of the audit report.

NOTE 1 The assembly line audit report is a customer document provided to the supplier and is used as input for the customer to decide if the verification programme can be further implemented.

NOTE 2 An example of audit report template is given in Annex G.

ECSS-Q-ST-70-61_1510781

e. The audit shall also include a further on-site review of the documentation listed in Annex A.2.1.

ECSS-Q-ST-70-61_1510782

f. Assembly line audit shall be conducted every four years by Approval Authority or after any major changes in the manufacturing floor such as new equipment.

13.1.4 Verification programme documentation

ECSS-Q-ST-70-61_1510783

a. A verification programme shall be submitted to the Approval Authority for acceptance prior to the start of assembly verification in accordance with DRD from Annex A.

NOTE Requirement A.2.1b gives possibility to tailor verification programme.

ECSS-Q-ST-70-61_1510784

b. Verification programme shall be in compliance with:

1. clause 13.2 for generic verifications,
2. clause 13.3 for ceramic area array components,
3. clause 13.4 for assembly verification with electrical testing procedure,
4. clause 13.5 for verification with reduced temperature range,
5. clause 13.6 for solderless process.

ECSS-Q-ST-70-61_1510785

c. The schedule of the verification activities shall be provided and updated.

ECSS-Q-ST-70-61_1510786

d. Any nonconformance or major change with reference to the verification plan shall be notified to the Approval Authority within one week.

13.1.5 Verification samples and testing

ECSS-Q-ST-70-61_1510787

a. The PCB material, PCB build-up, interconnections and footprint used for the verification shall be representative of the FM hardware.

ECSS-Q-ST-70-61_1510788

b. Assembled components shall be flight representative with regards to construction, materials and lead finish.

ECSS-Q-ST-70-61_1510789

c. Assembly shall be flight representative including mechanical and thermal configuration.

ECSS-Q-ST-70-61_1510790

d. Surface mount connectors not screwed to the PCB shall be verified in the flight representative configuration.

ECSS-Q-ST-70-61_1510791

e. For surface mount connectors not screwed to the PCB, mating/demating operations, interconnections to other boards and harnesses shall be included in the verification for flight representativity.

ECSS-Q-ST-70-61_1510792

f. For assembly sensitive components, where the failure mode is damage of the component QM grade level components should be used as a minimum.

NOTE The ESA list of assembly sensitive components is regularly updated and published on ESCIES for information, see www.escies.org, Technologies - ESA SMT Verification. ESA-MPSMO-018961.

ECSS-Q-ST-70-61_1510793

g. The components used for the verification shall be listed in the Verification programme documentation, in accordance with the DRD in Annex A.

NOTE It is the responsibility of the company that the soldering method and temperature are compliant with the manufacturer datasheet or technical notes.

ECSS-Q-ST-70-61_1510794

h. Only component types used during the verification programme shall be regarded as approved.

NOTE 1 Approved components are listed in the assembly summary table.

NOTE 2 Component approved by similarity, as per clause 13.8, are not listed in the Assembly Summary Table

ECSS-Q-ST-70-61_1510795

i. The verification samples shall be assembled and tested according to agreed verification programme.

ECSS-Q-ST-70-61_1510796

j. All test conditions shall be compliant with requirements from clause 14.

13.1.6 Final verification review

ECSS-Q-ST-70-61_1510797

a. The verification report shall be in compliance with DRD from Annex B.

ECSS-Q-ST-70-61_1510798

b. The verification report shall be made available to the Approval Authority.

ECSS-Q-ST-70-61_1510799

c. The supplier shall organise with the Approval Authority a final verification review.

NOTE The assembly processes can be reviewed during the meeting to issue the PID. Verification of closure of the actions identified during the audit of the manufacturing line.

13.1.7 Approval status of assembly line

ECSS-Q-ST-70-61_1510800

a. Following the completion of the final verification review, the following documents shall be submitted to the Approval Authority:

1. PID
2. Assembly summary tables.

ECSS-Q-ST-70-61_1510801

b. The assembly summary tables shall be prepared by the supplier according to DRD from Annex D.

ECSS-Q-ST-70-61_1510802

c. In case of changes in assembly line impacting its approval, an audit shall be conducted to re-establish the approval as specified in clause 13.1.3.

NOTE A non-exhaustive list of changes that impact the Approval of the line is given in Table 13-1.

ECSS-Q-ST-70-61_1510803

d. A letter confirming the completion of a successful verification programme shall be sent to the contact person of the supplier from the Approval Authority, with the Assembly summary table in conformance with the DRD of Annex D.

NOTE 1 The letter and the Assembly summary table provide evidence of the verification approval to a third party.

NOTE 2 The approval of verification applies to all space projects from the date of the approval until withdrawal.

ECSS-Q-ST-70-61_1510804

e. Reference to the Assembly summary table number shall be made on each Space project declared processes list.

ECSS-Q-ST-70-61_1510805

f. Assembly verification status of the electronic hardware shall be reviewed during assembly MPCB review.

NOTE A guideline to support MPCB review is: ESA-TECQTM-MO-1931 Issue 3 "Guideline for the review of Approval status of electronics assembly configurations during MPCB".

ECSS-Q-ST-70-61_1510806

g. Except for components covered by requirement 13.1.7j, verification may be omitted for components for which supplier can demonstrate their acceptance through previous verification heritage, listed in their approved summary table.

ECSS-Q-ST-70-61_1510807

h. Assembly sensitive components that have successfully passed the assembly verification in compliance with this standard, and are outside of what is defined in 3.2.2,shall not be considered as assembly sensitive component in the supplier PID.

ECSS-Q-ST-70-61_1510808

i. The supplier shall maintain a list of assembly sensitive components.

ECSS-Q-ST-70-61_1510809

j. Assembly sensitive components listed in the supplier PID shall be submitted to re-verification every four years to monitor the stability of the assembly.

ECSS-Q-ST-70-61_1510810

k. The re-verification of assembly sensitive components specified in the requirement 13.1.7j may be performed on limited verification programme with worst case configuration identified during initial verification provided acceptance of Approval Authority.

NOTE 1 One substrate, one package per component type, three samples per component.

NOTE 2 For leadless components, mechanical testing can be omitted.

NOTE 3 Non-destructive characterization can be proposed as alternative to microsection.

13.1.8 Withdrawal of approval status

ECSS-Q-ST-70-61_1510811

a. The approval status of the supplier shall be withdrawn if any of the following occurs:
   1. Repetitive supply problems and manufacturing defects,
   2. Undeclared changes of items listed in Table 13-1,
   3. Numerous non compliances to the PID.

      NOTE 1 Renewed approval can be granted following a review of the discrepancies.

      NOTE 2 A repeat, or partial repeat of the verification programme can be requested by the Approval Authority.

13.2 Verification programme

13.2.1 General

ECSS-Q-ST-70-61_1510812

a. The approval of mounting and supporting of components, terminals and conductors, as specified in this standard, shall be applicable only to assemblies designed to continuously operate over the mission within the temperature limits of -55 °C to +85 °C at solder joint level.

ECSS-Q-ST-70-61_1510813

b. Compliance to environmental range within -55 °C to +85 °C at solder joint level for the mission shall be stated.

ECSS-Q-ST-70-61_1510814

c. The supplier shall demonstrate verification for each combination of substrate material type, PCB footprint, component type, soldering technique applied, staking and bonding, lead forming configuration, solder mask and conformal coating as used on FM.

   NOTE 1 Material type groups as defined in Table 6-1 of ECSS-Q-ST-70-12.

   NOTE 2 Vapour phase reflow, convection reflow, hot air and hand soldering are examples of different soldering techniques.

ECSS-Q-ST-70-61_1510815

d. Verification of area array components shall be performed in accordance with the requirements in clause 13.3.

ECSS-Q-ST-70-61_1510816

e. Except for area array components which are covered by clause 13.3, verification may be performed with electrical testing procedure in compliance with clause 13.4.

ECSS-Q-ST-70-61_1510817

f. Verification of solderless assemblies shall be performed in compliance with clause 13.6.

ECSS-Q-ST-70-61_1510818

g. Verification programme with reduced temperature range in accordance with clause 13.5 may be applied to reduce risk of failure during thermal cycling due to CTE mismatch between component and PCB.

NOTE 1 Ceramic chip capacitors type II are highly prone to cracks in the ceramic. It has been demonstrated that the type of cracks and length of cracks seen in microsectioning at the top side are directly correlated to the temperature range during thermal cycling as well as the temperature gradient. It is therefore for this type of components recommended to perform verification programme with reduced temperature range from the beginning, not only after a previously failed verification programme.

NOTE 2 For chip capacitors it is good practice to perform the verification on the capacitance value used which has the thinnest cover plate and most densely packed dielectric planes. Cover plate is the distance between external surface. and first electrode.

ECSS-Q-ST-70-61_1510819

h. The verification shall be performed on at least 3 (three) components except for the assembly of sensitive components where 5 (five) components are used per configuration in the verification programme.

ECSS-Q-ST-70-61_1510820

i. When assembly sensitive component is listed in summary table, if the verification was performed with less than 5 (five) components, a new verification shall be performed.

ECSS-Q-ST-70-61_1510821

j. Verification of the assembly shall be performed with a nominal process and a repair process for each component.

NOTE Manual process covers a range of processes such as hand soldering, hot gas station and IR station.

ECSS-Q-ST-70-61_1510822

k. The nominal process shall be representative of the FM manufacturing flow.

NOTE If both collective and non-collective processes are used on FM, verification board is submitted to both processes also in verification.

ECSS-Q-ST-70-61_1510823

l. No rework shall be performed before MIP1 except for manually soldered components.

ECSS-Q-ST-70-61_1510824

m. Rework of components, other than manually soldered, shall be decided during the MIP1

ECSS-Q-ST-70-61_1510825

n. For chip components, more than 20 % of reworked soldered joints per component type and assembly configuration shall not be acceptable.

ECSS-Q-ST-70-61_1510826

o. For all components except those defined in requirement 13.2.1n, more than 10 % of reworked soldered joints per component type and assembly configuration shall not be acceptable.

ECSS-Q-ST-70-61_1510827

p. Reworks outside of what is allowed in 13.2.1m and 13.2.1n may be accepted by Approval Authority.

NOTE Some packages due to their complexity can be more difficult to assemble without any rework.

ECSS-Q-ST-70-61_1510828

q. Any repair or modification, not compliant to ECSS-Q-ST-70-28, shall be submitted to a verification programme as agreed with the Approval Authority.

ECSS-Q-ST-70-61_1510829

r. The supplier's repair process using the nominal manual process including removing and replacing of 1 (one) of each type of mounted component shall be submitted to verification testing with the exception of AAD assembly verification for which a minimum of 2 (two) parts are being repaired.

NOTE The supplier has the option to perform more than 1 (one) repair for each type of component.

ECSS-Q-ST-70-61_1510830

s. For each type of component, per configuration, the repair shall be performed on the largest component.

ECSS-Q-ST-70-61_1510831

t. For repair verification of collective assembled components, the repair shall be performed only on the components being assembled by manual soldering method, provided the same assembly configuration.

NOTE The repair is required on the hand soldering process to keep a sample of 3 (three) or 5 (five) on the collective assembly configuration.

ECSS-Q-ST-70-61_1510832

u. Verification testing of commercial components shall be performed for each lot in conformance with this clause 13.2.1, except when requirement 13.8.1d can be met.

ECSS-Q-ST-70-61_1510833

v. Terminations to be microsectioned shall be connected to the internal PCB layers.

NOTE The terminations to be microsectioned are described in Table 14-5.

ECSS-Q-ST-70-61_1510834

w. The verification sample shall be submitted to 2 (two) nominal soldering method reflows when reflow is performed on both PCB sides of the FM.

NOTE The supplier has the option to flip the board for the second reflow.

ECSS-Q-ST-70-61_1510835

x. The verification programme shall be performed in accordance with Figure 13-1.

ECSS-Q-ST-70-61_1510836

y. A soldering log as specified in clause 13.2.4 shall be put in place for all soldering processes involved in a board manufacturing during verification programme.

ECSS-Q-ST-70-61_1510837

z. The soldering log shall be made available to the Approval Authority.

ECSS-Q-ST-70-61_1510838

aa. The conditions associated with long term storage, extensive ground testing, mechanical stress after launch, high temperature application with or without thermal cycles shall be assessed by the supplier.

ECSS-Q-ST-70-61_1510839

bb. The environmental conditions of the mission including ground testing shall be covered by the environmental conditions of the verification programme.

ECSS-Q-ST-70-61_1510840

cc. For surface mounted components the total number of temperature cycles shall be 500, except for the cases defined in requirement 13.3.3g and requirement 13.4p.

ECSS-Q-ST-70-61_1510841

dd. For components mounted in plated through holes the total number of temperature cycles shall be 200.

ECSS-Q-ST-70-61_1510842

ee. When mechanical bonding is underneath the component, microsectioning of one component may be performed after vibration and 50 thermal cycles to justify the integrity of the bonding.

NOTE The component can be 1 (one), not the one repaired, of the 3 (three) assembled components which were cut out from the same verification board after the 50 thermal cycles.

ECSS-Q-ST-70-61_1510843

ff. Prior to start verification assembly the supplier shall organize a MRR with two weeks notification with the Approval Authority

NOTE 1 The PCB design is reviewed to check compliance with requirements from clause 13.1.5.

NOTE 2 During the review, the Approval Authority can check that the verification programme is approved by all parties and that all actions are closed.

ECSS-Q-ST-70-61_1510844

gg. The supplier shall organise a MIP1 with two weeks notification, with the Approval Authority prior to any conformal coating.

NOTE The Approval Authority can delegate the MIP1 to the supplier.

ECSS-Q-ST-70-61_1510845

hh. Prior to any environmental testing, the supplier shall organise with the Approval Authority a TRR with two weeks notification during which the MIP1 outputs and outstanding actions are reviewed.

NOTE The Approval Authority can delegate the action review to the supplier.

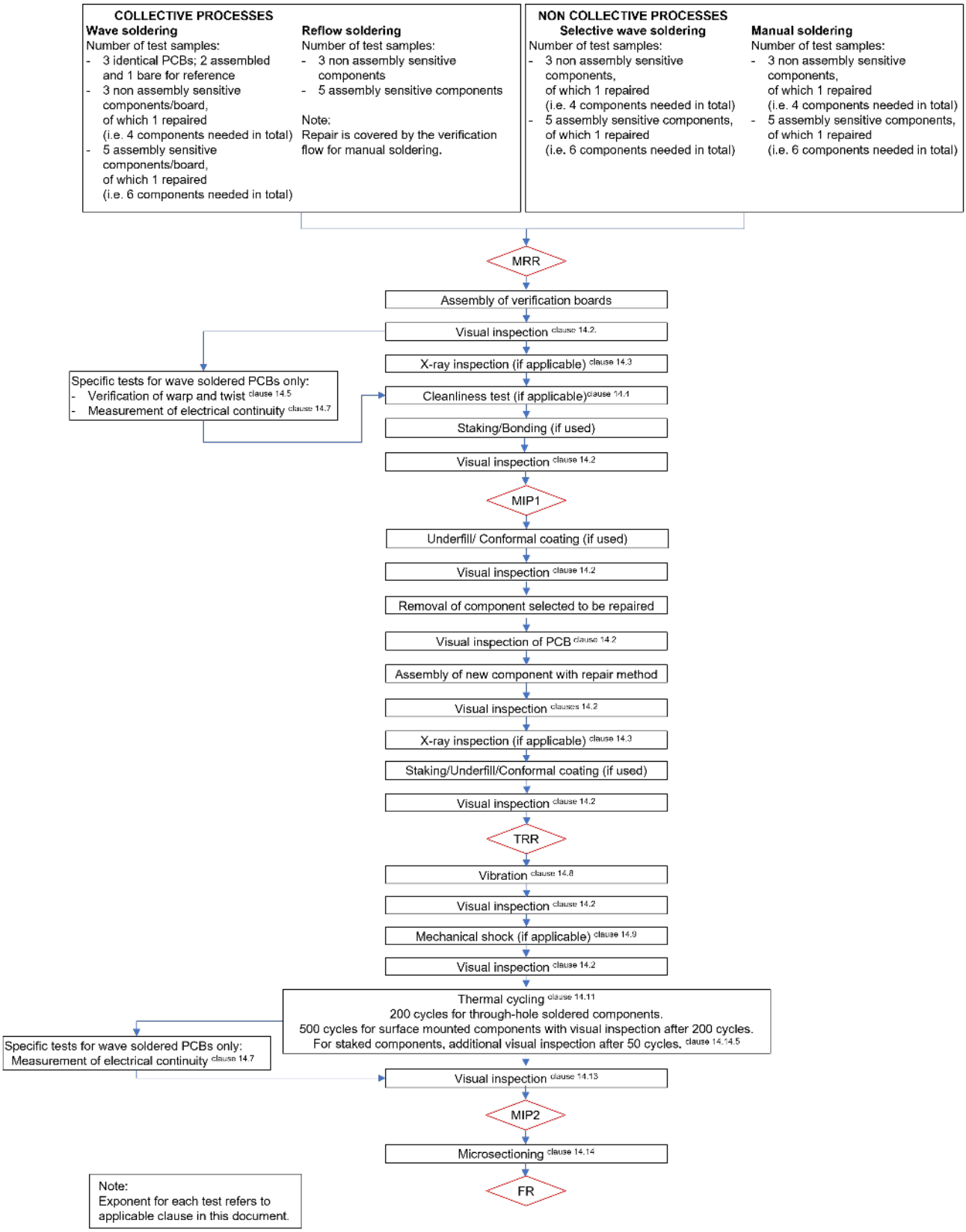
ECSS-Q-ST-70-61_1510846

ii. The supplier shall organise with Approval Authority a MIP2 with two weeks notification at the completion of the environmental test.

NOTE The Approval Authority can delegate the MIP2 to the supplier.

ECSS-Q-ST-70-61_1510847

jj. The supplier shall organize with the Approval Authority a final VR during which the environmental tests results are reviewed.



ECSS-Q-ST-70-61_1510848

Figure 13-1 : Generic soldering verification flow

13.2.2 Verification for PTH manual soldering

ECSS-Q-ST-70-61_1510849

a. Any soldering configuration not covered by requirements from clauses 8.2, 9,10.2.6 and 10.3 or covered but for which assembly verification is requested shall be verified in accordance with clause 13.2.1.

ECSS-Q-ST-70-61_1510850

b. A process specific verification programme shall be performed for through hole component assemblies with stress relief that are not compliant to clause 8.2.

13.2.3 Additional verification for wave soldering

ECSS-Q-ST-70-61_1510851

a. For components that are not assembly sensitive, the supplier shall provide 2 (two) assembled PCBs with at least 3 (three) components of each type per board and 1 (one) non-assembled PCB as reference.

ECSS-Q-ST-70-61_1510852

b. For assembly sensitive components, the supplier shall provide 2 (two) assembled PCBs with at least five components of each type per board and 1 (one) non-assembled PCB as reference.

ECSS-Q-ST-70-61_1510853

c. Each board shall have an identical layout and be from the same batch.

ECSS-Q-ST-70-61_1510854

d. The layout and component density shall be similar to that envisaged for FM boards.

ECSS-Q-ST-70-61_1510855

e. Warp and twist of all assembled PCBs shall be measured for wave soldering verification, according to clause 14.5.

ECSS-Q-ST-70-61_1510856

f. Electrical continuity measurements shall be performed on wave soldered multilayer PCBs according to clause 14.7.

ECSS-Q-ST-70-61_1510857

g. One component of each type per board shall be submitted to repair.

ECSS-Q-ST-70-61_1510858

h. More than 5 % of reworked soldered joints per component shall not be accepted.

13.2.4 Soldering log

ECSS-Q-ST-70-61_1510859

a. The soldering log shall contain as a minimum the following data:
   1. Board identification
   2. Board technology description: materials, build up, ground planes
   3. Soldering process identification
   4. Main parameters for the soldering process
   5. List of identified defects
   6. Number of reworks performed on each solder joint
   7. Calculation of percentage of defects
   8. Inspectors observations
   9. Any miscellaneous remark of interest.

      NOTE An example of a soldering log for a wave process soldering is given in Figure 13-2.

Part identification **Wave soldering parameters** **Assembly: _____ PCB P/N: _____ Preheat temp: _____ Solder temp: _____ Conveyor Speed: _____ Wave height: _____**																				
Description					**Insufficient**						**Excess**					**Miscellaneous**				
MLB ❑ No. of through holes: _____ ❑ No. of layers: _____ Ground plane estimated area: Topside: _____% Botside: _____%				T: component side; B: bottom side	Lead poor wetting	Pad poor wetting	Large voids	Small bottomless voids	Insufficient solder flow-thru	Depressed solder	Bridging	Icicling	Accumulations	Excess solder (lead obscured)	Stress-relief bends filled	Raised component	Other solder discrepancies (specify)			
Acceptable rework level: ___% total	Date	Inspector	Insptn. S/N															Subtotals	% for rework	
Inspector's observations:				T																
				B																
				T																
				B																
Totals:																				

Figure 13-2: Example of soldering log for joints discrepancy log

13.3 Special verification testing for ceramic area array components

13.3.1 General

ECSS-Q-ST-70-61_1510860

a. The assembly verification of ceramic AADs shall be divided in the following 2 (two) steps, as shown in Figure 13-3.
   1. Demonstration of capability in accordance with clause 13.3.2, and
   2. Demonstration of electrical integrity in accordance with clause 13.3.3.

      NOTE 1 Once the capability samples show a satisfactory result the verification of AAD can commence.

      NOTE 2 Capability samples can be excluded from the programme if the supplier can demonstrate previous verification heritage.

ECSS-Q-ST-70-61_1510861

b. The capability and verification samples shall be representative of the FM hardware.

   NOTE For example, PCB build-up and size, mechanical fixation, component packages.

   NOTE It is recommended to have a successful IST test on PCB to avoid failing the assembly verification due to damaged PCB.

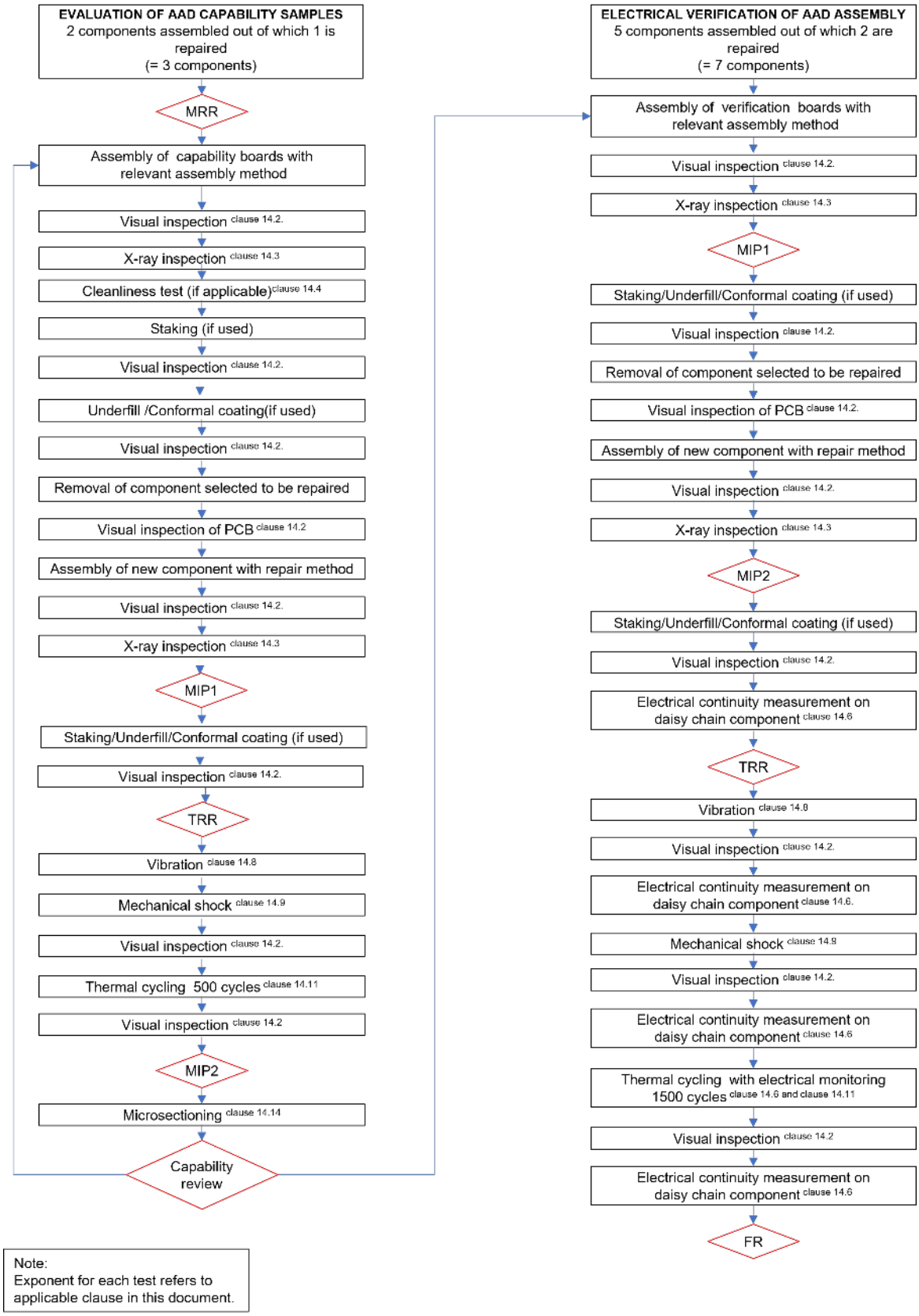
ECSS-Q-ST-70-61_1510862

c. The PCB material, footprint, via technology used for the capability and verification samples shall be the same and interconnection similar as the ones used for the FM hardware.

   NOTE HDI, blind via and buried via are different types of via technologies.

ECSS-Q-ST-70-61_1510863

d. The verification shall be performed with daisy chain components to demonstrate a reliable electrical function of the PCB and the package interface throughout the environmental test campaign.



ECSS-Q-ST-70-61_1510864

Figure 13-3: Area Array component verification programme flow chart

13.3.2 Evaluation of AAD capability samples

ECSS-Q-ST-70-61_1510865

a. The supplier shall manufacture and demonstrate that the 2 (two) capability samples are in conformance with the requirement 13.3.2i before the manufacture of the verification samples using daisy chain components can be initiated.

ECSS-Q-ST-70-61_1510866

b. 2 (two) components shall be assembled with the nominal reflow process.

NOTE The supplier can use daisy chain packages for the capability to have an early results of electrical monitoring during thermal cycles.

ECSS-Q-ST-70-61_1510867

c. One of the components from requirement 13.3.2b shall be removed and replaced with a new component using the repair process.

ECSS-Q-ST-70-61_1510868

d. When nominal and repair processes are identical then the number of components, may be reduced to 1 (one) which is repaired

NOTE The total number of components needed is 2 (two).

ECSS-Q-ST-70-61_1510869

e. The components shall be inspected in conformance with requirements from the clause 10.4.14.

ECSS-Q-ST-70-61_1510870

f. The components shall be submitted to vibration testing in conformance with requirements from the clause 14.7.

ECSS-Q-ST-70-61_1510871

g. The components shall be submitted to shock testing in conformance with clause 14.9.

ECSS-Q-ST-70-61_1510872

h. The components shall be submitted to 500 thermal cycles in conformance with requirements from the clause 14.11.

ECSS-Q-ST-70-61_1510873

i. After environmental tests completion, microsectioning of the components shall be performed to demonstrate PCB integrity in the AAD area with respect to:

1. Damage to the component outside the procurement specification,
2. Damages outside of what is allowed in clause 14.15.3.
3. Damages outside of what is allowed in clause 14.16.

NOTE The purpose of the capability samples is to show that the PCB and the component body are intact after the assembly and repair of AAD and environmental testing (vibration, mechanical shock and 500 temperature cycles). A crack in the columns or balls is not considered as reason for rejection.

13.3.3 Electrical verification of AAD assembly

ECSS-Q-ST-70-61_1510874

a. 5 (five) components shall be assembled for each nominal assembly method and mounting configuration.

ECSS-Q-ST-70-61_1510875

b. 2 (two) of the assembled components shall be removed and replaced with new components using the repair process.

ECSS-Q-ST-70-61_1510876

c. When nominal and repair processes are identical then the number of components, may be reduced to 3 (three) out of which 2 (two) are repaired.

NOTE The total number of components needed is 5 (five).

ECSS-Q-ST-70-61_1510877

d. The components shall be inspected in conformance with requirements from the clause 10.4.14.

ECSS-Q-ST-70-61_1510878

e. The 5 (five) components shall be submitted to vibration testing in conformance with requirements from the clause 14.7.

ECSS-Q-ST-70-61_1510879

f. The 5 (five) components shall be submitted to shock testing in conformance with requirements in clause 14.9.

ECSS-Q-ST-70-61_1510880

g. The 5 (five) components shall be submitted to 1500 thermal cycles with temperature conditions in conformance with clause 14.11 and with continuous electrical monitoring in accordance with clause 14.6.

ECSS-Q-ST-70-61_1510881

h. Resistance measurement shall be done, at ambient, before and after any mechanical testing in accordance with clause 14.6.

ECSS-Q-ST-70-61_1510882

i. After environmental testing the verification samples shall fulfil the acceptance criteria in accordance with clause 14.16.

13.4 Assembly verification with electrical testing procedure

ECSS-Q-ST-70-61_1510883

a. Except for the cases specified in requirement 13.4b the supplier may propose assembly verification with electrical testing procedure as an alternative method.

ECSS-Q-ST-70-61_1510884

b. Leadless chip capacitors and leadless components with plane termination shall not be assembly verified through electrical testing procedure.

NOTE Capacitor and TO276 packages such as SMD05, SMD1, SMD2 and SMD5C, are excluded as the failure mechanism is crack in ceramic.

ECSS-Q-ST-70-61_1510885

c. Assembly verification with electrical testing procedure shall be performed in accordance with Figure 13-4 with samples for both capability verification with microsectioning and with electrical verification.

ECSS-Q-ST-70-61_1510886

d. Verification of capability shall be performed on at least one component except for the assembly sensitive components where 5 (five) components are assembled with nominal process.

ECSS-Q-ST-70-61_1510887

e. One of the components from requirement 13.4d shall be removed and replaced with a new component using the repair process providing the repair process is identical to the nominal assembly.

ECSS-Q-ST-70-61_1510888

f. If the repair procedure is different from the nominal assembly, a separate assembly verification with full number of capability as well as electrical verification samples shall be performed.

ECSS-Q-ST-70-61_1510889

g. Capability samples may be excluded from the programme if capability can be demonstrated through previous verification heritage.

ECSS-Q-ST-70-61_1510890

h. Verification with electrical monitoring shall be performed on at least 32 components assembled for each assembly configuration with nominal process.

NOTE 1 Machine reflow, hand soldering are the examples of assembly method.

NOTE 2 The assembly of the capability and the electrical verification samples can be made on the same board.

ECSS-Q-ST-70-61_1510891

i. One of the components from requirement 13.4h, except for assembly sensitive components where it is 5 (five) components, shall be removed and replaced with new components using the repair process.

ECSS-Q-ST-70-61_1510892

j. All solder terminations shall be continuously electrically monitored throughout the temperature cycling

ECSS-Q-ST-70-61_1510893

k. The electrical value of components for electrical monitoring shall be selected to be able to detect anomalies in the solder joint:

1. for resistor zero ohm or the lowest value in the procurement specification,
2. for other types, custom daisy chain.

ECSS-Q-ST-70-61_1510894

l. In case of non-representative daisy chain component to FM one, the use of functional component may be proposed providing agreement of Approval Authority.

NOTE Example of such components are commercial components.

ECSS-Q-ST-70-61_1510895

m. For the capability samples microsectioning shall be performed in accordance with clause 14.14 after verification steps in accordance with Figure 13-1.

ECSS-Q-ST-70-61_1510896

n. If capability and electrical monitoring samples are on the same board they shall be separated before the microsectioning of the capability samples and before the environmental tests for the samples for electrical monitoring.

ECSS-Q-ST-70-61_1510897

o. The samples for electrical monitoring shall be submitted to vibration testing in conformance with requirements from clause 14.8 and shock testing in conformance with requirements in clause 14.9.

ECSS-Q-ST-70-61_1510898

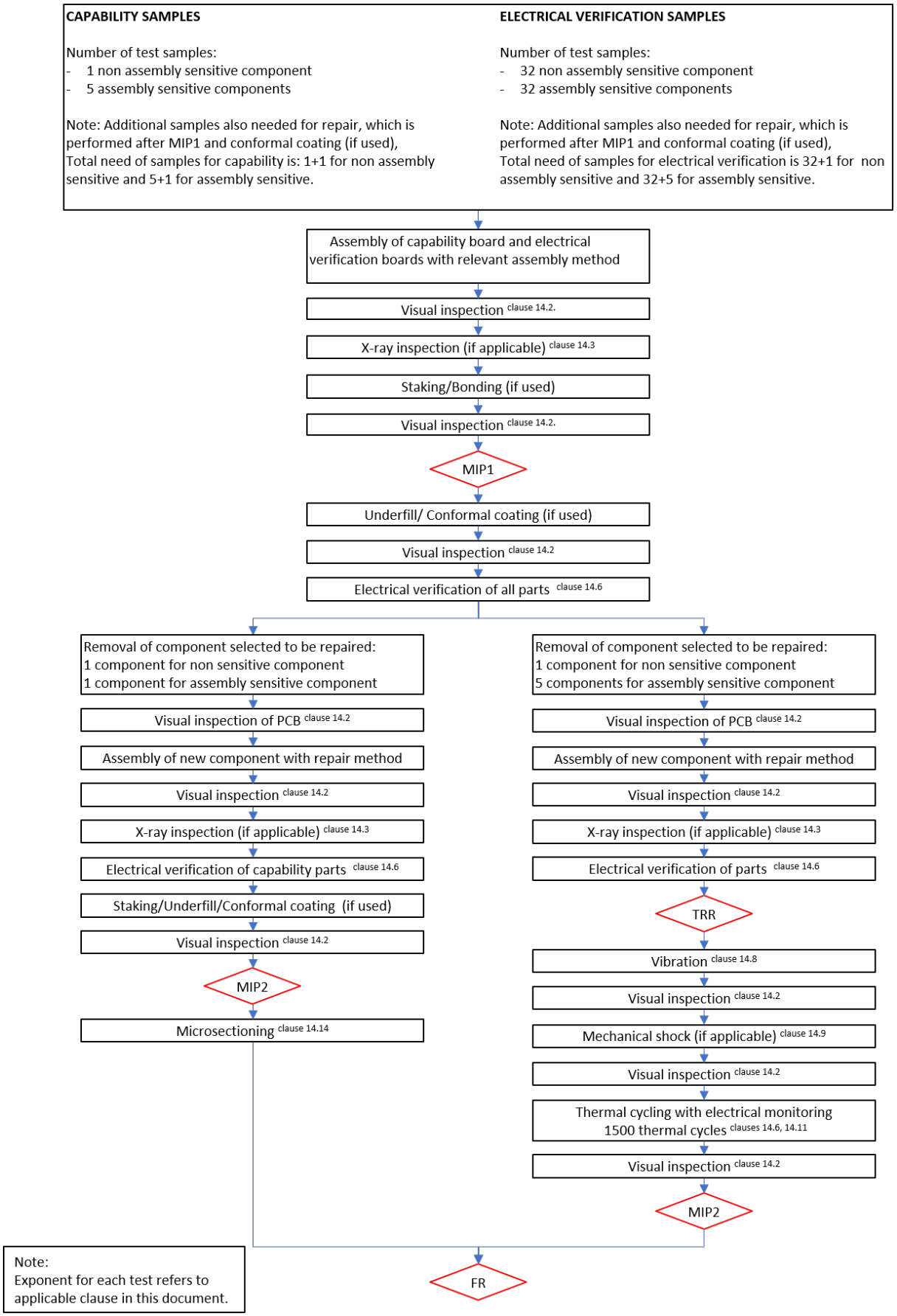
p. The samples for electrical monitoring shall be submitted to 1500 thermal cycles in conformance with requirements in clause 14.11 and with continuous electrical monitoring in accordance with clause 14.6.

ECSS-Q-ST-70-61_1510899

q. Any failed component shall be subjected to failure analysis.

ECSS-Q-ST-70-61_1510900

r. If the first failure occurs before the end of the 1500 thermal cycles, the number of cycles before the first failure shall be identified as the component assembly verification limitation.



ECSS-Q-ST-70-61_1510901

Figure 13-4: Assembly verification with electrical testing procedure

13.5 Verification programme with reduced temperature range

ECSS-Q-ST-70-61_1510902

a. Verification programme with reduced temperature range may be applied to reduce risk of failure during thermal cycling due to CTE mismatch between component and PCB.

NOTE 1 The majority of assembly sensitive components (see definition 3.2.2) has CTE mismatch between components and PCB as root cause of failure. Reduction of the temperature range and the temperature gradient can lower the risk of failure due to such root cause, but the thermal cycling will take a longer time. A case-by-case trade-off based on risk vs leadtime is necessary.

NOTE 2 Ceramic chip capacitors type II are highly prone to cracks in the ceramic. It has been demonstrated that the type of cracks and length of cracks seen in microsectioning at the top side are directly correlated to the temperature range during thermal cycling as well as the temperature gradient. It is therefore for this type of components recommended to perform verification programme with reduced temperature range from the beginning, not only after a previously failed verification programme.

NOTE 3 For ceramic chip capacitors it is good practice to perform the verification on the capacitance value used which has the thinnest cover plate and most densely packed dielectric planes.

NOTE 4 It is good practice to apply verification with reduced temperature range for leadless components with plane termination such as SMD0.5 to reduce the risk of cracks in the ceramic.

ECSS-Q-ST-70-61_1510903

b. Verification programme with reduced temperature range shall follow the generic flow described in Figure 13-1, except for the temperature cycling conditions that are modified in compliance with clause 14.12.

ECSS-Q-ST-70-61_1510904

c. Components that have passed a successful verification with reduced temperature range in compliance with this clause may be added in the assembly summary tables as tailored verification, provided approval by the Approval Authority.

ECSS-Q-ST-70-61_1510905

d. Request for approval shall be submitted in each project where the component with tailored verification is used to justify that the verified temperature range covers the mission in which it is intended to be used.

13.6 Verification for solderless process

ECSS-Q-ST-70-61_1510906

a. The verification of solderless process shall be performed on flight representative assembly configuration in accordance with Figure 13-5.

NOTE Representative assembly configuration includes elements for thermal dissipation configuration.

ECSS-Q-ST-70-61_1510907

b. The verification tests shall be performed to show absence of degradation within the solderless interconnection part, PCB and component during all ground and in-orbit mission.

NOTE Possible degradations can be creeping of the spring, fretting degradation of the contact.

ECSS-Q-ST-70-61_1510908

c. 6 (six) components shall be assembled with the same mechanical configuration as flight model.

ECSS-Q-ST-70-61_1510909

d. Mate/demate number shall permit to cover the application requirement with a margin of 4 in compliance with Table 4-4 of ECSS-E-ST-33-01.

ECSS-Q-ST-70-61_1510910

e. Minimum vibration levels shall be in compliance with requirement 14.8e.

ECSS-Q-ST-70-61_1510911

f. Shock test shall be performed in conformance with requirements from clause 14.9.

ECSS-Q-ST-70-61_1510912

g. Electrical monitoring shall be carried out according to clause 14.6 before and after mate/demate, and during vibration and shock tests, if the equipment is to be functional during launching phases.

ECSS-Q-ST-70-61_1510913

h. The samples for environmental testing shall be submitted to 500 thermal cycles with temperature conditions in conformance with clause 14.11 and with continuous electrical monitoring in accordance with clause 14.6.

ECSS-Q-ST-70-61_1510914

i. Damp heat test shall be performed for all applications in compliance with clause 14.10.

ECSS-Q-ST-70-61_1510915

j. In case of long-term storage application, project specific requirements may apply instead of requirement 13.6i.

ECSS-Q-ST-70-61_1510916

k. Electrical continuity test according to clause 14.6 shall be performed to verify absence of degradation of the connection after damp heat test.

ECSS-Q-ST-70-61_1510917

l. Life test shall be performed in accordance with clause 14.13 and with continuous electrical monitoring in accordance with clause 14.6 to evaluate the spring reliability.

ECSS-Q-ST-70-61_1510918

m. Life test may be omitted provided representative test were performed by the component manufacturer.

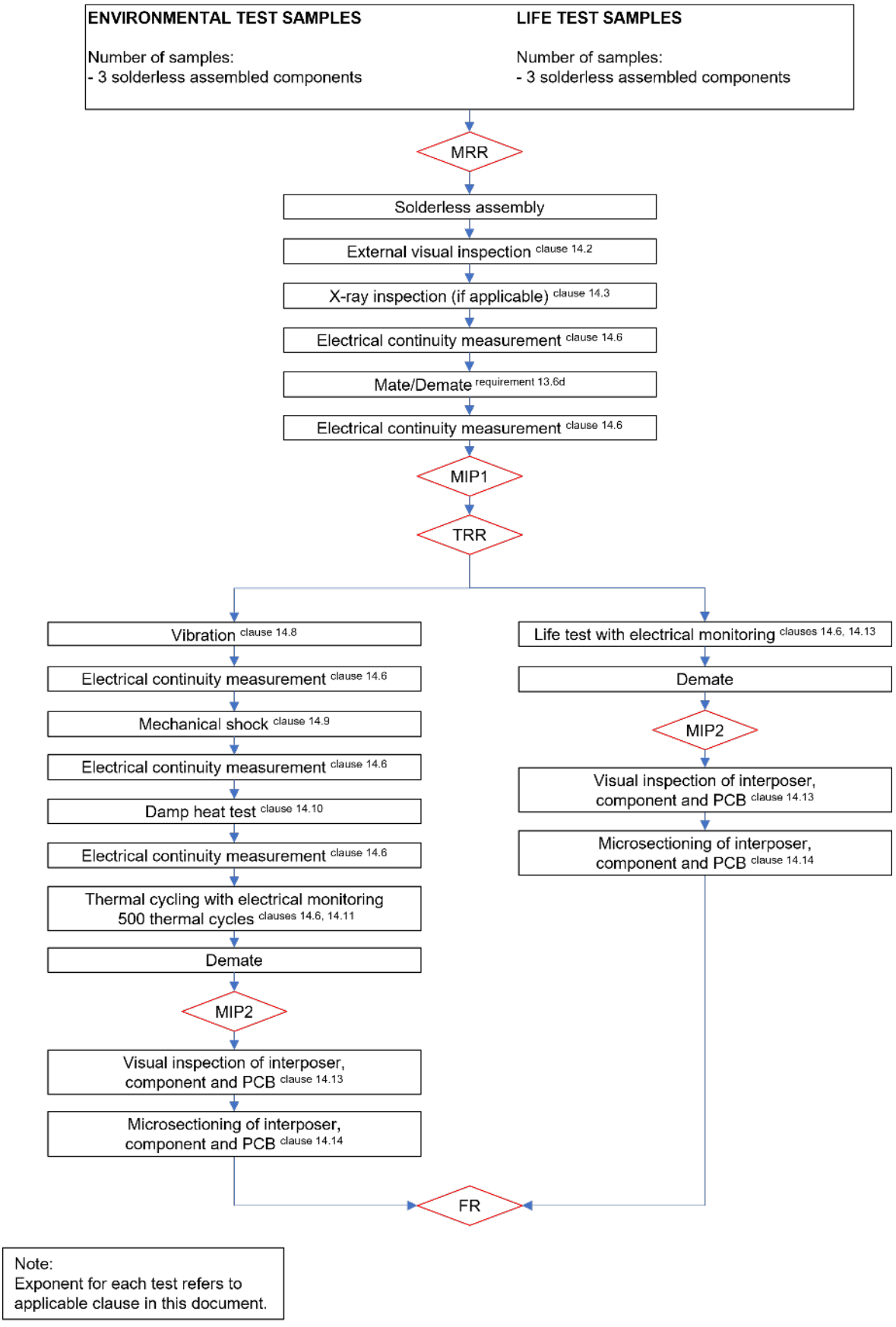
ECSS-Q-ST-70-61_1510919

n. Visual inspection criteria in compliance with clause 12 shall apply to interposer, component and PCB.

ECSS-Q-ST-70-61_1510920

o. Microsections of interposer, component and PCB shall be done according to clause 14.15 in order to verify absence of plating damage at interposer level, component damage and laminate cracks or plating damage in the PCB.

NOTE Microsectioning can be performed after dismounting of the assembly.



ECSS-Q-ST-70-61_1510921

Figure 13-5: Verification procedure for solderless technology

13.7 Conditions for delta verification

ECSS-Q-ST-70-61_1510922

a. The supplier shall undertake a verification for any new configuration not covered by similarity rules in accordance with requirements from clause 13.8.

ECSS-Q-ST-70-61_1510923

b. The delta verification shall be performed when changes are undertaken as specified in Table 13-1.

ECSS-Q-ST-70-61_1510924

c. For a process delta verification program, the number of samples may be tailored from the general requirements from clause 13.2, depending on the type of process changes made, subject to approval by the Approval Authority.

NOTE 1 The selection criteria are based on worst cases depending on the change of process to be verified.

NOTE 2 For PCB materials change, examples of worst cases are CTE mismatch, thermal dissipation, stiffness, glass transition temperature and copper peel strength.

ECSS-Q-ST-70-61_1510925

d. For delta verification associated with process change the verification boards shall be designed such that they are representative of the new process.

ECSS-Q-ST-70-61_1510926

e. A delta-verification programme in accordance with the DRD from Annex A shall be submitted for approval to the Approval Authority.

Table 13-1: Conditions invoking verification

Examples of changes	Cleanliness and solvent compatibility tests (see clause 11.1)	Limited verification without environmental tests	Full verification with environmental tests (see clauses 13.2, 13.3, 13.4, 13.5 or 13.6)
New component mounting configuration (for example, change of staking, bonding or coating material)			X
New component size not covered by conditions for similarity			X
New PCB material type (for example, polyimide vs. epoxy)			X
New PCB surface finish			X
New solder paste without change of alloy, powder size distribution or flux activation type	X	X With microsections	
New solder paste with new alloy, flux activation type and/or different physical and chemical characteristics	X		X
New flux activation type for manual soldering	X	X With microsections	
New cleaning solvent or cleaning process	X		
New reflow profile [1]			X
New solder paste deposition, or reflow equipment without process change		X With microsections	
New component placing equipment of same process method		X Visual inspection only	
New solder paste depositing process			X
New reflow equipment with process change			X
New conformal coating application process or equipment (without material or thickness change)		X With microsections	
Move of manufacturing location outside the clean room specified in the PID		X With microsections	

[1] The reflow profile is considered identical when the duration of the pre-heating, ramp of flux activation phase, peak temperature and time above solder liquidus, ramp of cooling phase can be repeated between different types of PCBs.

13.8 Verification by similarity

13.8.1 General conditions for similarity

ECSS-Q-ST-70-61_1510928

a. Verification by similarity shall not be declared successful unless all the following conditions are met:

1. Same substrate material type,
2. Same solder mask,
3. Same PCB finish,
4. PCB footprint designed with same aspect ratios and same via technology of interconnection,
5. Representative PCB build up
6. Same solder material,
7. Same flux
8. Same solder process, and
9. Same staking, bonding and conformal coating configuration.

NOTE 1 to item 1: Material type groups as defined in Table 6-1 of ECSS-Q-ST-70-12.

NOTE 2 to item 1: Similarity for different materials belonging to the same type group is reviewed during assembly MPCB.

NOTE 3 to item 1: See clause 13.7 for delta verification conditions, requirements and possible tailoring.

NOTE 4 to item 4: Blind via in pads and microvias are different technologies of interconnection.

ECSS-Q-ST-70-61_1510929

b. Different solder masks may be used providing a risk assessment for the affected components.

NOTE Examples of factors to consider are materials, thickness, locations, if bonding or staking, compatibility with cleaning solvents.

ECSS-Q-ST-70-61_1510930

c. Verification by similarity shall not apply to commercial components.

ECSS-Q-ST-70-61_1510931

d. Verification by similarity between different lots of commercial components may only be valid if a constructional analysis of the component is performed and confirms no changes in its construction.

13.8.2 Conditions for similarity for PTH components

ECSS-Q-ST-70-61_1510932

a. Verification by similarity for PTH components requiring assembly verification, shall only be applied when all the following conditions are met:
   1. Components are smaller than the verified Lmax, Wmax and Hmax,
   2. Construction of the component is identical to that verified,
   3. Assembly configuration is the same,
   4. Materials are identical,
   5. Lead material is the same,
   6. Lead section is the same, and
   7. Pitch is smaller than the one verified
   8. Evidence that the PCB is not damaged for assembly with the same or smaller pitch.

      NOTE Absence of PCB damage can be demonstrated by successful verification on a different component with same small pitch

ECSS-Q-ST-70-61_1510933

b. Verification by similarity for a PTH shall be declared successful when the PCB thickness is thicker or equal to the one verified.

   NOTE The calculation of the crack should be re assessed taking into account the FM PCB thickness.

13.8.3 Conditions for similarity for SMD

ECSS-Q-ST-70-61_1510934

a. Verification by similarity shall not apply to leadless castellated ceramic chip carrier components, ceramic resistor arrays or no-lead Quad Flat Packs.

ECSS-Q-ST-70-61_1510935

b. Verification by similarity for leaded packages, described in 10.4.7, 10.4.10, 10.4.11 and 10.4.13 shall only be applied when all the following conditions are met:
   1. Package is smaller than the verified Lmax, Wmax and Hmax,
   2. Package weight is lower than the maximum verified,
   3. Lead pitch, nominal thickness, nominal width, and materials composition are identical,
   4. Coated lead finishes on the termination are identical,
   5. Bending dimensions and shape are identical,
   6. Packages are constructed from the same materials.
   7. When existing, the bottom termination or exposed pad has the same aspect ratio to the component body as the one verified.

NOTE 1 to item 2: Radiation shielded packages are heavier than standard flatpack and not covered by similarity.

NOTE 2 to item 6: Glass to metal sealed, glass sealed side-brazed, top-brazed, and bottom-brazed packages are different families.

NOTE 3 to item 6: Dual side pin arrangements are different to quad side pin families.

ECSS-Q-ST-70-61_1510936

c. For flat pack components, described in 10.4.10, verification by similarity may apply even if the lead materials are different.

NOTE Kovar and Alloy 42 leads are considered similar.

ECSS-Q-ST-70-61_1510937

d. Verification by similarity for end-capped and end-metallized components with rectangular body, described in 10.4.2, shall only be applied when all the following conditions are met:

1. Component length is between Lmin and Lmax of the verified component,
2. Component width is between Wmin and Wmax of the verified component,
3. Component height is less than Hmax of the verified component,
4. Ceramic material type is identical,
5. Metallization of the termination and the barrier layers on components are identical, and
6. Component manufacturer is identical.

NOTE 1 to item 1 and 2: For example, 0402 - 2220 does not qualify 1825 as the width is outside the max 20 verified.

NOTE 2 to item 4: Ceramic chip capacitors can be very sensitive to mounting conditions and generally, type I chip capacitors are less sensitive than type II. The sensitivity is design and process related and can therefore vary from one manufacturer to another. Within a manufacturer type II range one or more different ceramic materials can also be used. It is therefore impossible to apply similarity rules between type I and type II ceramic chip capacitors and different manufacturers. Lower capacitance values are less sensitive than higher, based on the increased ratio between electrode layers and ceramic material. It is therefore good practice to select the highest capacitance values in a class or type I or type II ceramic capacitors range to be submitted to assembly verification.

NOTE 3 to item 4: Examples of ceramic types are NPO, Z5U and Y7R.

NOTE 4 to item 5: Flexible and non-flexible terminations are not identical.

NOTE 5 to item 5: termination platings Sn60 and Sn63 are equivalent and different from Sn85 which in turn is equivalent with Sn95.

ECSS-Q-ST-70-61_1510938

e. For leadless chip resistors, described in 10.4.2, thick film resistors may be verified by similarity to thin film resistors provided that the supplier has successfully performed a full verification programme according to clause 13.2 for at least one thin film resistor technology, covering the dimensions, termination plating and the type of material, in accordance with requirements 13.8.3d.1, 2, 3, 5.

ECSS-Q-ST-70-61_1510939

f. Verification by similarity for thermistors and fuses described in 10.4.2, for MELF resistors and MELF diodes in 10.4.3, for leadless chip inductors in 10.4.4, and L-Shape inwards components in 10.4.5, shall only be applied when all the following conditions are met

1. Component length is less than Lmax of the verified component,
2. Component width is less than Wmax of the verified component,
3. Component height is less than Hmax of the verified component,
4. Material type is identical,
5. Package shape is identical and
6. Metallization of the termination and the barrier layers on components are identical.

ECSS-Q-ST-70-61_1510940

g. For components with inward formed L-shaped leads, described in 10.4.5, verification by similarity may apply even if the lead materials are different.

NOTE Tantalum leaded capacitors can have copper alloy or Alloy 42 leads for which impact is considered negligible.

ECSS-Q-ST-70-61_1510941

h. Verification by similarity for leadless component with plane termination according to clause 10.4.6 shall only be applied when all the following conditions are met

1. Components are smaller than the verified L_{max} , W_{max} and H_{max}
2. Construction of the component package is identical to the verified component package, and
3. Materials are identical.

NOTE to item 2: SMD0.2 exists in 2 versions which are not identical.

ECSS-Q-ST-70-61_1510942

i. Verification by similarity for components with ribbon terminals without stress relief, according to clause 10.4.12, shall only be applied when all the following conditions are met

1. Package is smaller than the Lmax, Wmax and Hmax of the verified component,
2. Package weight is lower than the maximum weight of the verified component,
3. Lead nominal thickness, nominal width and materials composition are identical to the verified component,
4. Lead finishes on the termination are identical to the verified component,
5. Bending dimensions and shape are identical to the verified component,
6. Packages are constructed from the same materials.

ECSS-Q-ST-70-61_1510943

j. Verification by similarity for area array components, described in 10.4.14, shall only be applied when all the following conditions are met

1. Package is smaller than the Lmax, Wmax and Hmax of the verified component,
2. Package weight is lower than the maximum weight of the verified component,
3. Number of columns is lower than the one of the verified components,
4. Column pitch is the same,
5. Column dimensions are the same,
6. Column distribution are the same,
7. Column materials are the same,
8. Column construction is the same,
9. Column manufacturer is the same,
10. Column attachment process is the same,
11. Package has the same construction and materials, and
12. Package has the same body shape (aspect ratio).

13.8.4 Conditions for similarity for solderless components

ECSS-Q-ST-70-61_1510944

a. Verification by similarity for solderless assembly described in 10.7, shall only be applied when all the following conditions are met

1. Component and interposer lengths are less than Lmax of the verified component and interposer,
2. Component and interposer widths are less than Wmax of the verified component and interposer,

3. Interposer has the same height as the verified interposer,
4. Component weight is lower than the verified component,
5. Number of terminations is lower than the verified component,
6. Pitch is the same as the verified component,
7. Materials for both component and interposer are the same as the verified component,
8. Component and interposer finishes are the same as the ones verified,
9. Manufacturer and technology for the interposer are the same as the one verified,
10. Mechanical construction and mounting principle are the same as the one verified and,
11. Component and interposer have the same body shape (aspect ratio).

NOTE to item 7 and 8: In case the interposer connects two PCBs, the component requirements refer to the PCBs.

14 Environmental tests conditions

14.1 Overview

Whenever a test is referred in this document, test conditions are described in the following clauses.

14.2 Visual inspection

ECSS-Q-ST-70-61_1510945

a. Visual inspection shall be performed on each of the verification boards according to clauses 12.1, 12.2 and 12.3.

NOTE For leadless ceramic components with plane terminations such as SMD0.5, it is good practice to add intermediate visual inspection point to identify when any crack in the ceramic occurs.. The aim is to cover the ground testing thermal cycles.

14.3 X-ray inspection

ECSS-Q-ST-70-61_1510946

a. X-ray inspection shall be performed when required according to clauses 8, 10 and 13.

NOTE X-ray inspection is used for hidden solder joints, for example for bottom terminated components, soldered exposed pads and area array components.

14.4 Cleanliness test

ECSS-Q-ST-70-61_1510947

a. The supplier shall perform cleanliness verification according to clause 11.1.2.

14.5 Warp and twist of PCB

ECSS-Q-ST-70-61_1510948

a. Warp and twist of PCB shall be performed as part of the verification programme for wave soldering according to clause 13.2.3.

ECSS-Q-ST-70-61_1510949

b. Warp and twist shall be measured on each of the verification boards and recorded in accordance with clause 9.3.3.2 and 9.3.3.3 of ECSS-Q-ST-70-60.

NOTE Warp and twist control is part of the verification flow for wave soldered components.

14.6 Electrical continuity measurement

ECSS-Q-ST-70-61_1510950

a. Electrical continuity measurement in accordance with this clause shall be performed as part of the following verification programmes:

1. ceramic area array components according to clause 13.3,
2. assembly verification with electrical testing procedure according to clause 13.4, or
3. verification of solderless process according to clause 13.6.

NOTE See clause 14.7 for electrical continuity measurements for wave soldered multilayer PCBs

ECSS-Q-ST-70-61_1510951

b. Electrical continuity shall be measured with a daisy chained component including 100 % of the component connections.

NOTE It is good practice to add test points whenever possible for failure investigation.

ECSS-Q-ST-70-61_1510952

c. For AAD resistance measurement at ambient temperature shall be done after assembly, before and after any mechanical testing.

ECSS-Q-ST-70-61_1510953

d. Continuous electrical monitoring of daisy chain shall be performed during the thermal cycling.

NOTE 1: The number of thermal cycles for each verification is defined in the respective clause for each type of verification programme.

NOTE 2: Alternative electrical monitoring methods can be agreed with the Approval Authority.

ECSS-Q-ST-70-61_1510954

e. The sampling time for the continuous electrical monitoring shall be maximum 10 s.

ECSS-Q-ST-70-61_1510955

f. No interrupts in the electrical monitoring shall be detected throughout the thermal cycles.

ECSS-Q-ST-70-61_1510956

g. The maximum increase of each individual daisy chain resistance after the full number of thermal cycles shall not be more than 10 % compared to the initial resistance recorded during the first 5 (five) cycles.

ECSS-Q-ST-70-61_1510957

h. The supplier may provide their own criteria for an electrical failure to Approval Authority for approval.

14.7 Electrical continuity for wave soldered multilayers PCB

ECSS-Q-ST-70-61_1510958

a. Electrical continuity measurements shall be performed as part of the verification programme for wave soldering on multilayer PCBs according to clause 13.2.3.

ECSS-Q-ST-70-61_1510959

b. Electrical continuity shall be measured on at least 25 % of all holes.

ECSS-Q-ST-70-61_1510960

c. The electrical continuity measurement shall include at least one internal connection per hole.

ECSS-Q-ST-70-61_1510961

d. Initial resistance measurement shall be performed at ambient temperature.

ECSS-Q-ST-70-61_1510962

e. Electrical continuity measurements shall be performed by continuous electrical monitoring of the daisy chain resistance during the first 5 (five) thermal cycles and the last 10 (ten) thermal cycles.

ECSS-Q-ST-70-61_1510963

f. The maximum increase of each individual daisy chain resistance after the full number of thermal cycles shall not be more than 5 % compared to the initial resistance measured in requirements 14.7d.and 14.7e.

ECSS-Q-ST-70-61_1510964

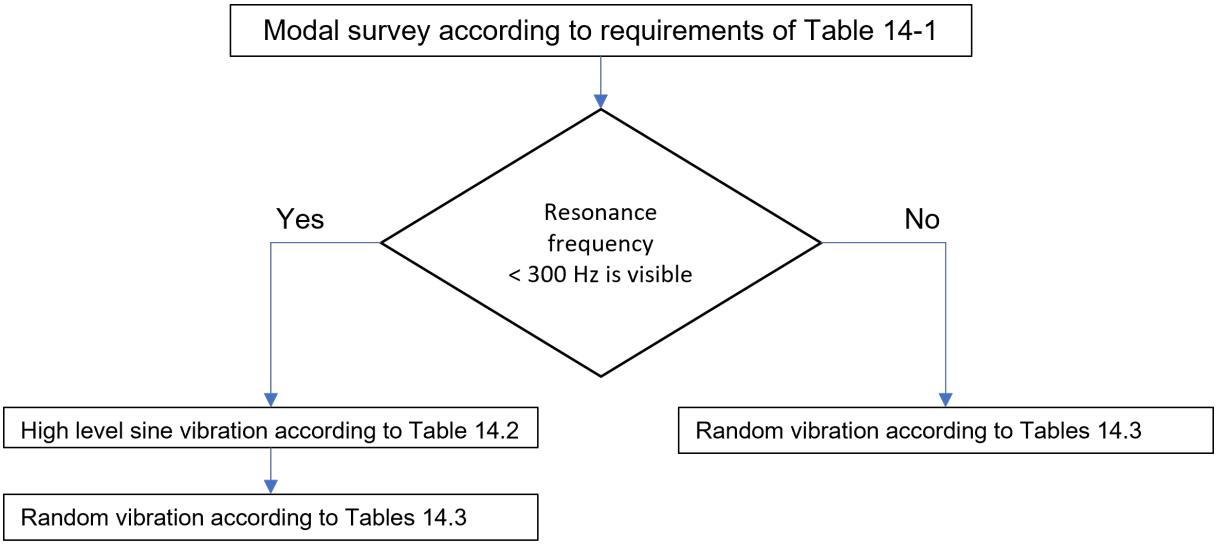
g. Electrical continuity measurements for multilayer boards with positive changes greater than 10 % shall be recorded as failed in the verification report.

14.8 Vibration

ECSS-Q-ST-70-61_1510965

a. The test specimen shall be vibration tested according to test flow chart described in Figure 14-1.

NOTE Vibration testing methodology - From the input levels required by the projects in progress, the maximum deformation of the printed circuit board at the part level is established for each configuration (component type, location on the printed circuit board).



ECSS-Q-ST-70-61_1510966

Figure 14-1:Vibration test flow chart

ECSS-Q-ST-70-61_1510967

b. The PCB design and mechanical mounting including fittings such as stiffeners, frames or spacers shall be representative of the flight model.

ECSS-Q-ST-70-61_1510968

c. The mechanical mounting configuration of the PCB for the vibration tests shall be identified.

ECSS-Q-ST-70-61_1510969

d. In order to take into account test samples imperfections, notching may be used to reduce non-representative mechanical over stresses provided that the following two conditions are met:

1. Notching is justified to the Approval Authority, and
2. Internal notching is identified in the vibration test report.

ECSS-Q-ST-70-61_1510970

e. Minimum vibration levels shall be as specified in Table 14-1, Table 14-2 and Table 14-3.

ECSS-Q-ST-70-61_1510971

f. The vibration levels and duration during verification shall fulfil the project requirements

ECSS-Q-ST-70-61_1510972

g. A modal survey shall be performed to detect any primary resonance frequency.

NOTE 1 Modal survey can be done with sine or random vibration

NOTE 2 It is a good practice, for generic applications, that the verification board exhibits a primary resonant frequency in the range of 500 Hz - 800 Hz.

ECSS-Q-ST-70-61_1510973

h. For sine modal survey, the conditions shall be as defined in Table 14-1a.

ECSS-Q-ST-70-61_1510974

i. For random modal survey, the conditions shall be as defined in Table 14-1b.

ECSS-Q-ST-70-61_1510975

j. High level sine vibration may be omitted, provided that the resonance frequency is above 300 Hz for both the verification board and flight model

ECSS-Q-ST-70-61_1510976

k. Transfer function shall be issued from modal survey and presented to customer.

ECSS-Q-ST-70-61_1510977

l. Input vibration levels shall be measured at the interface between the vibration plate and the PCB.

ECSS-Q-ST-70-61_1510978

m. The response acceleration of the assembled PCB shall be monitored and recorded during testing.

ECSS-Q-ST-70-61_1510979

n. The accelerometers shall be placed on the PCB as well as on the base plate to determine the acceleration of the PCB.

NOTE It is a good practice to mount the accelerometers on the PCB area of largest deflection.

ECSS-Q-ST-70-61_1510980

o. Vibration testing shall be performed in the three orthogonal axes: one out-of-plane and two in-plane.

ECSS-Q-ST-70-61_1510981

p. The severity of the vibration test shall not be less than that shown in Table 14-2 and Table 14-3.

ECSS-Q-ST-70-61_1510982

Table 14-1: Modal survey conditions

Table 14-1a - Sine survey		Table 14-1b - Random survey	
Amplitude	0,5 g (zero to peak)	Range (Hz)	Level
Frequency range	10 Hz to 2000 Hz	10 Hz- 2000 Hz	$5{,}10^{-4}$ g^2/Hz
Sweep rate	2 octaves/minute	Global levels: 1 g r.m.s.	
Direction	X, Y and Z axis	X, Y and Z axis	1 min/axis
		Frequency sampling = 2 Hz	

ECSS-Q-ST-70-61_1510983

Table 14-2: Minimum severity for sine vibration testing

	Axis	Frequency range [Hz]	PSD level (zero to peak)	Sweep rate [oct/min]
Spacecraft	All	25 - 100	25 g	1
		100 - 200	15 g	1
	Duration: 1 cycle up from 25 Hz to 200 Hz			
Launchers	All	10 - 16	10 mm	1/3
		16 - 60	10 g	1/3
		60 - 70	22,5 g	1/3
		70 - 200	22,5 g	2
		200 - 2000	10 g	2
	Duration: 1 cycle up from 10 Hz to 2000 Hz			

ECSS-Q-ST-70-61_1510984

Table 14-3: Minimum severity for random vibration testing

	Axis	Frequency range [Hz]	PSD level	Global level [g r.m.s.]
Spacecraft	Parallel to PCB	20 - 100	+ 6 dB/oct.	27,1 g r.m.s.
		100 - 800	0,5 g^2/Hz	
		800 - 2000	- 3 dB/oct.	
	Perpendicular to PCB	20 - 100	+ 6 dB/oct.	28,5 g r.m.s.
		100 - 500	1,0 g^2/Hz	
		500 - 2000	- 6 dB/oct.	
	Duration: 5 minutes per axis			
Launchers	All	20 - 60	+ 3 dB/oct.	20,0 g r.m.s.
		60 - 1000	0,27 g^2/Hz	
		1000 - 2000	- 6 dB/oct.	
	Duration: 5 minutes per axis			

14.9 Mechanical shock

ECSS-Q-ST-70-61_1510985

a. Mechanical shock test shall be performed in assembly verification for area array components in accordance with requirements in clause 13.3, for solderless assemblies in accordance with requirements in clause 13.6 and for the following components:

1. Relay
2. Quartz
3. Magnetic components (RM)
4. Transformer and self
5. Hybrid
6. Tantalum capacitor
7. Heavy or large component
8. Optical components
9. Low insertion force DIP socket
10. Semiconductors (IC) components, Hybrid components, relays, capacitors with cavities

NOTE The list of components is taken from Table 17-1 of ECSS-E-HB-32-25A (14July2015) that is reproduced in this Standard as Table 14-4.

ECSS-Q-ST-70-61_1510986

b. For components listed in requirement 14.9a, assembly verification shall be made with functional testing to be capable to identify degradation due to shock tests.

ECSS-Q-ST-70-61_1510987

c. The levels and duration of the shock shall be provided in the verification report.

ECSS-Q-ST-70-61_1510988

d. The mechanical shock levels shall be set to meet the intended mission with margin.

ECSS-Q-ST-70-61_1510989

e. Mechanical shock may be omitted if it can be demonstrated that the design has robust margin or proven heritage.

Table 14-4: Shock sensitive electronic components vs. failure modes (Table reproduced from ECSS-E-HB-32-25A)

Electronic components	Failure modes			
	Mode 1	Mode 2	Mode 3	Remarks
Relay	Bouncing	Temporary or permanent transfer	Non reversible mechanical damage	
Quartz	Relief of residual stress in the quartz ⇒ frequency shift that can be temporary during the shock application or definitive	Solder overstress or adhesive crack at clip interfaces	Broken crystal	Quartz are usually mounted on a damping material
Magnetic components (RM) Transformer and self	Crack initiation in ferrite	Electrical lead wire rupture		The internal part is fragile, in particular if the component is composed of ferrite or ceramic
Hybrid	Adhesive rupture at substrate level or other small part level (getter, absorber)	Crack in glass feed-thru	Packaging or lid structural failure	Packaging is often made of brittle material Particles in hybrids are detected by a PIND test
Tantalum capacitor	Bending of the PCB leading reversible electrical peak of current due to local destruction of the dielectric	Bending of the PCB leading to internal over-stresses with non-reversible total destruction by short circuit - Avalanche phenomenon	Tantalum capacitor can also be of large dimensions, hence with same failure modes as for heavy/large components	
Heavy or large component	For heavy components (> 5 gr), overstress at the attachment due to loads, e.g. capacitor, transformer, shielded components …	For large components, overstress at the attachment due to PCB bending		
Optical components	Fibre optic pigtail cleavage	Damaged fibre surface in connectors		
Low insertion force DIP socket	Disjunction of the component			
Semiconductors (IC) components, Hybrid components, relays, capacitors with cavities	Dislodging of mobile particle			Particles are detected by a PIND test

14.10 Damp heat test

ECSS-Q-ST-70-61_1510990

a. Damp heat test shall be performed as part of the verification programme for solderless processes according to clause 13.6.

ECSS-Q-ST-70-61_1510991

b. Damp heat test conditions shall be (93 ± 3) % at (40 ± 3) °C for 240 hours in compliance with the Annex C of ECSS-Q-ST-70-14.

14.11 Temperature cycling test

ECSS-Q-ST-70-61_1510992

a. The test specimen shall be temperature cycled in an air circulating or inert gas purged chamber.

ECSS-Q-ST-70-61_1510993

b. Before the start of the temperature cycling, the test specimen shall be baked out to remove the internal humidity according to clause 7.3.

ECSS-Q-ST-70-61_1510994

c. The bake-out may be part of the first temperature cycle.

ECSS-Q-ST-70-61_1510995

d. The temperature cycling shall be between –55 (-5/+0) °C and +100 (-0/+5) °C.

ECSS-Q-ST-70-61_1510996

e. The first temperature cycle shall be hot.

ECSS-Q-ST-70-61_1510997

f. The rate of temperature change during the temperature cycle shall not exceed 10 °C per minute.

NOTE Higher ramp rates reduce the stresses in the solder joint but increase the stresses within the ceramic materials.

ECSS-Q-ST-70-61_1510998

g. The soak time at each temperature extreme shall be a minimum of 15 minutes.

ECSS-Q-ST-70-61_1510999

h. The monitoring thermocouple shall be attached to the surface of the printed circuit board.

ECSS-Q-ST-70-61_1511000

i. The number of thermal cycles shall be in accordance with:

1. clause 13.2 for general verification programme,

2. clause 13.3 for assembly verification of ceramic area array components,
3. clause 13.4 for assembly verification with electrical testing procedure,
4. clause 13.5 for verification programme with reduced temperature range, and
5. clause 13.6 for verification for solderless components.

NOTE The number of thermal cycles can be higher for SMD, PTH or AAD, based on specific mission requirements.

14.12 Temperature cycling test with reduced temperature range

ECSS-Q-ST-70-61_1511001

a. Temperature cycling with reduced temperature range shall be performed as part of the special verification programme in accordance with requirements in clause 13.5.

ECSS-Q-ST-70-61_1511002

b. The stresses during temperature cycling may be reduced by modification of the temperature cycling conditions as follows:

1. Decreasing the thermal range during temperature cycling by increasing the minimum temperature from the nominal one, or
2. decreasing the thermal range during temperature cycling by decreasing the maximum temperature from the nominal one, or
3. decreasing the temperature cycling gradient from the nominal one, or
4. any combination of 1 to 3 above.

NOTE The modifications refer to changes from the nominal temperature cycling conditions as described in requirements 14.11d and 14.11f.

ECSS-Q-ST-70-61_1511003

c. The temperature cycling may be performed in several steps, with different conditions in the different steps.

NOTE A typical stepwise temperature cycling test is to perform the cycling in 2 steps as follows:

- Step 1: Temperature range tailored so that the minimum and maximum temperature on board level during the on-ground qualification conditions are covered including the minimum and maximum temperatures during cold start, non-operating and operating, as required for the intended mission. Number of cycles in this step tailored such that the on-ground qualification conditions are covered at least with a safety margin of 2.
  The lower temperatures often result in largest

stresses, and it is therefore good practice to cover cold start conditions in this first step so that the number of cycles at the larger temperature range are minimized.

Example: 20 cycles between -40°C/+85°C with a gradient of 2°C/min and a dwell time of 15 minutes corresponds to 15,5 cycles of -55°C/+100°C with a gradient of 10°C/min as calculated with the equation in requirement 14.12g.

- Step 2: Temperature range tailored so that the minimum and maximum temperature on board level during the in-orbit conditions are covered. Number of cycles in this step tailored such that steps 1 and 2 in total correspond to the nominal temperature cycling range that is required for the type of components being verified, typically 500 cycles, when re-calculated with the modified Coffin-Manson (Norris-Landzberg) equation.

  Example: 981 cycles between -10/+100°C with a gradient of 10°C/min or slightly lower and 15 minutes of dwell time. 981 such cycles correspond to 484,8 cycles -55/+100°C with gradient ~10°C/min, as calculated with the equation in requirement 14.12g.

  Thus the cycling during step 1 and step 2 in total covers the full 500 cycles (15,5 + 484,8 = 500,3) required for surface mounted components as required by requirement 13.2.1cc.

NOTE 2 The reason behind dividing the temperature cycling in different steps is to decrease the risk of thermally overstressing the assembly while not prolonging the schedule more than necessary.

NOTE 3 It is recommended to perform the tailoring of the temperature cycling such that the envelope of all intended mission requirements can be covered. A case-by-case trade-off between cost, schedule and risk is though often needed.

ECSS-Q-ST-70-61_1511004

d. The total number of cycles shall be tailored such that all the steps in total correspond to the nominal number of thermal cycles with nominal temperature cycling range that is required for the type of components being verified.

ECSS-Q-ST-70-61_1511005

e. The temperature conditions during temperature cycling shall cover the minimum and maximum board temperatures seen by the component in the intended mission profile including on ground qualification testing.

ECSS-Q-ST-70-61_1511006

f. The corresponding number of thermal cycles for the on-ground qualification and in-orbit environment shall be covered at least with a safety margin of 2.

NOTE Temperature on board level are taken into account during all the on-ground qualification conditions including the minimum and maximum temperatures during cold start, non-operating and operating, as required for the intended missions.

ECSS-Q-ST-70-61_1511007

g. The modified Coffin-Manson (Norris-Landzberg) equation used for the calculation of the equivalent thermal cycles shall be the following:

$$AF = \left[\frac{\Delta T_{lab}}{\Delta T_{field}}\right]^{1.9} \cdot \left(\frac{f_{field}}{f_{lab}}\right)^{1/3} \cdot exp\left(1414 \cdot \left\{\frac{1}{T_{max\_field}} - \frac{1}{T_{max\_lab}}\right\}\right)$$

where:

AF = Acceleration factor between lab and field conditions

T_{max} and T_{min} = Maximum and minimum temperatures [Kelvin]

ΔT = Temperature difference between T_{max} and T_{min}

f = Frequency of the cycling when considering each plateau and the gradients [cycles/24h]

NOTE The coefficients specified are valid for soldering with SnPb solder only.

14.13 Life test

ECSS-Q-ST-70-61_1511008

a. Life test shall be performed as part of the assembly verification for solderless components in accordance with requirements in clause 13.6.

ECSS-Q-ST-70-61_1511009

b. Life test conditions shall be 2000 hours at 125 °C or at maximal operational temperature during flight mission.

14.14 Final visual inspection

ECSS-Q-ST-70-61_1511010

a. Visual inspection of each verification sample shall be made using the list of nonconformance criteria of clause 12.3.

ECSS-Q-ST-70-61_1511011

b. Prior to microsectioning, the components shall be in conformance with the dimensional and solder fillet requirements of clause 8,clause 9 and clause 10.

ECSS-Q-ST-70-61_1511012

c. Any identified nonconformance during the visual inspection specified in 14.14a, before any aging test, shall lead to rejection of the verification sample.

ECSS-Q-ST-70-61_1511013

d. Any identified nonconformance during the visual inspection specified in 14.14a, after any aging test, shall be recorded in the traveller sheet of the verification sample.

ECSS-Q-ST-70-61_1511014

e. In the case of visual failures, an analysis shall be performed to identify if the failure results from the component or the assembly process.

ECSS-Q-ST-70-61_1511015

f. The identified nonconformances of 14.14d should be classified in acceptable or unacceptable depending on performed test flow.

NOTE After the environmental test campaign, some defects are acceptable. For example disturbed solder joints are typical after verification programme and are acceptable provided that the microsectioning acceptance criteria are fulfilled. In case of visible cracks in the solder joints, it is difficult to know the crack length from external visual inspection only. Cracks in solder joints can therefore be acceptable provided that the microsectioning acceptance criteria are fulfilled.

ECSS-Q-ST-70-61_1511016

g. The nonconformances identified in 14.14b and 14.14d shall be notified to the Approval Authority within one week.

14.15 Microsection

14.15.1 Microsection facilities

ECSS-Q-ST-70-61_1511017

a. The Approval Authority shall make available a list of laboratories available to perform microsection.

NOTE The list of available laboratories is on ESCIES website, see www.escies.org, Technologies - ESA SMT Verification: ESA-TECMSP-MO-013165 “ESA recommended microsectioning facilities”.

ECSS-Q-ST-70-61_1511018

b. Microsections shall be performed by a laboratory specified in 14.15.1a except the case specified in the requirement 14.15.1c.

ECSS-Q-ST-70-61_1511019

c. When in-house or other non-listed microsection facilities are used, the supplier shall demonstrate the following:

1. the capability of the laboratory on representative samples including chip components, LCCs and FPs as well as conformal coating.
2. a report with associated microsections sent to the Approval Authority for review and assessment of quality of microsectioning.

NOTE In accordance with ESA memo ESA-TECMSP-MO-013161. See www.escies.org, Technologies - ESA SMT Verification.

14.15.2 Microsections location

ECSS-Q-ST-70-61_1511020

a. At least one microsection shall be made per assembly configuration after environmental testing on each type of component, size and assembly processes and soldering processes.

NOTE 1 Different soldering processes and different staking, bonding or conformal coating are examples of different configurations.

NOTE 2 Successive polishing planes can be performed.

ECSS-Q-ST-70-61_1511021

b. Microsectioning of repaired sample shall cover the manually soldered assembly, provided the same configuration.

ECSS-Q-ST-70-61_1511022

c. The microsection shall be done on the component having the worst solder joint appearance as identified at MIP2.

ECSS-Q-ST-70-61_1511023

d. For assembly sensitive components, 5 (five) components shall be microsectioned per assembly configuration.

ECSS-Q-ST-70-61_1511024

e. Additional microsections may be requested by the Approval Authority in case of cracks or other features detected during the first microsection sampling..

ECSS-Q-ST-70-61_1511025

f. Adhesive bonding for thermal or mechanical purpose underneath a component shall be microsectioned.

ECSS-Q-ST-70-61_1511026

g. The microsections of the component shall be done as specified in Table 14-5.

14.15.3 Microsection acceptance criteria

14.15.3.1 General

ECSS-Q-ST-70-61_1511027

a. The integrity of the assembly shall be assessed by microsectioning.

NOTE Integrity covers PCB, solder joints, adhesives and packages.

ECSS-Q-ST-70-61_1511028

b. After microsectioning, the microsections shall be in compliance with requirements of Table 14-5.

ECSS-Q-ST-70-61_1511029

c. The microsection shall be inspected with a magnification of 50x to 200x except the case specified in the requirement 14.15.3.1d

ECSS-Q-ST-70-61_1511030

d. The microsection for components with small stand-off should be inspected with magnification up to 500x.

NOTE Examples of small stand-off components are LCCs, chip resistors and capacitors, QFN.

ECSS-Q-ST-70-61_1511031

e. In case the microsection shows a crack more than 75 % of acceptable crack, the component type shall be classified as assembly sensitive.

ECSS-Q-ST-70-61_1511032

f. If the component type is classified as assembly sensitive, according to requirement 14.15.3.1e, all remaining components from verification boards shall be microsectioned in order to confirm that acceptance criteria are still fulfilled.

NOTE For a first verification of a new component not identified as assembly sensitive, 3 components are sufficient.

ECSS-Q-ST-70-61_1511033

g. The Approval Authority shall have access to the moulded microsection and pictures.

ECSS-Q-ST-70-61_1511034

h. The verification board and associated microsections shall be stored for a period of at least ten years.

NOTE 1 It is good practice to store the boards until end of mission.

NOTE 2 Boards can assist the analysis of in-orbit failures.

14.15.3.2 Acceptance criteria

ECSS-Q-ST-70-61_1511035

a. Cracks in the solder joint outside of the critical zone shall be accepted.

ECSS-Q-ST-70-61_1511036

b. Cracks in the mechanical bonding shall not be accepted.

ECSS-Q-ST-70-61_1511037

c. Cracks in the mechanical bonding may be accepted provided that the criteria defined in Table 14-5 are met and accepted by Approval Authority.

ECSS-Q-ST-70-61_1511038

d. Cracks in the mechanical staking shall not be accepted.

ECSS-Q-ST-70-61_1511039

e. Cracks in the mechanical staking may be accepted provided that one of the following items are met:

   1. at completion of verification the criteria defined in Table 14-5 are met and accepted by Approval Authority.
   2. after vibration and a minimum of 50 thermal cycles, visual inspection show absence of cracks in the staking and photos of staking are provided.

ECSS-Q-ST-70-61_1511040

f. Cracks in the thermal bonding shall not be accepted.

ECSS-Q-ST-70-61_1511041

g. Cracks in the thermal bonding may be accepted at the completion of the verification testing when they are perpendicular to PCB surface plane.

ECSS-Q-ST-70-61_1511042

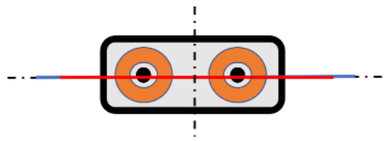
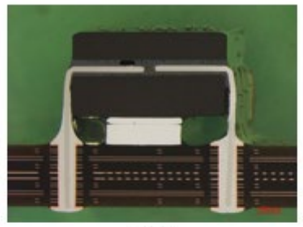
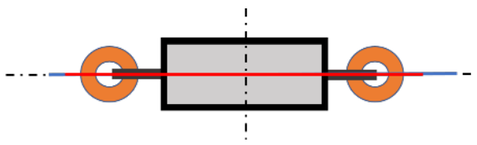
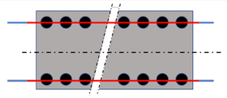
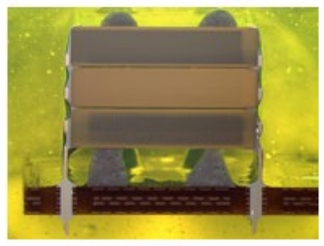
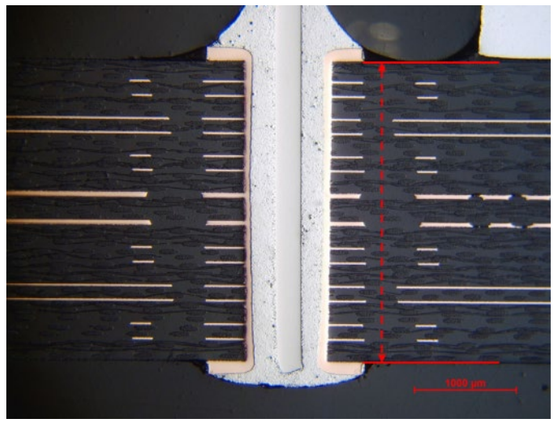
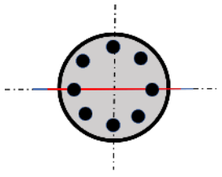
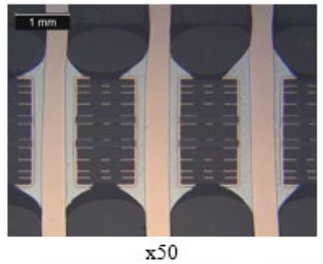
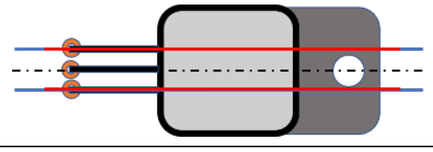
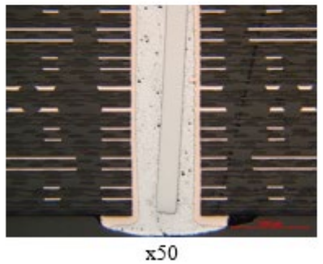
h. Any damage to the component beyond the ones acceptable by the component datasheet shall be identified as a verification failure.

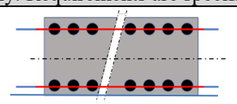
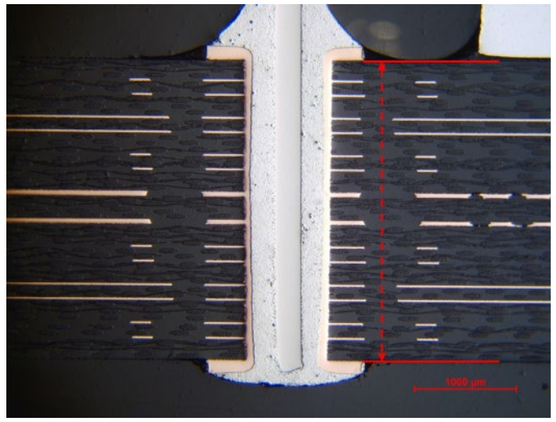
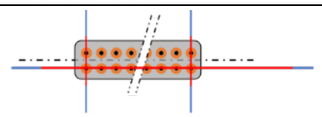
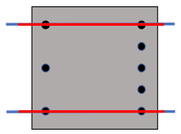
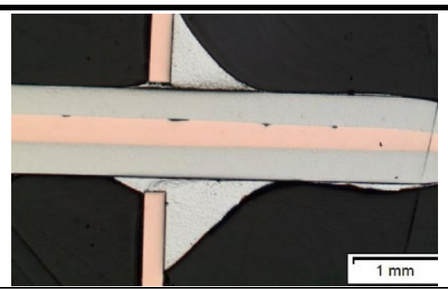
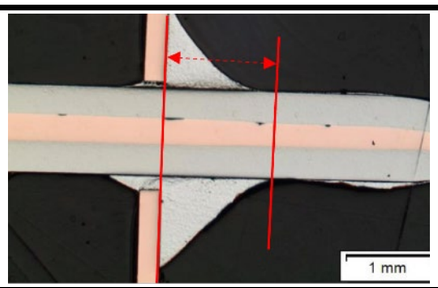
ECSS-Q-ST-70-61_1511043

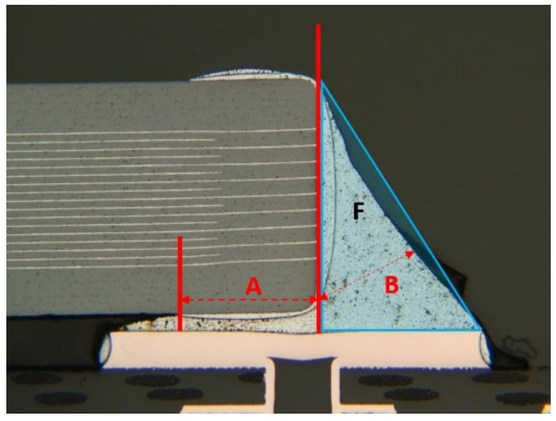
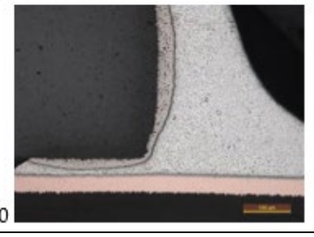
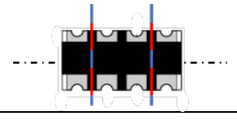
i. Damages outside of what is allowed in the component data sheet may be acceptable providing acceptance of Approval Authority.

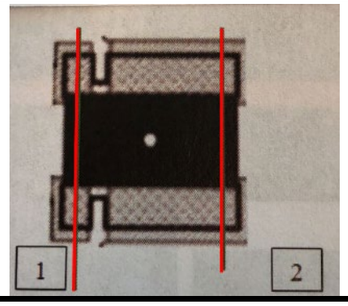
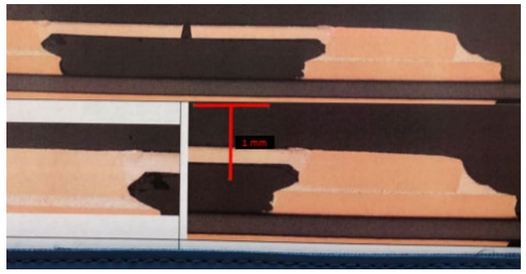
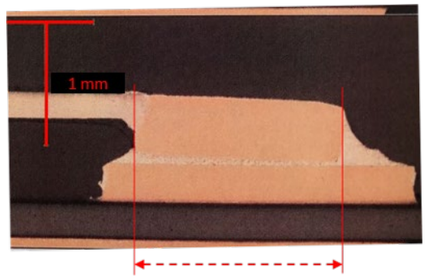
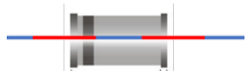
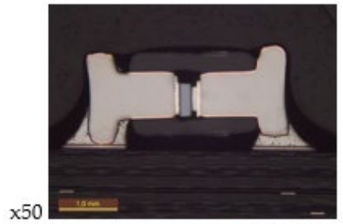
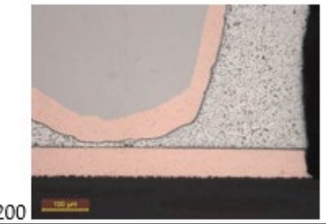
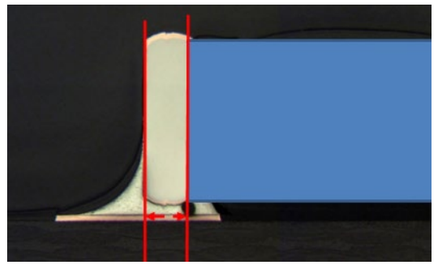
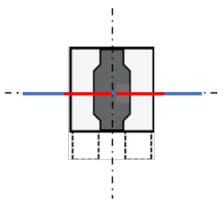
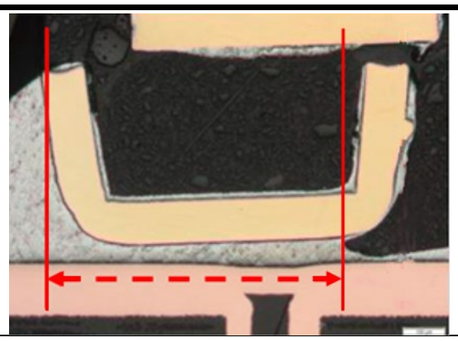
ECSS-Q-ST-70-61_1511044

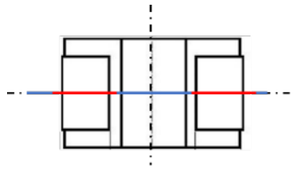
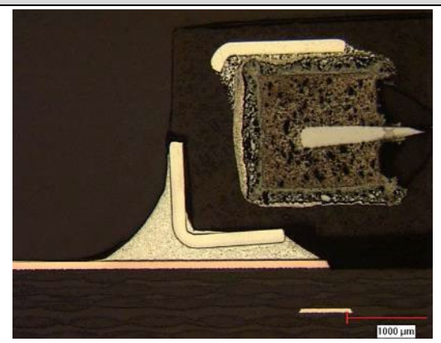
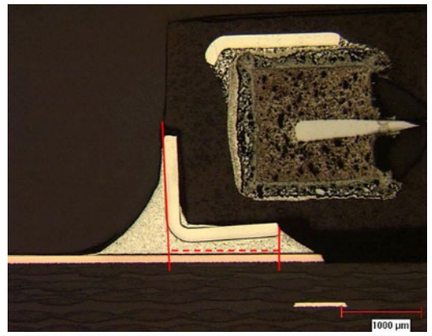
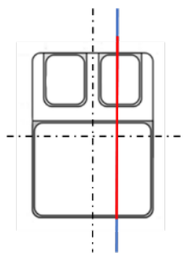
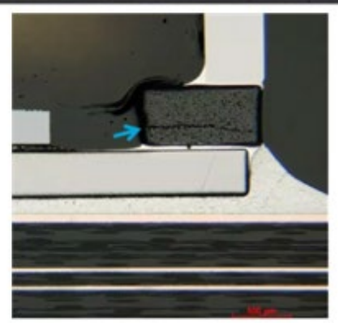
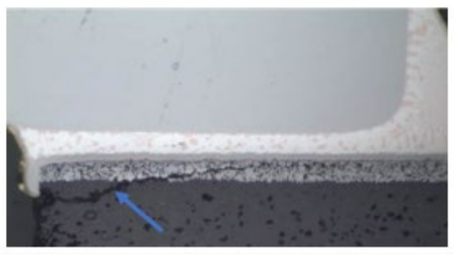
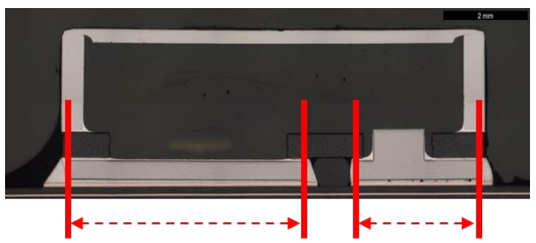
Table 14-5: Component microsection location and acceptance criteria

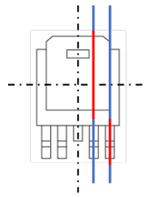
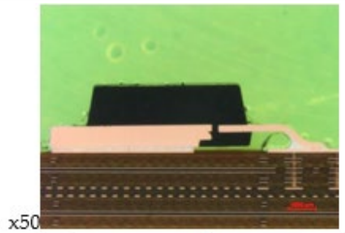
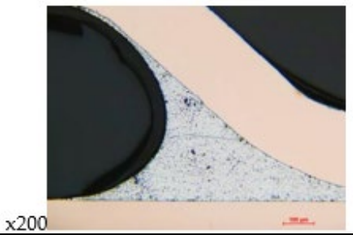
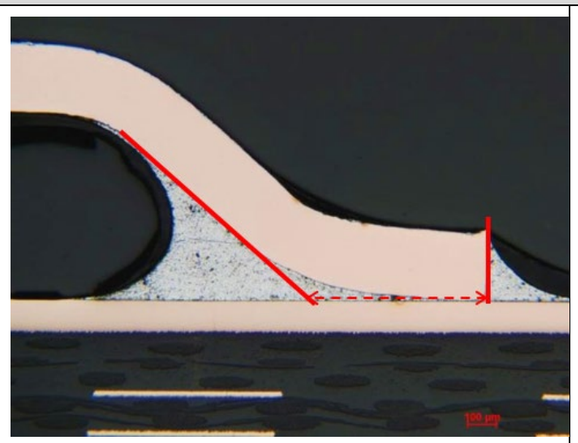
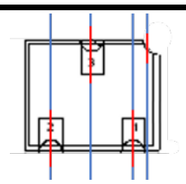
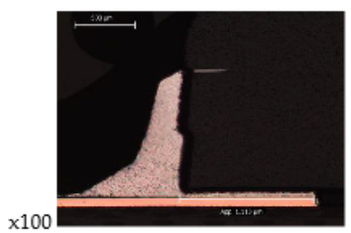
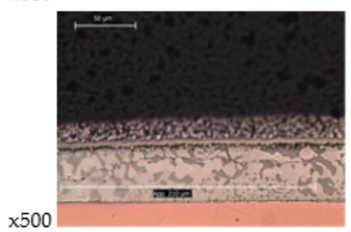
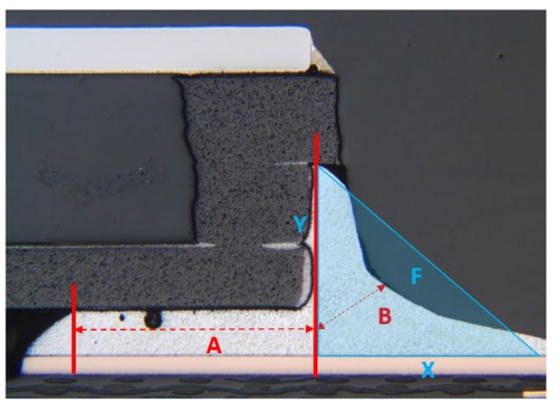
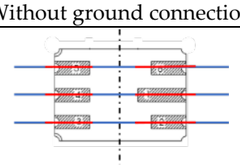
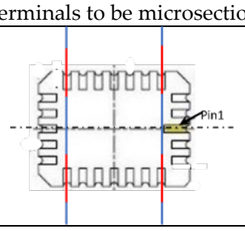
Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
Images in the table are informative examples only. Requirements are specified in text.					
Radial component	CKR capacitors		 x20		
Axial components	CH capacitors CNC capacitors RWR resistors				
Stacked capacitors	-	 1 component is necessary: - parallel to the component axis for repair process on both sides	 x25		The total sum of cracks in the solder joint is less than 25% of critical zone length
TO package component	TO39	 Microsection in the largest distance between two leads	 x50		
TO package component with metal tab	TO254	 This package generally contains BeO that can be considered as hazardous for microsectioning. The microsectioning plane might need to be redefined after discussion with the microsectioning laboratory and asses possible health and safety issues.	 x50		

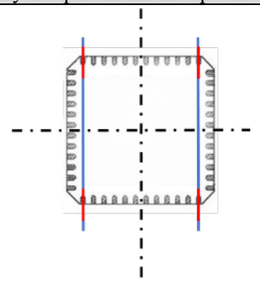
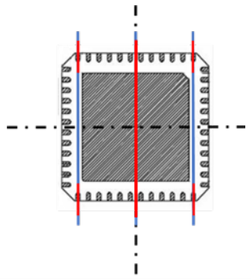
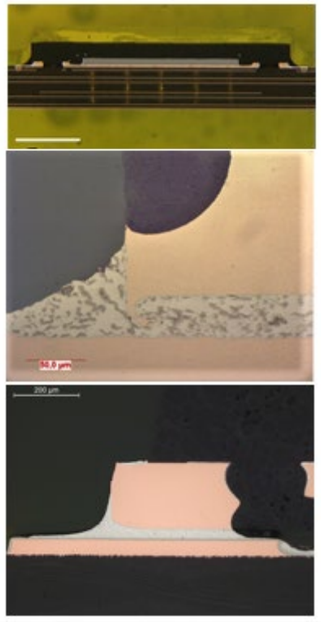
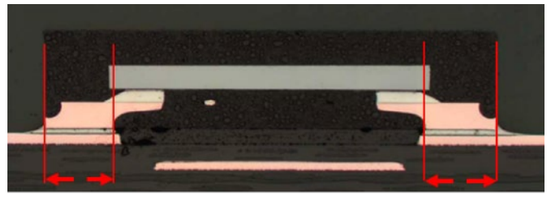
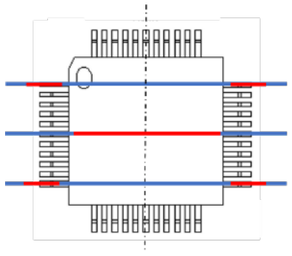
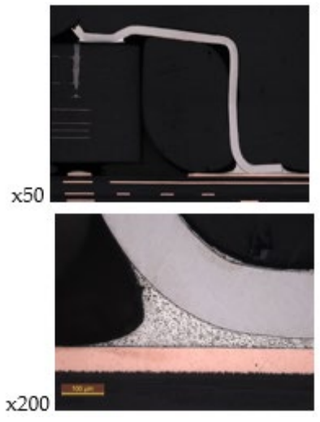
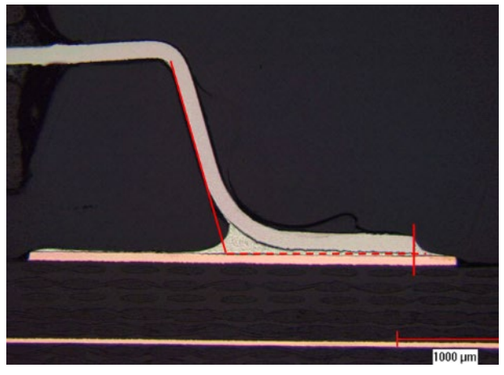
Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
Images in the table are informative examples only. Requirements are specified in text.					
Dual in Line Package (DIL or DIP)	Side brazed DIP>24 pins	 1 component is necessary: - parallel to the component axis for repair process on both sides	-		The total sum of cracks in the solder joint is less than 25% of critical zone length
Connectors		 2 components are necessary: - perpendicular to component axis for nominal assembly - parallel to component axis for repair process	-		
Radial magnetics	1553 transformers		-		
Sculptured flexible		-			No crack in the solder joint on the solder side at completion of the test.

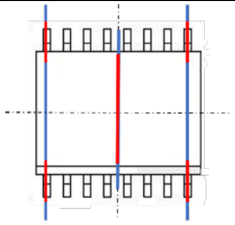
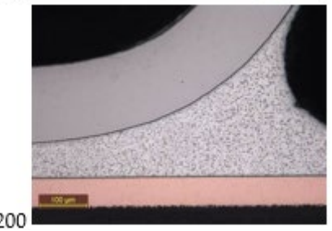
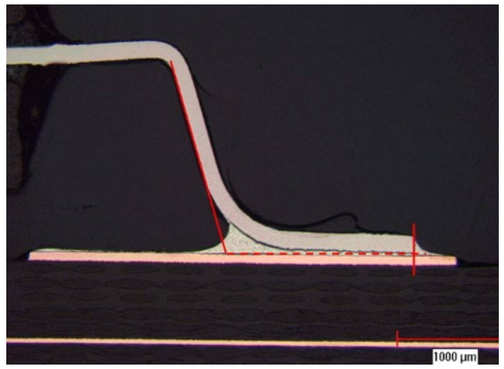
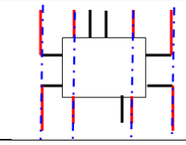
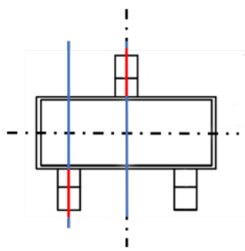
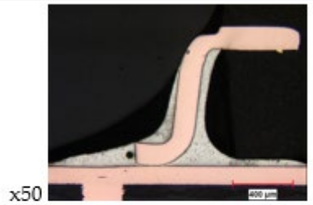
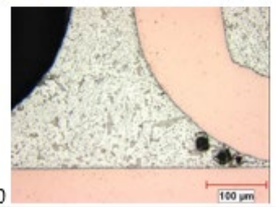
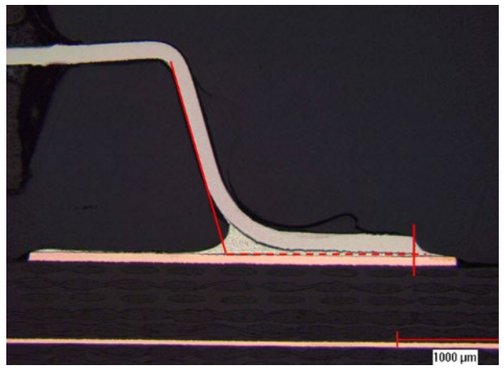
Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
Images in the table are informative examples only. Requirements are specified in text.					
Rectangular and square end-capped or end-metallized component with rectangular body	Chip resistors		 		The total sum of cracks in the solder joint is less than 60% of A+B and no crack in fillet area F The vertical limit to the fillet area F shall be the outermost ceramic edge. In addition, for ceramic chip capacitors, clause 14.15.4 is applicable for damages inside the component.
	Chip capacitors		 		
	Resistor array		-		

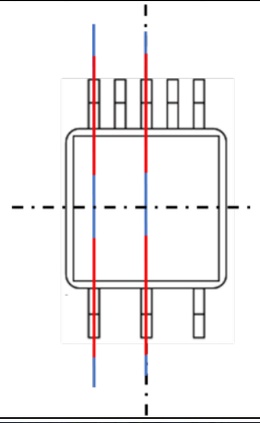
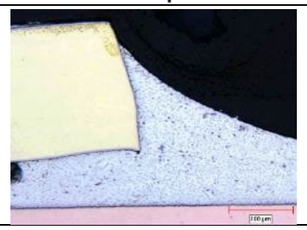
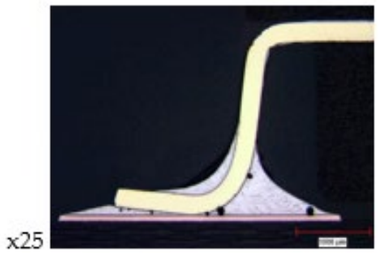
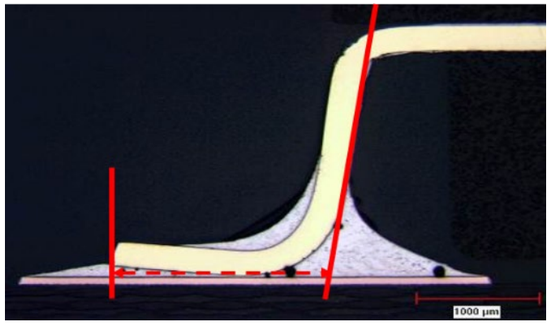
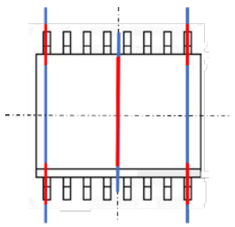
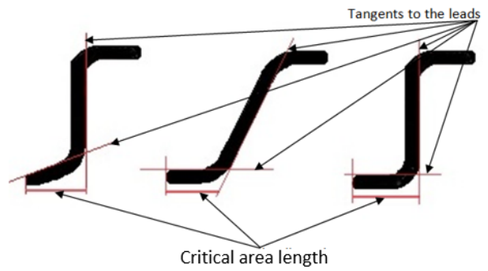
Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
Images in the table are informative examples only. Requirements are specified in text.					
Rectangular and square end-capped or end-metallized metallic component with rectangular body,	CSM				The total sum of cracks in the solder joint is less than 33% of lap connection
Cylindrical and square end-capped components with cylindrical body	MELF		 		The total sum of cracks in the solder joint is less than 33% of critical zone length
Bottom terminated chip component	Coil				The total sum of cracks in the solder joint is less than 33% of lap connection

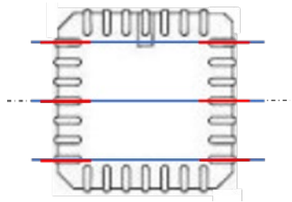
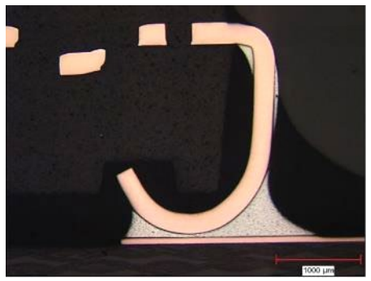
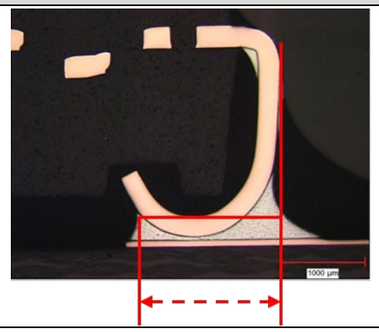
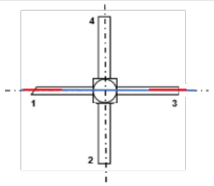
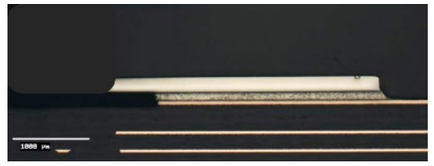
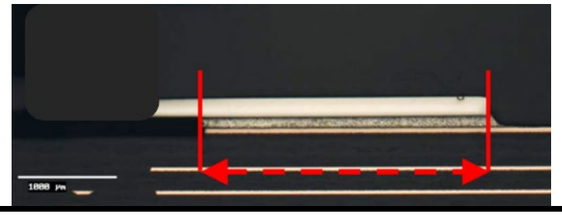
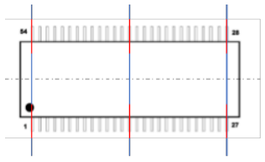
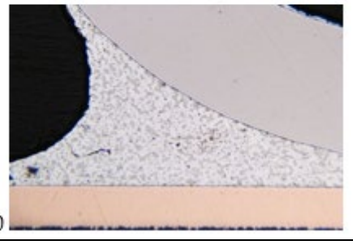
Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
Images in the table are informative examples only. Requirements are specified in text.					
Component with Inward formed L-shaped leads	Tantalum chip capacitor				The total sum of cracks in the solder joint is less than 33% of critical zone length
Leadless component with plane termination	SMD0.5, SMD1, SMD2, SMD0.2	 + X-ray prior to microsectioning	Absence of cracks in the ceramic to be checked by visual inspection prior to microsectioning x50   		The total sum of cracks in the solder joint is less than 33% of lap connection No cracks in the ceramic to be checked by visual inspection prior to microsectioning and by microsectioning.

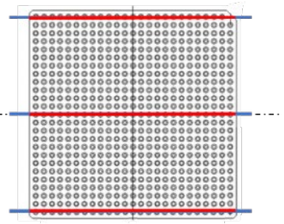
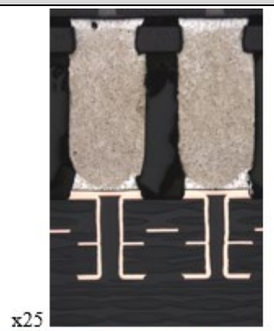
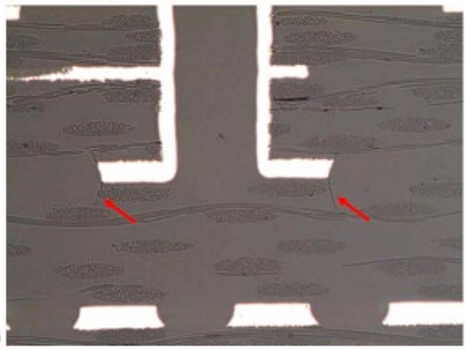
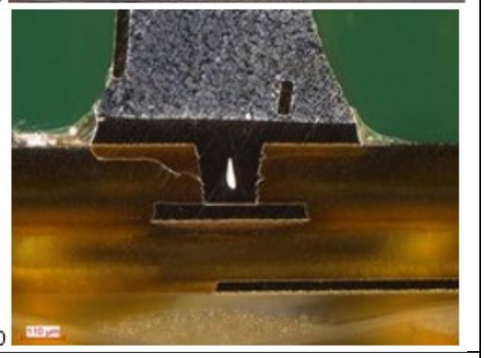
Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
Images in the table are informative examples only. Requirements are specified in text.					
Leaded component with plane termination	DPAK/TO252 D2 PAK SOT 223	 - X-ray+ micro section (lead + plane) - Microsection plane in on edge - Additional microsection depending on lead configuration (different dimensions or shape)	 		For lead, the total sum of cracks in the solder joint is less than 33% of critical zone length. For plane termination, X-ray criteria in accordance with clause 14.3.
Leadless ceramic chip carrier component	LCC3	With ground connection (microsection to be done in the middle of castellation)  Without ground connection	  The presence of AuSn intermetallic on the top of LCC package does not lead to a rejection		• The total sum of cracks in the solder joint length is less than 70% of A+B and no crack in fillet area F (blue area) **OR** • Total crack length in the solder joint less than 100% of A provided the following: - no crack in fillet area F - convex solder joint - wetting height (Y) 100% of castellation - solder wetting length on the solder footprint X shall be more than the wetting height Y The vertical limit to the fillet area F shall be the outermost ceramic edge in the castellation
	LCC with terminations on 2 faces	 all terminals to be microsectioned			
	LCC with termination on 4 faces				

Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
Images in the table are informative examples only. Requirements are specified in text.					
No lead Quad Flat Pack QFN	QFN	 When thermal plane is present, the third microsection is in the middle axis: 			The total sum of cracks in the solder joint is less than 33% of critical zone The total sum of cracks in the solder joint is less than 33% of exposed pad when present.
Flat pack and Gull-wing leaded component with round, rectangular, ribbon leads, Moulded magnetics	CQFP + MQFP	 Centre micro-section to be done only when component is bonded.	 Similar magnification to be applied for the assessment of the bonding lines.		The total sum of cracks in the solder joint is less than 33% of critical zone length Absence of crack in the adhesive

Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
Images in the table are informative examples only. Requirements are specified in text.					
Flat pack and Gull-wing leaded component with round, rectangular, ribbon leads, Moulded magnetics	FP, SO, SOIC	 Centre micro-section to be done only when component is bonded.	 		The total sum of cracks in the solder joint is less than 33% of critical zone length Absence of crack in the adhesive
	FP with spider leads				
	SOT 23		 		

Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
Images in the table are informative examples only. Requirements are specified in text.					
	1553 interface transformers or specific transformers	  Microsection plane in one edge. Additional microsection depending on lead configuration (different dimensions or shape)	 x25		The total sum of cracks in the solder joint is less than 33% of critical zone length Absence of crack in the adhesive
Flat pack and Gull-wing leaded component with round, rectangular, ribbon leads, Moulded magnetics	TSOP			 	The total sum of cracks in the solder joint is less than 10% of critical zone length

Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
Images in the table are informative examples only. Requirements are specified in text.					
"J" leaded component	ceramic leaded chip carriers (CLCC) and plastic leaded chip carriers (PLCC).				The total sum of cracks in the solder joint is less than 33% of critical zone length
Components with ribbon terminals without stress relief (flat lug leads)					The total sum of cracks in the solder joint is less than 33% of critical zone length
Stacked modules components with leads protruding vertically from bottom		 Can be reduced to two microsections when package is ≤ 50 leads	 		The total sum of cracks in the solder joint is less than 33% of critical zone length OR The total sum of cracks in the solder joint is less than 50% of critical zone length, provided leads length ≥2,9 mm and 5 micro-sectioned components

Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
Images in the table are informative examples only. Requirements are specified in text.					
Area Array components (Capability Phase only)	CCGA		 x25  x200  x200 Presence of cracks in the laminate and interconnection of microvia	Not applicable	For capability samples only: Acceptance criteria as defined in clause 13.3.2.
Solderless	Component, interposer and PCB	Cross sections of PCB pad in the contact area Cross section of interposer in the contact area Cross section of component plating	*No picture available for now*		Acceptance criteria as defined in clause 13.6.

14.15.4 Microsection acceptance criteria for ceramic chip capacitors

ECSS-Q-ST-70-61_1511045

a. Solder joint of ceramic chip capacitors after microsectioning shall be in compliance with Table 14-5.

ECSS-Q-ST-70-61_1511046

b. For ceramic chip capacitors damages inside the component after microsectioning shall be in compliance with Table 14-6.

NOTE 1. The cracks in the ceramic observed at completion of assembly verification may be located either on the top terminations or on the bottom terminations. The cause of the cracks depends on their location on the component.

NOTE 2 Cracks in the ceramic material at the bottom terminations can have several different root cause:

- Mechanical stress from bending the PCB during handling, depanelization, integration of the PCB in the unit or from mechanical testing.
- Thermal shock during soldering due to excessive solder tip temperature or the solder tip touching the component termination.

Due to the different root causes the repeatability of bottom side ceramic cracks are low.

The risk of bottom side terminations can be reduced by for example pre-heating the board before soldering, and using lower soldering tip temperatures, as also noted in requirement 10.2.5q.

NOTE 3 Cracks in the ceramic material at the top terminations can be caused by the pull stress occurring at cold temperatures during temperature cycling. Verification with reduced temperature range in accordance with clause 13.5 reduce the amount and size of such top side cracks.

EIA-469 issue E criteria for minimum insulation of the cover plate has been used to define the acceptance criteria of these cracks at the completion of assembly verification. EIA 469 issue E requires a minimum insulation of 80 µm for 50 V and above.

The as received thickness of the cover plate vary between different chip capacitor values and ratings, as well as between different batches. The ceramic cracks could furthermore occur on all corners of the part. Therefore the acceptability of ceramic cracks is assessed by projecting the worst crack seen on all 4 corners of the

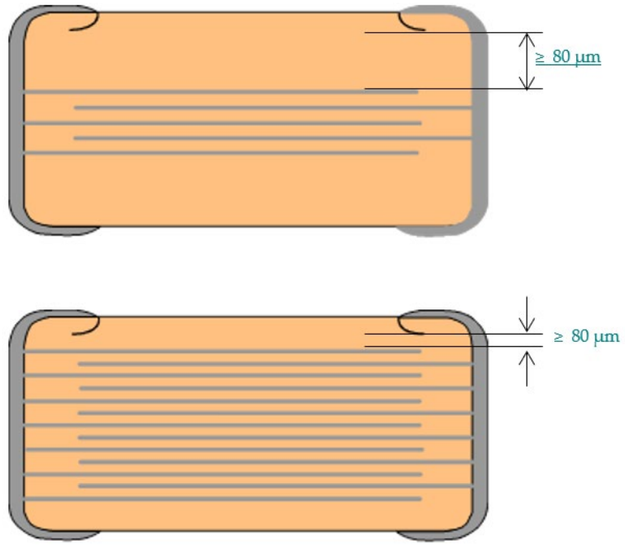
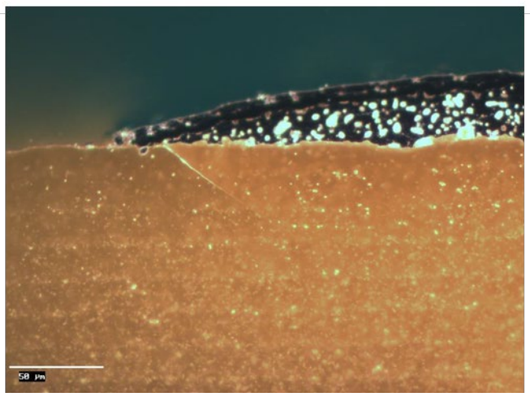
component and also by comparing it to the flight batch of the component.

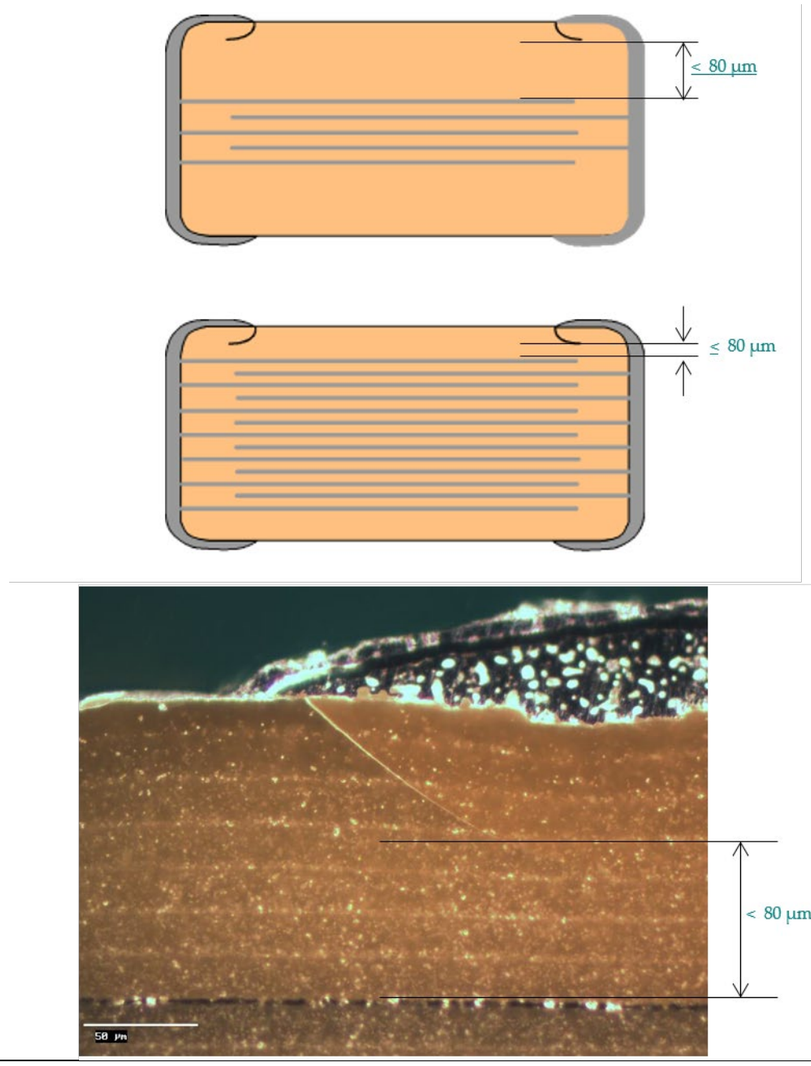
NOTE 4 For chip capacitors it is good practice to perform the verification on the capacitance value used which has the thinnest cover plate and most densely packed dielectric planes.

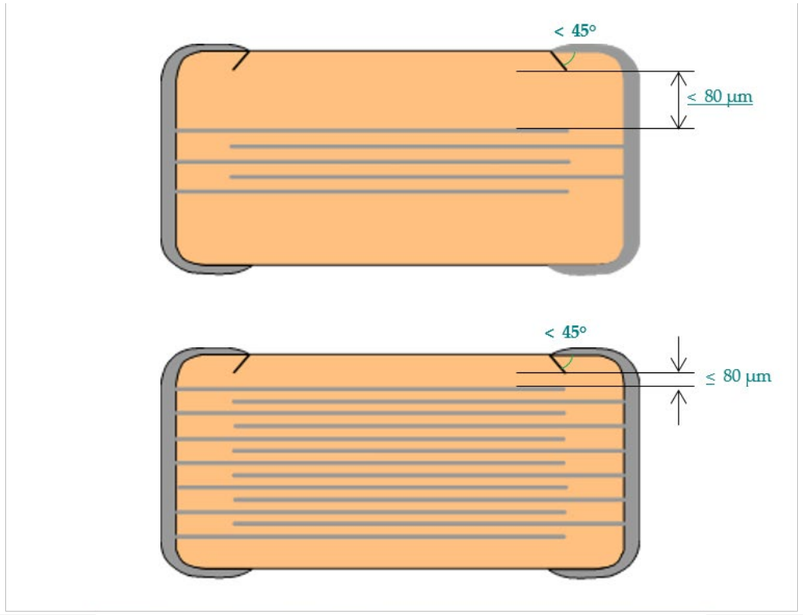
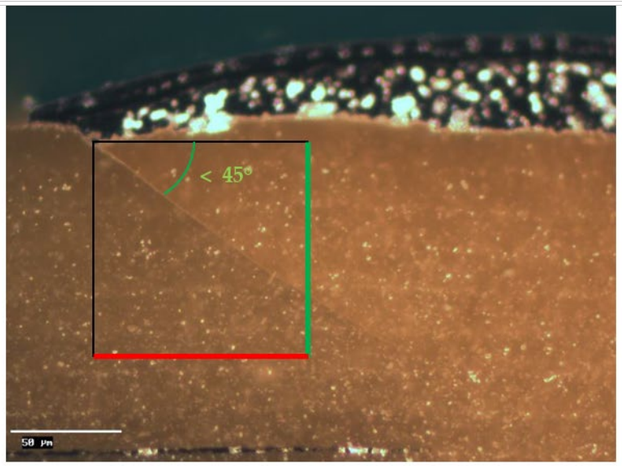
NOTE 5 EIA-469 issue E has been used to define the acceptance criteria for delaminations.

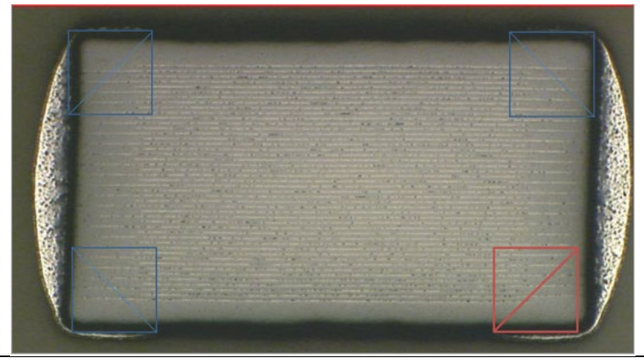
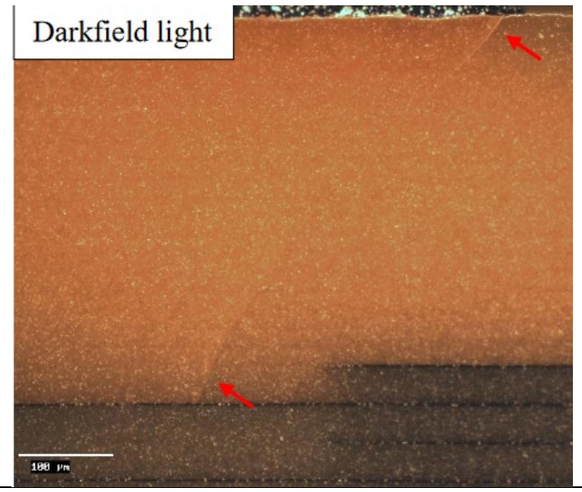
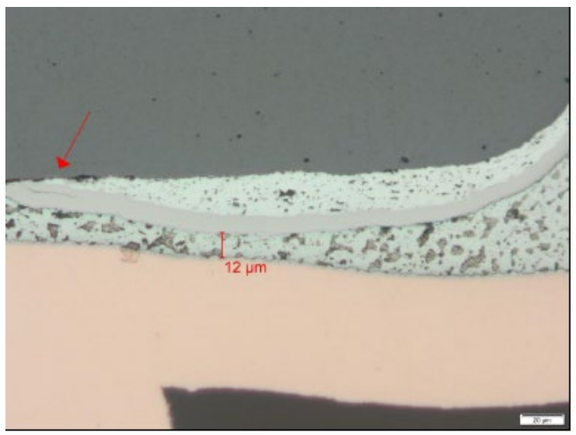
ECSS-Q-ST-70-61_1511047

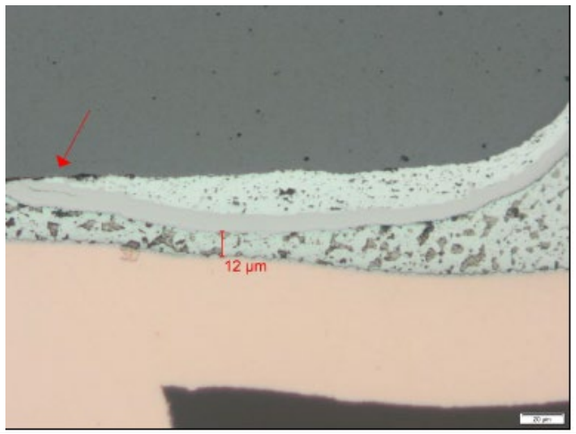
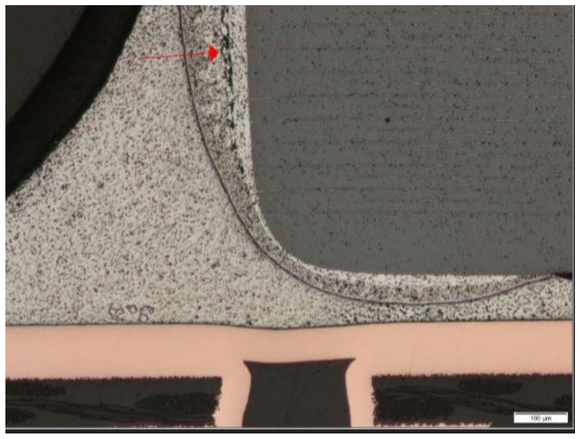
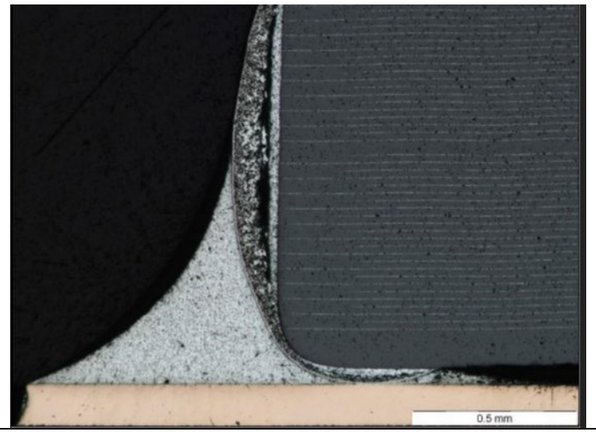
Table 14-6: Acceptance criteria for internal defects in ceramic chip capacitors after microsectioning

Type of defect	Location	Case	Figure	Additional note See also notes to 14.15.4a	Acceptance criteria
Crack in solder joint	N/A	N/A	N/A	N/A	See clause 14.15.3 and Table 14-5.
Crack in ceramic	Bottom terminations	N/A	N/A	Due to the different root causes the repeatability of bottom side ceramic cracks are low.	No cracks in the ceramic on the bottom termination.
	Top terminations	Case 1a: Crack curving towards the termination on same side and remaining cover plate thickness ≥ 80µm	 	Example: Assembly verified component has minimum 100 µm cover plate as received and a ceramic crack which reduces the insulation distance with 15 µm, i.e. 85 µm remaining insulation which is acceptable. This would in addition be acceptable justification for all chip capacitors of the same type, provided they have minimum 95 µm cover plate as received at all 4 corners.	Crack is curving towards the termination on same side. AND No cracks in the ceramic with less than 80 µm remaining insulation to first opposite electrode. AND Assessment is made based on the longest crack projected on all 4 corners of the component. AND In case of top side ceramic crack, project specific request for deviation is submitted with assessment made on the longest crack projected on the flight batch of component which is intended to be used.

Type of defect	Location	Case	Figure	Additional note See also notes to 14.15.4a	Acceptance criteria
Crack in ceramic	Top terminations	Case 1b: Crack curving towards the termination on same side and remaining cover plate thickness < 80µm		The review of ceramic cracks is assessed by projecting the worst crack seen on all 4 corners of the component and also by comparing it to the flight batch of the component. It is also good practice to compare the temperature cycling during verification and in the mission in which the component is intended to be used.	Not acceptable. May be accepted by project based on project specific request for deviation.

Type of defect	Location	Case	Figure	Additional note See also notes to 14.15.4a	Acceptance criteria
Crack in ceramic	Top terminations	Case 2a: Straight crack with ≤45° angle to electrode plane and no projected crossing of opposite electrodes	 	It is good practice to draw a quadrat from the root of the ceramic crack to assess the crack angle. See also Case 1a for an example of calculation of allowed crack length for a different component value than was verified.	Crack has maximum 45° angle to electrode plane. AND Minimum 80 µm remaining insulation to first opposite electrode from end of crack. AND The tangent of the crack does not cross any opposite electrode. AND Assessment is made based on the longest crack projected on all 4 corners of the component. AND In case of top side ceramic crack, project specific request for deviation is submitted with assessment made on the longest crack projected on the flight batch of component which is intended to be used.

Type of defect	Location	Case	Figure	Additional note See also notes to 14.15.4a	Acceptance criteria
Crack in ceramic	Top terminations	Case 2b: Straight crack with ≤45° angle to electrode plane and projected crossing of opposite electrodes		The review of ceramic cracks is assessed by projecting the worst crack seen on all 4 corners of the component and also by comparing it to the flight batch of the component. It is also good practice to compare the temperature cycling during verification and in the mission in which the component is intended to be used.	Not acceptable. May be accepted by project based on project specific request for deviation.
Crack in ceramic	Top terminations	Case 3: Straight crack with >45° angle to electrode plane		The review of ceramic cracks is assessed by projecting the worst crack seen on all 4 corners of the component and also by comparing it to the flight batch of the component. It is also good practice to compare the temperature cycling during verification and in the mission in which the component is intended to be used.	Not acceptable. May be accepted by project based on project specific request for deviation.
Delamination	Any termination	Chip capacitors size ≥1210		The delamination can have an impact on the size of the cracks in the solder joint as they provide stress relief.	No delamination larger than 130 µm. AND Successful assembly verification results without any delamination for at least one sample.

Type of defect	Location	Case	Figure	Additional note See also notes to 14.15.4a	Acceptance criteria
		Chip capacitors size <1210		N/A	Not acceptable. May be accepted by project based on project specific request for deviation.
		Chip capacitors with flexible terminations	 	The risk of delamination in the vertical part of the flexible polymer layer can be reduced by the decreasing the solder height.	Not acceptable. May be accepted by project based on project specific request for deviation.

14.16 Anomalies in PCB and sculptured flex during verification

ECSS-Q-ST-70-61_1511048

a. After verification testing the acceptance criteria of ECSS-Q-ST-70-60 clause 10.3 and 10.5 shall apply, except for the case specified in requirements 14.16b and 14.16c.

NOTE 1 ECSS-Q-ST-70-60 includes acceptance criteria for cracks in dielectrics for PTH.

NOTE 2 ECSS-Q-ST-70-60 Table 10-25 includes acceptance criteria for pad lift types and Table 10-26 for dielectric cracks.

ECSS-Q-ST-70-61_1511049

b. Anomalies outside the conditions specified in requirement 14.16a may be accepted provided that at least one of the following conditions is met:

1. Presence of anomaly also during PCB procurement, either on the PCB coupons or in certificate.
2. Presence of anomaly also on a spare non-assembled nor tested PCB.
3. Presence of anomaly also on a spare footprint, included on the verification board, showing that the defect was not caused by the assembly processes.

NOTE It is good practice to include additional footprints on the verification board, which are not populated, to assist failure investigations.

ECSS-Q-ST-70-61_1511050

c. Cracks in the dielectrics under SMT footprints, outside the conditions specified in requirement 14.16a, may be accepted provided that the remaining insulation distance of the flight PCB is in conformance with the PCB definition dossier.

ECSS-Q-ST-70-61_1511051

d. Cracks in the Printed Circuit Board that have not been identified in the clause 10 of ECSS-Q-ST-70-60 shall be unacceptable.

ECSS-Q-ST-70-61_1511052

e. Defects, such as footprint lifting, cracks in laminate, cracks in via, cracks of tracks, PCB delamination shall be recorded as a nonconformance and analysed.

15 Outsourcing

15.1 General

ECSS-Q-ST-70-61_1511053

a. A supplier may be designated for outsourcing from a customer provided that the following conditions are met:

1. Outsourcing activities are limited to degolding and pretinning, lead forming, hand soldering, bonding, staking and conformal coating.
2. The manufacturing processes to be performed are included in the customer's PID approved by the Approval Authority.
3. The manufacturing at the supplier site is performed with the same materials as the one used by the customer.
4. The manufacturing at the supplier site is performed in compliance with the manufacturing procedures of the customer PID.
5. In case the outsourcing includes lead forming activities, the demonstration that lead geometry is identical are provided to the customer.
6. The customer is responsible for the assembly carried out by the supplier,
7. The supplier fills in the manufacturing traveller of the customer.
8. In case the supplier is not equipped to fill in the manufacturing traveller of the customer, he can use his own manufacturing traveller provided that it has been reviewed and accepted by the customer.
9. All operators and inspectors working at the supplier site are trained and certified according to clause 17.8 and being active in their certification status.
10. All operators and inspectors working at the supplier site for the customer as outsourcing are trained on customer applicable PID procedures and certified by the instructor of the customer.

NOTE For the requirement 15.1a.3, ideally those materials are provided in the kitting.

ECSS-Q-ST-70-61_1511054

b. The operators and inspectors shall work only on one set of specified process procedures at a time at the supplier site.

ECSS-Q-ST-70-61_1511055

c. The customer shall issue and maintain a certification matrix of the certification status of the supplier’s operators and inspectors including the name of the instructor and the supplier assembly contact point name.

ECSS-Q-ST-70-61_1511056

d. The customer PID shall identify the certification matrix with the associated names of the supplier involved personnel.

ECSS-Q-ST-70-61_1511057

e. The manufacturing dossier of the boards and unit shall identify the operations performed by the supplier.

ECSS-Q-ST-70-61_1511058

f. The customer shall appoint a person in charge of NCRs issued by customer and supplier.

ECSS-Q-ST-70-61_1511059

g. The supplier shall be informed about assembly NCRs in the customer assembly line.

ECSS-Q-ST-70-61_1511060

h. The customer shall conduct an audit at supplier according to clause 13.1.3 to verify the compliance of the assembly line.

ECSS-Q-ST-70-61_1511061

i. The customer shall provide to the Approval Authority the audit report.

ECSS-Q-ST-70-61_1511062

j. In case of modification in the procedures, the supplier operators and inspectors shall be informed, trained, and certified according to requirement 15.1a.10.

ECSS-Q-ST-70-61_1511063

k. KIPs shall be performed by the customer inspector,

ECSS-Q-ST-70-61_1511064

l. The customer shall have a storage, packing and transportation procedure for the hardware manufactured at supplier assembly line,

ECSS-Q-ST-70-61_1511065

m. Incoming inspections of the assembly shall be performed by the customer to verify absence of damage due to the storage, packing and transportation,

ECSS-Q-ST-70-61_1511066

n. Every 4 years the customer shall invite the Approval Authority to participate the audit of the supplier assembly line, in compliance with requirement 13.1.3f.

ECSS-Q-ST-70-61_1511067

o. The customer shall list in its PID the supplier as “outsourcing” to manufacture hardware.

16
Process identification document (PID)

16.1 Overview

The purpose of the PID is to establish a precise reference for the assembly processes approved in accordance with this Standard.

The PID provides a standard reference against which any anomalies occurring after the approval can be examined and resolved.

16.2 Document preparation

ECSS-Q-ST-70-61_1511068

a. Prior to any start of verification, the supplier shall provide a draft PID to the Approval Authority, in conformance with the DRD in Annex C.

ECSS-Q-ST-70-61_1511069

b. The PID may supersede the requirements from this standard in case supplier can demonstrate that any deviation recorded in the PID is approved by Approval Authority based on tests results.

16.3 Approval

ECSS-Q-ST-70-61_1511070

a. The PID shall be submitted to the Approval Authority

ECSS-Q-ST-70-61_1511071

b. The Approval Authority shall approve the PID.

NOTE The approval can be achieved by PID signature or minutes of meeting being signed by the Approval Authority.

16.4 Contact person

ECSS-Q-ST-70-61_1511072

a. The supplier shall appoint a contact person for assembly topics.

16.5 Process identification document update

ECSS-Q-ST-70-61_1511073

a. A PID shall represent the verified manufacturing processes and production controls.

ECSS-Q-ST-70-61_1511074

b. Any proposed change to the PID shall be agreed by the Approval Authority.

ECSS-Q-ST-70-61_1511075

c. At least every two years the supplier shall perform a review of the PID, the summary table and the relevant applicable documents for agreement by the Approval Authority.

ECSS-Q-ST-70-61_1511076

d. The PID shall be managed in accordance with configuration control requirements of ECSS-M-ST-40.

17 Quality assurance

17.1 General

ECSS-Q-ST-70-61_1511077

a. Requirements from clause 5 from ECSS-Q-ST-20 shall apply for "Quality assurance".

17.2 Data

ECSS-Q-ST-70-61_1511078

a. Quality records shall be retained for at least ten years, or in accordance with the project contract.

NOTE Example of quality records are travellers log, work orders.

ECSS-Q-ST-70-61_1511079

b. Quality records shall be gathered in the Verification report in conformance with the DRD in Annex B.

ECSS-Q-ST-70-61_1511080

c. The following documents, as a minimum, shall be made available to supplier

1. PID.
2. Audit report established by the Approval Authority.
3. Verification report.

17.3 Nonconformance

ECSS-Q-ST-70-61_1511081

a. The requirements from clauses 5 and 6 from ECSS-Q-ST-10-09 shall apply for "Nonconformance".

17.4 Calibration

ECSS-Q-ST-70-61_1511082

a. Equipment and tools, degolding and pretinning bathes, soldering equipment, and measuring equipment shall be calibrated within a period of one year.

ECSS-Q-ST-70-61_1511083

b. The supplier shall maintain records of the calibration according to clause 5.2.6 of ECSS-Q-ST-20.

ECSS-Q-ST-70-61_1511084

c. A suspected or confirmed tool or equipment failure shall be recorded as a project nonconformance.

NOTE The records can aid early detection of a trend towards nonconformance.

ECSS-Q-ST-70-61_1511085

d. Defective or out of calibration date equipment or tools shall be labelled or removed from work areas.

ECSS-Q-ST-70-61_1511086

e. The Approval Authority shall be notified of the nonconformance.

17.5 Traceability

ECSS-Q-ST-70-61_1511087

a. The requirements from clause 5.2.5 of ECSS-Q-ST-20 shall apply for traceability.

17.6 Workmanship standards

ECSS-Q-ST-70-61_1511088

a. The supplier shall prepare in-house visual workmanship standards to be made available to each operator and inspector.

NOTE 1 Examples are: Satisfactory work samples or visual aids which illustrate the quality characteristics of all types of soldered connection involved in the task.

NOTE 2 The illustrations presented in Annex F and Annex E this standard can be included as part of the examples.

17.7 Inspection points

ECSS-Q-ST-70-61_1511089

a. During all stages of the process, the inspection points defined in the manufacturing flow chart shall be carried out.

ECSS-Q-ST-70-61_1511090

b. The inspection shall be performed in conformance with clause 12.

17.8 Operators, inspectors and instructors training and certification

ECSS-Q-ST-70-61_1511091

a. Trained and certified personnel shall be employed for soldering operations and inspections.

ECSS-Q-ST-70-61_1511092

b. A training programme shall be developed, maintained and implemented by the supplier to provide excellence of workmanship and personnel skills in soldering.

ECSS-Q-ST-70-61_1511093

c. Records of training, testing and certification status of the operators and inspectors shall be maintained for at least 10 years.

ECSS-Q-ST-70-61_1511094

d. The training programme shall include procedures for the training, internal certification, maintenance of certified status, recertification, and revocation of certified status for soldering and inspection personnel.

ECSS-Q-ST-70-61_1511095

e. Training success shall be based on objective evidence of soldering quality, resulting from practical training and inspection of soldered joints.

ECSS-Q-ST-70-61_1511096

f. Personnel shall be retrained or re-assessed in the following circumstances:

1. Repeated quality nonconformance.
2. Change in soldering techniques.
3. Change in soldering parameters.
4. Additional process skills.

ECSS-Q-ST-70-61_1511097

g. The operators performing X-ray inspection shall be trained and in-house certified to perform and assess X-ray results.

ECSS-Q-ST-70-61_1511098

h. Operators, inspectors and instructors shall be certified at an ESA school in compliance with ESA STR-258 or in-house training authorised by the Approval Authority.

ECSS-Q-ST-70-61_1511099

i. Operators and inspectors may be re-certified at an ESA school or by an in-house instructor authorised by the Approval Authority.

NOTE The supplier company is responsible for checking the constant visual acuity of its workers i.a.w. ESA STR-258 to maintain certification status of personnel.

Annex A (normative) Verification programme - DRD

A.1 DRD identification

A.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-61, requirement 13.1.4a.

A.1.2 Purpose and objective

The purpose of the Verification programme DRD is to detail the requirements for the documentation of the verification programme.

A.2 Expected response

A.2.1 Scope and content

ECSS-Q-ST-70-61_1511100

a. The verification programme documentation shall contain as a minimum the following:
   1. Indication of process of the assembly:
      (a) soldering process
      (b) repair process.
   2. Substrate information:
      (a) PCB material and manufacturer
      (b) PCB footprint surface finish
      (c) Number of layers
      (d) Thickness
      (e) Build up with identification of signal and full copper plane
      (f) Connection of the footprints to the internal layer representative of the FM
      (g) Location of the components on the PCB
      (h) For through hole component, ratio of hole to lead diameter
      (i) Location of the mechanical fixation or stiffeners if any
      (j) Number of PCB used for the verification programme.
   3. Materials used
      (a) Solder paste and wire designation, commercial trademark, and composition with associated flux class

(b) Flux class used for pretinning and soldering

(c) Conformal coating

(d) Adhesive, potting, underfill and encapsulants used for mechanical and for thermal purpose

(e) Solvent

(f) Others.

4. List of components with their materials leads and finish
5. Environmental test conditions and facility
6. Electrical continuity test specification, procedure
7. Verification method Microsection or Electrical monitoring
   (a) Microsection laboratory.
8. PID and Manufacturing document process references
9. Verification workflow
10. Verification by similarity
11. Certification status of the operators and inspectors
12. Compliance status of the operators and inspectors
13. Compliance of the manufacturing room
14. Additional information.

ECSS-Q-ST-70-61_1511101

b. The content of Verification programme specified in requirement A.2.1a may be tailored for companies already having an approved PID in accordance with this standard.

A.2.2 Special remarks

None.

Annex B (normative) Verification report - DRD

B.1 DRD identification

B.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-61, requirement 13.1.6a.

B.1.2 Purpose and objective

The purpose of the Verification report DRD is to summarize all the verification test specifications, procedures and test results which are relevant for the approval of the assembly component verifications.

B.2 Expected response

B.2.1 Scope and content

ECSS-Q-ST-70-61_1511102

a. The verification documentation shall contain as a minimum the following:
   1. Indication of process of the assembly:
      (a) soldering process
      (b) repair process.
   2. PCB information:
      (a) PCB material and manufacturer
      (b) PCB footprint surface finish
      (c) Number of layers
      (d) Thickness
      (e) Build up with identification of signal and full copper plane
      (f) Connection of the footprints to the internal layer representative of the FM
      (g) Location of the components on the PCB
      (h) For through hole component, ratio of hole to lead diameter
      (i) Location of the mechanical fixation or stiffeners if any
      (j) Number of PCB used for the verification programme.
   3. Materials used
      (a) Solder paste and wire designation, commercial trademark, and composition with associated flux class
      (b) Flux class used for pretinning and soldering
      (c) Conformal coating

(d) Adhesive for mechanical, and for thermal

(e) Solvent

(f) Others.

4. List of components with their materials leads and finish (including traceability).
5. Mechanical specification of the component with associated manufacturer specification.
6. Environmental test conditions and facility
7. Visual inspection report established in conformance with the requirements of clause 12
8. Summary of cleanliness test results in conformance with clause 11.1.2 of ECSS-Q-ST-70-61 or equivalent process when applicable
9. Tests results concerning the warp (bow) and twist of circuit board in conformance when applicable
10. Electrical continuity test report for multilayer boards when applicable
11. Verification method Microsection or Electrical monitoring

    (a) Microsection laboratory
12. PID and Manufacturing document process references
13. Verification workflow
14. Verification by similarity
15. NCRs
16. Certification status of the operators and inspectors
17. Compliance status of the operators and inspectors
18. Compliance of the manufacturing room
19. Quality records
20. Additional information.

ECSS-Q-ST-70-61_1511103

b. The verification report shall contain the results of all tests performed according to clauses 12 and 14.

ECSS-Q-ST-70-61_1511104

c. The verification report shall contain photographic evidence of the tested assembled boards where possible.

ECSS-Q-ST-70-61_1511105

d. The verification report shall contain the manufacturing soldering log according to clause 13.2.4.

ECSS-Q-ST-70-61_1511106

e. The verification report shall contain the list of all NCRs referring to assembly and test of verification boards and associated reports.

B.2.2 Special remarks

None.

Annex C (normative) Process Identification Documentation (PID) - DRD

C.1 DRD identification

C.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-61 requirement 16.2a.

C.1.2 Purpose and objective

The purpose of the PID is to consolidate the overall management, process and facilities utilised during the manufacturing and verification of the assembly.

C.2 Expected response

C.2.1 Scope and content

<1> SECTION 1: Document Format

ECSS-Q-ST-70-61_1511107

a. The PID shall contain the following information about the Document Format:
   1. Cover page: document title, document reference, revision number and date, page numbering, signing of Production and Quality representatives,
   2. Follow-up of PID updates: registration of PID updates indicating the nature of the update and the sections and pages updated,
   3. Purpose and scope of the document,
   4. Table of contents.

<2> SECTION 2: Manufacturing control

ECSS-Q-ST-70-61_1511108

a. The PID shall contain the Manufacturing control flow chart of the verified assembly.

NOTE 1 This illustrates the various stages of procurement, manufacturing and inspection

operations specific to this technology in a flow chart format.

NOTE 2 It can be used to identify, among others:

- the operation,
- the body responsible for its implementation,
- related documents: (only their reference),
- procurement specifications (for materials),
- acceptance inspection procedures (for materials and components),
- manufacturing procedures,
- manufacturing and quality control procedures during and at the end of production.
- storage documentation

<3> SECTION 3: Specifications

ECSS-Q-ST-70-61_1511109

a. The PID shall contain the following information about Specifications:

1. List of procurement specifications, assembly procedures and inspection procedures concerning the technology dealt within the PID, including the precise title, the reference or number, the revision number and date of each document
2. Printed circuit design rules in compliance with requirements from ECSS-Q-ST-70-12.
3. General Quality Assurance documents relating to the technology.

<4> SECTION 4: Organisation

ECSS-Q-ST-70-61_1511110

a. The PID shall contain the following information about Organisation:

1. Represented as a flow chart: organization of the company, organization of production department and organization of the quality Department.
2. Focal point and PID responsible,
3. Operators and inspectors' certification methodology.

<5> SECTION 5: Manufacturing traveller or log file

ECSS-Q-ST-70-61_1511111

a. The PID shall contain as a minimum the following information about the Manufacturing traveller or log file:

1. The sequencing of the various operations in their logical order of execution,

2. The references of the documents referred to and used during these operations,
3. The references of the Quality documents to trace the various batches of material used (record reference), together with the workstations and tools employed,
4. The signatures of the various actors with the date on which the task was completed.

<6> Section 6: List of verified technologies

ECSS-Q-ST-70-61_1511112

a. The PID shall contain as a minimum the following information about the list of verified technology:
   1. List of materials,
   2. Temperature and time profiles for the soldering machines used in the verification,
   3. List of verified components per assembly configuration,
   4. List of assembly sensitive components,
   5. List of components with limited project verification,
   6. For limited project verification, non-compliance with clause 13 shall be clearly identified.

<7> SECTION 7: Description of production line

ECSS-Q-ST-70-61_1511113

a. The PID shall contain as a minimum the following about the Description of production line:
   1. Layout of premises with associated surface area, with indication of location of production machines and quality inspection,
   2. Working environment; cleanliness class, ambient temperature limits, humidity, and positive pressure limits for each type of activities.

<8> SECTION 8: List of equipment

ECSS-Q-ST-70-61_1511114

a. The PID shall contain a list of all machines and tools utilised during the manufacturing activity.

<9> SECTION 9: List of laboratory services

ECSS-Q-ST-70-61_1511115

a. The PID shall contain range and capability of supporting laboratory services.

<10> SECTION 10: Project assembly heritage

ECSS-Q-ST-70-61_1511116

a. The PID shall contain a list of assembled board with associated assembly process by year manufactured in accordance with the PID.

C.2.2 Special remarks

None.

Annex D (normative) Assembly Summary Table - DRD

D.1 DRD identification

D.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-61, requirement 13.1.7d.

D.1.2 Purpose and objective

The purpose of the assembly summary table is to consolidate the approval status of the boundary conditions for the verification activity.

An assembly summary table is issued for each assembly process.

D.2 Expected response

D.2.1 Scope and content

ECSS-Q-ST-70-61_1511117

a. The assembly summary table shall include the following data:
   1. Assembly processes
   2. PID reference with issue
   3. Solder type for machine reflow and for hand assembly
   4. Conformal coating
   5. Substrate type
   6. Component data.

      NOTE An example of a component type preparation and mounting configuration table is given in Figure D-1.

D.2.2 Special remarks

None.

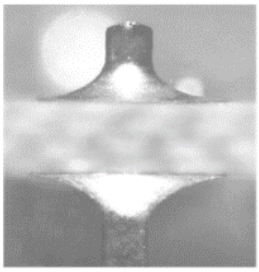
Component family	Package	Manufacturer	Package dimensions	Bonding material (under component)	Staking material (edge or corner)	Termination material	Lead finish	Pitch (mm)	Nominal Termination thickness (mm)/ Nominal width	In-House degolding / pretinning	In-house lead forming Yes/No/NA	Artificial stand-off Yes/No	Final report
Ceramic chip	C0603 Type I		Length, width	NA	NA		Sn/Pb	NA	NA	No	N/A	No	
Ceramic	C0603 Type II										N/A		
Ceramic resistor	R0805			NA	NA		Sn/Pb	NA	NA	No	N/A	No	
Diode	D5-B										N/A		
Tantalum capacitors													
IC	FP10 Bottom brazed			yes	One the side	Alloy42	Gold	1,27	0,25	yes	yes	NA	
CQFP	CQFP196 top brazed					Kovar					No		

Figure D-1: Example of component type preparation and mounting configuration

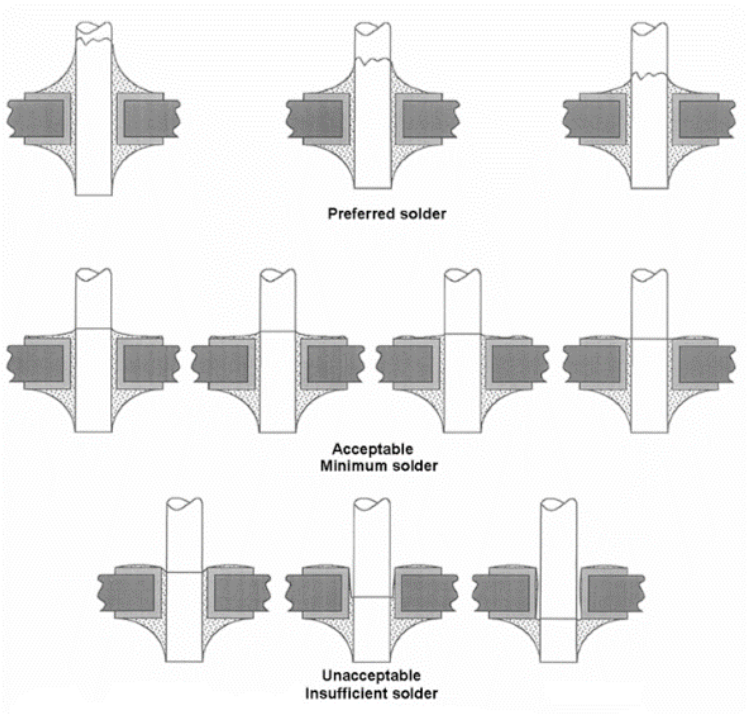
Annex E (normative) Visual workmanship standards for through hole component

E.1 Soldered stud terminals

NOTE: See clause 10.3.3 for details and allowed exceptions



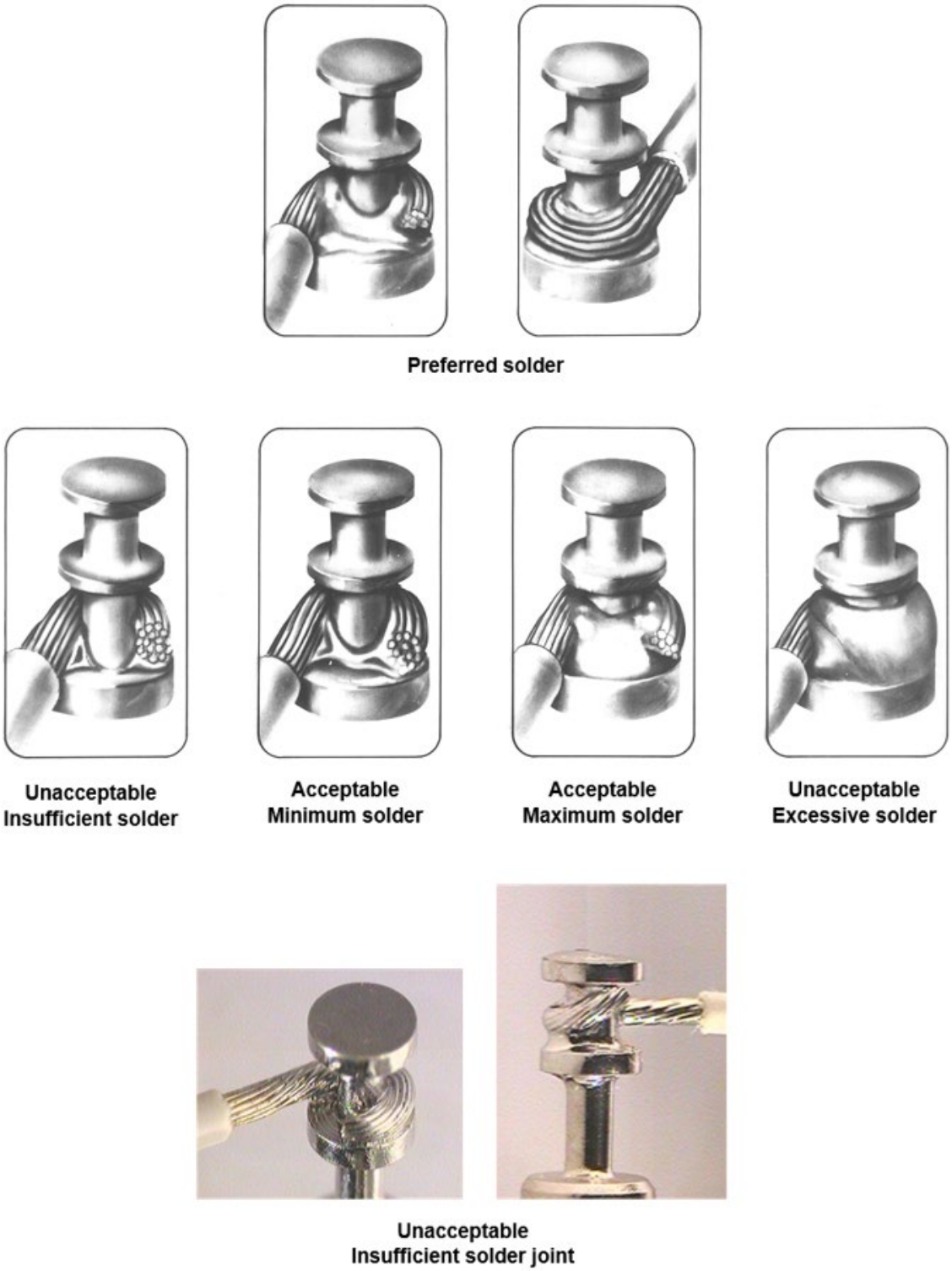
Preferred solder



ECSS-Q-ST-70-61_1511118

Figure E-1 : Soldered stud terminals

E.2 Soldered turret terminals



ECSS-Q-ST-70-61_1511119

Figure E-2: Soldered turret terminals with single conductors

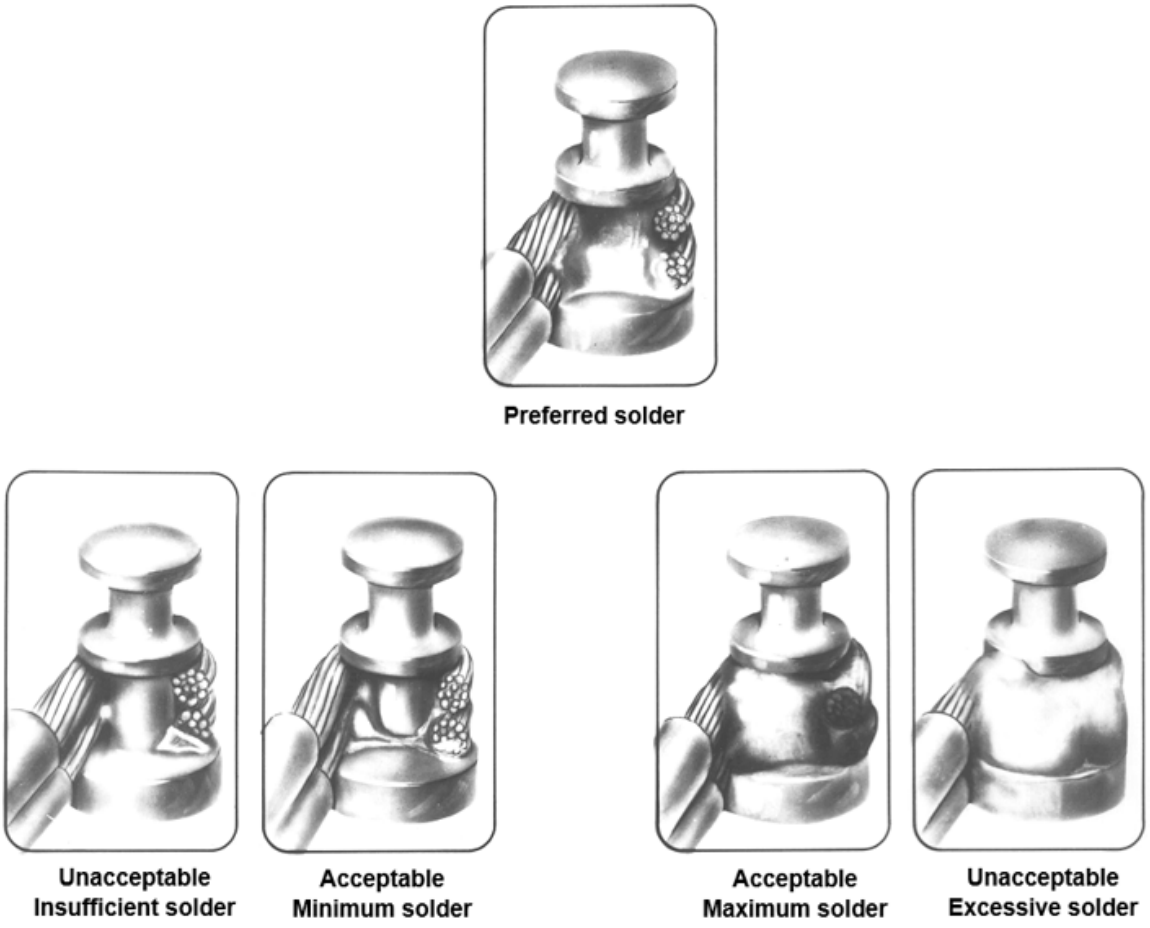
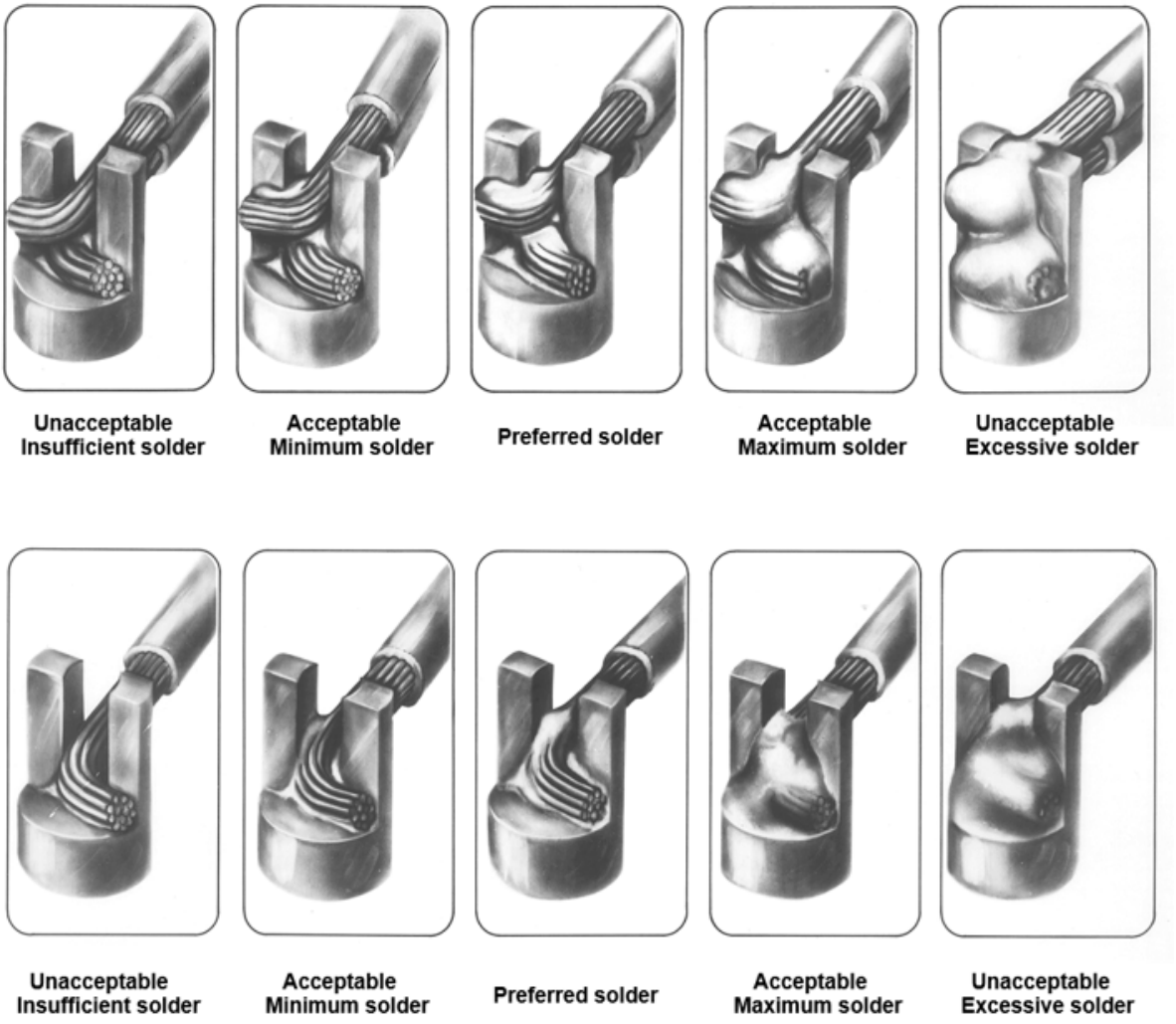


Figure E-3: Soldered turret terminals with twin conductors

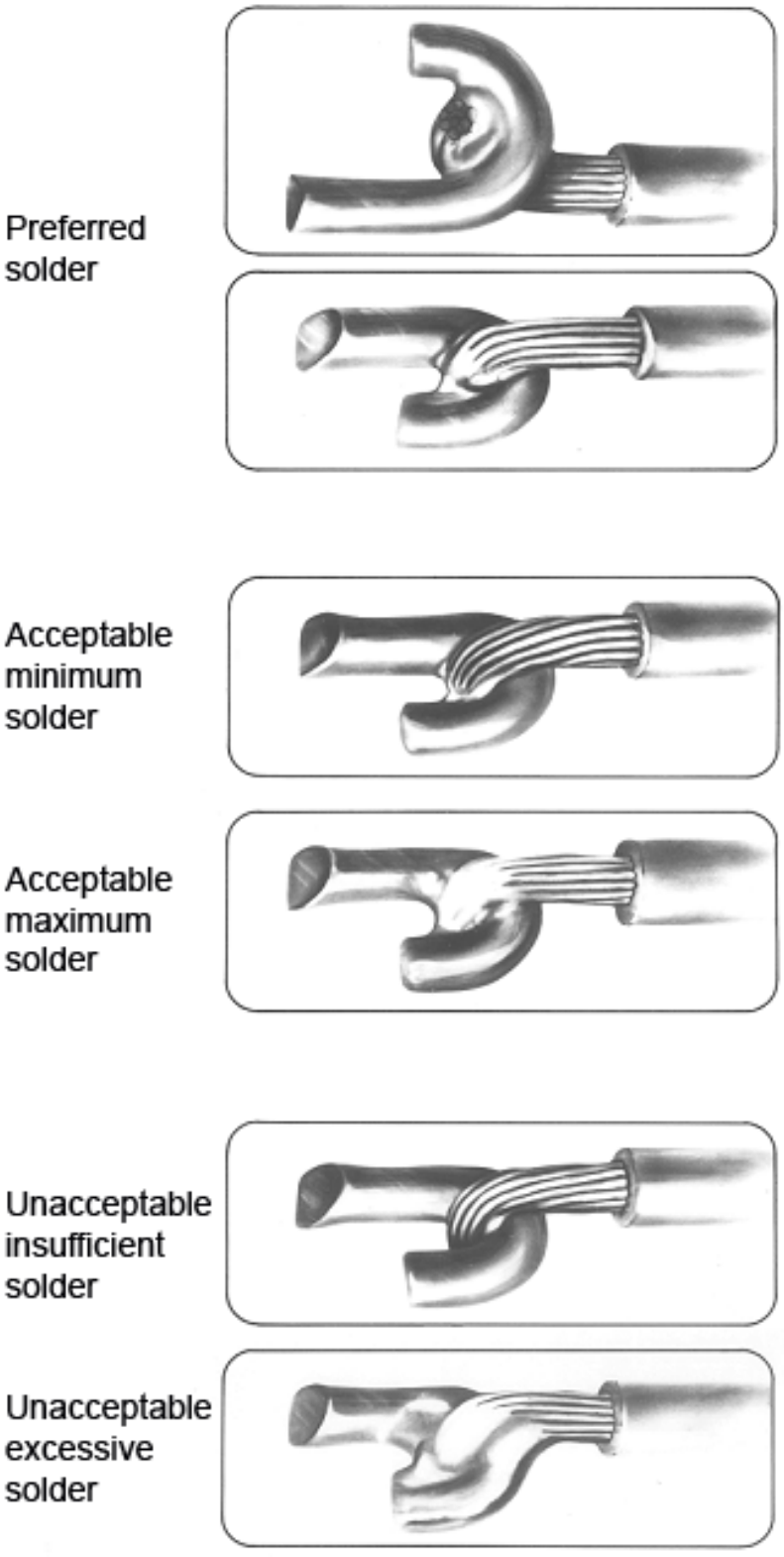
E.3 Soldered bifurcated terminals



ECSS-Q-ST-70-61_1511121

Figure E-4: Soldered bifurcated terminals

E.4 Soldered hook terminals



ECSS-Q-ST-70-61_1511122

Figure E-5: Soldered hook terminals

E.5 Soldered cup terminals

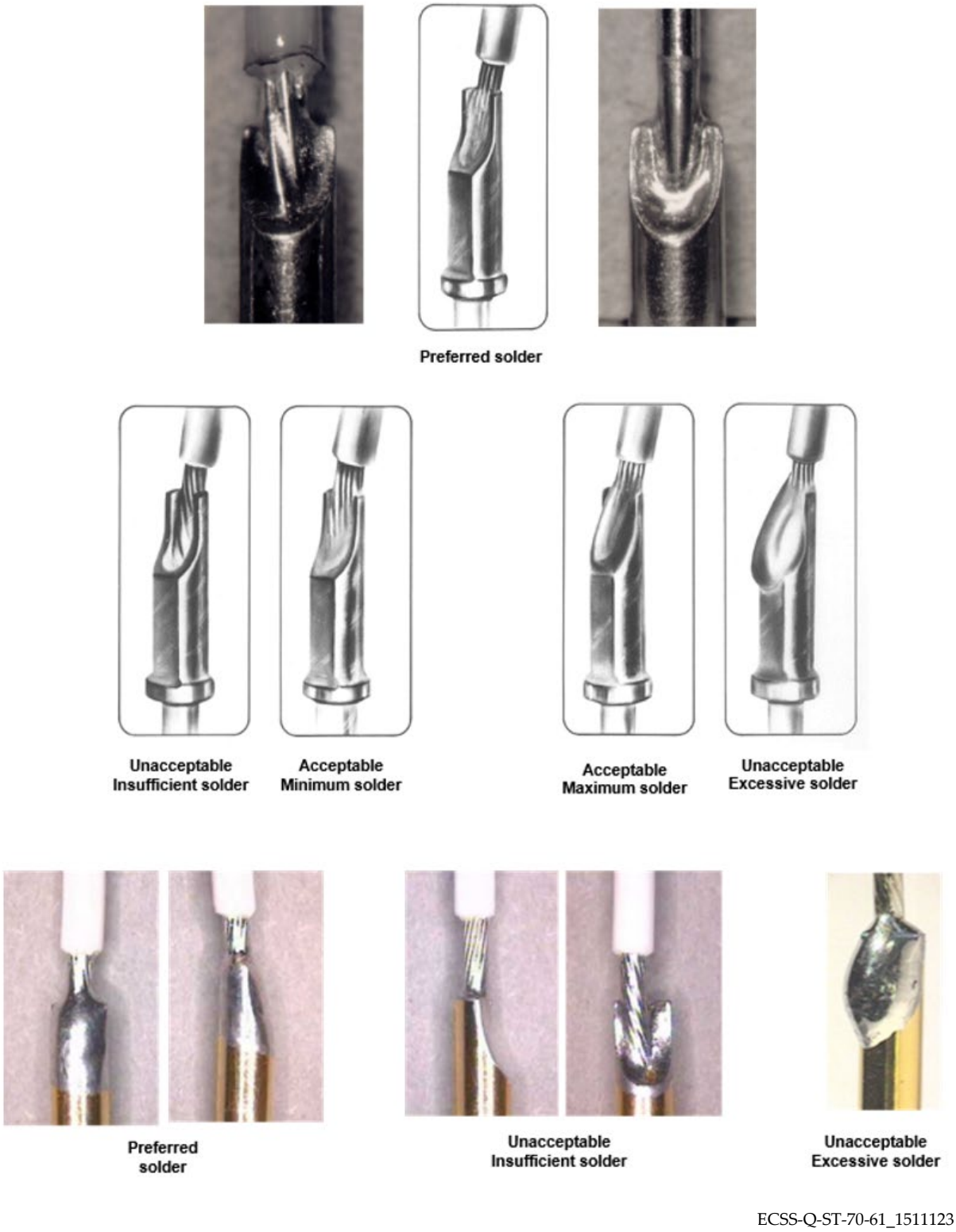


Figure E-6: Soldered cup terminals

E.6 Miscellaneous examples of soldered wires

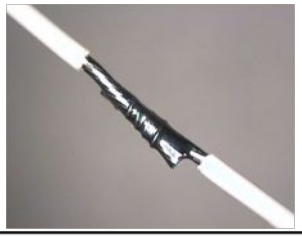
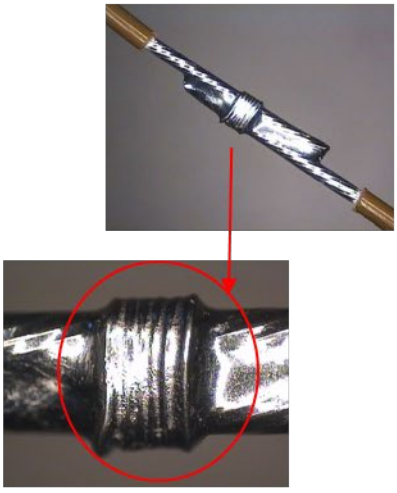
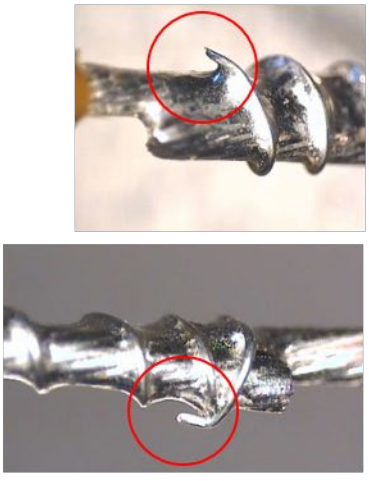
	**Unacceptable** **Excessive solder** Wire, terminal, component lead not visible
	**Unacceptable** Misalignment of wires
	**Unacceptable** Twisted wires jointed. Solder between turns not visible
	**Unacceptable** Strand of twisted wire standing off

Figure E-7: Examples of unacceptable soldered wires

E.7 Soldered wire to shielded cable interconnections

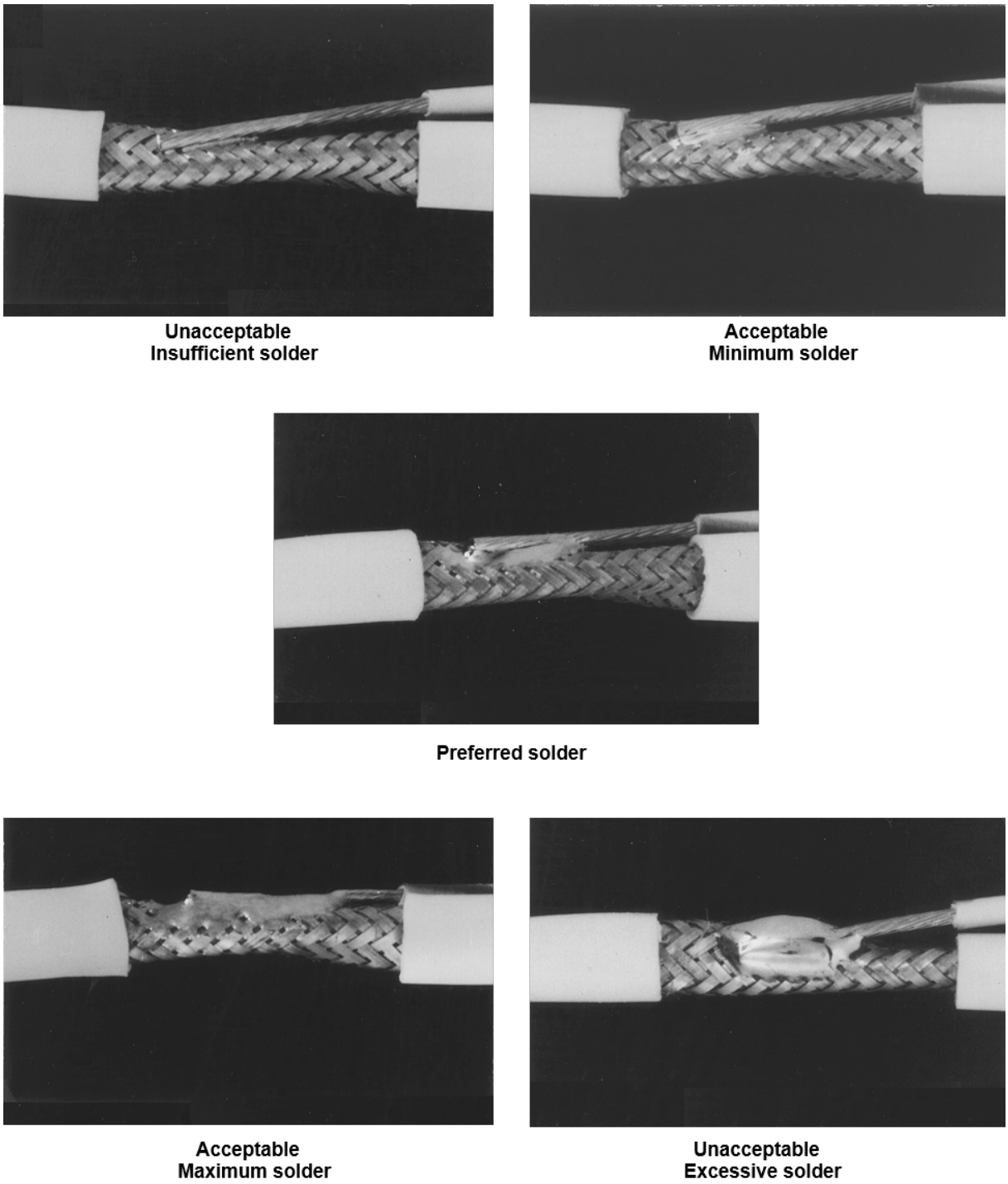
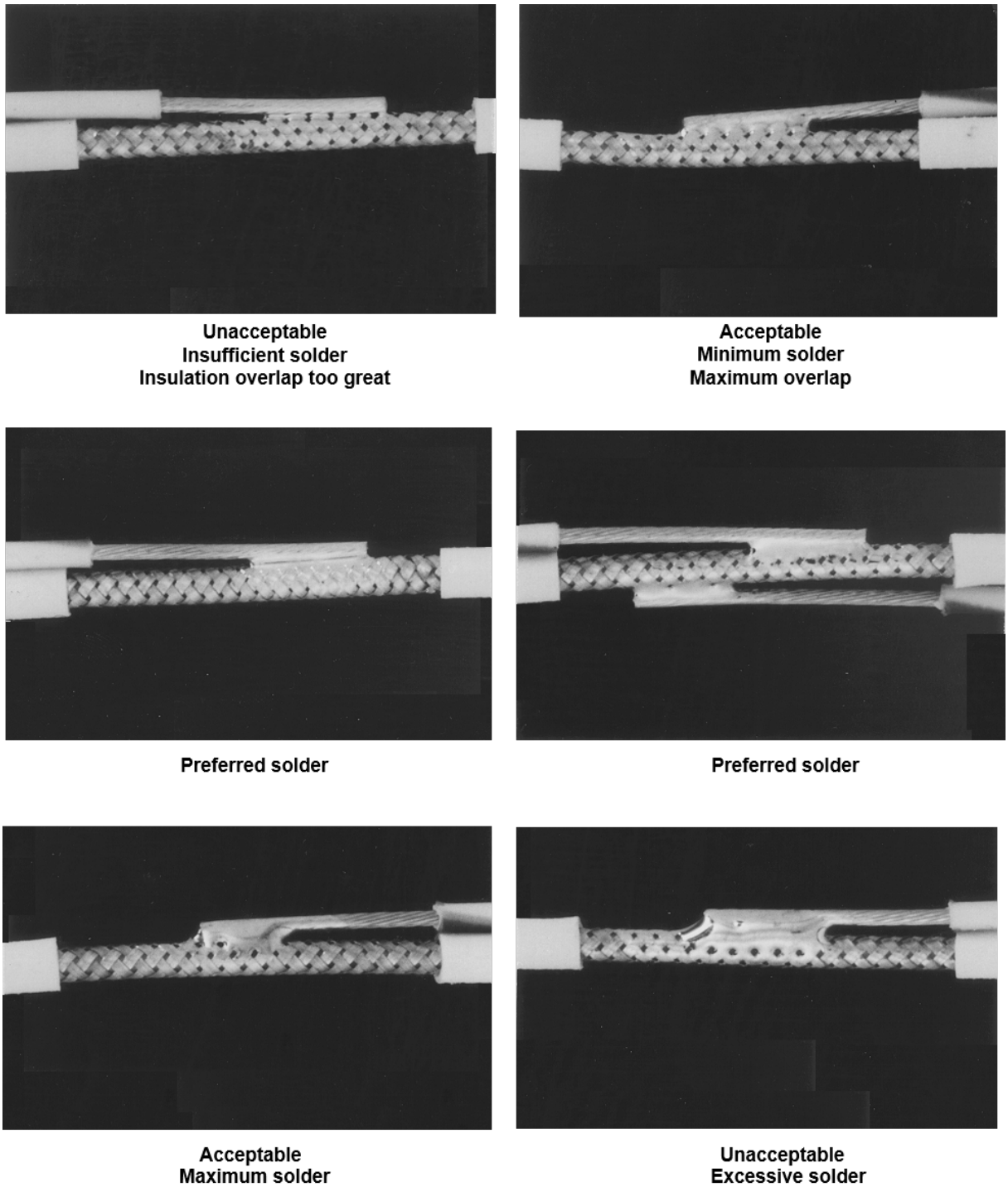
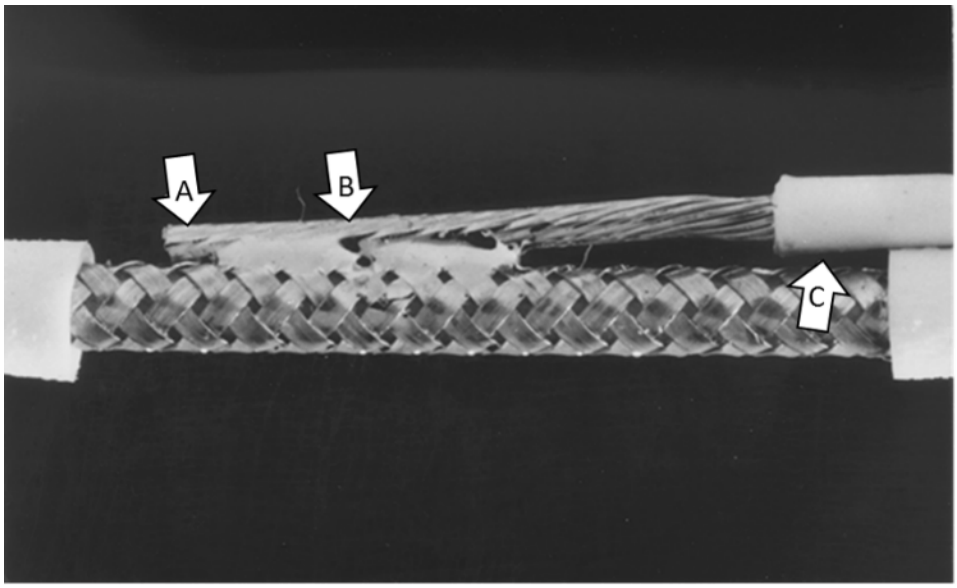


Figure E-8: Hand soldered wire to shielded cable interconnections



ECSS-Q-ST-70-61_1511125

Figure E-9: Hand soldered wire to shielded wire interconnections

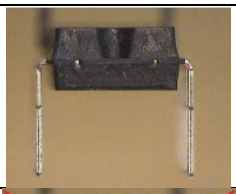
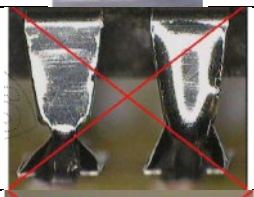


A= Unacceptable lack of solder between conductors
B = Acceptable maximum insulation overlap
C = Acceptable pit in solder fillet caused by weave of shield material

ECSS-Q-ST-70-61_1511126

Figure E-10: Hand soldered wire interconnections - details of defects

E.8 Assembly of Dual in Line Package

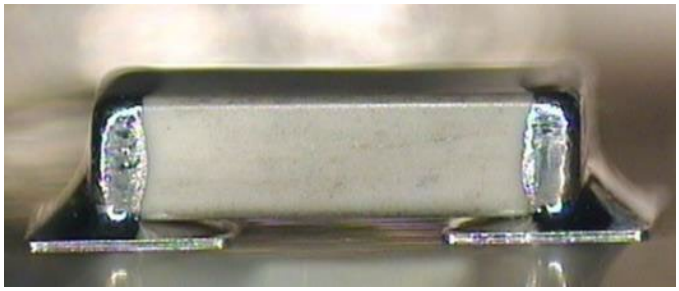
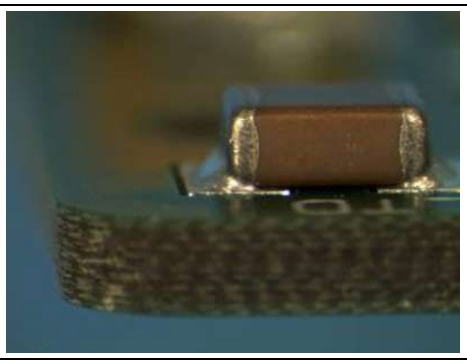
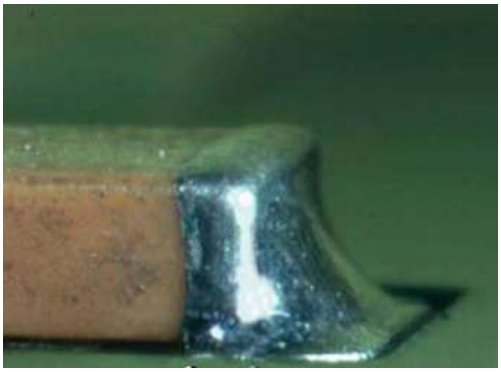
Component	Picture	Criteria
Vertical leads		Acceptable
		Unacceptable
No solder on tapered portion of leads		Acceptable
		Right termination is unacceptable
		Unacceptable

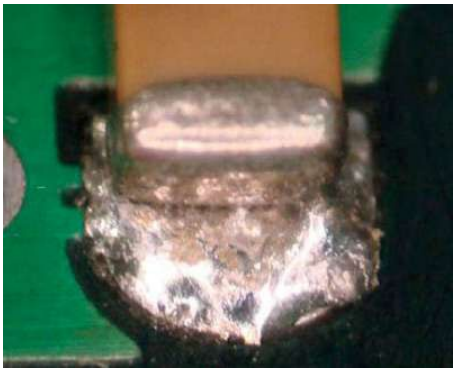
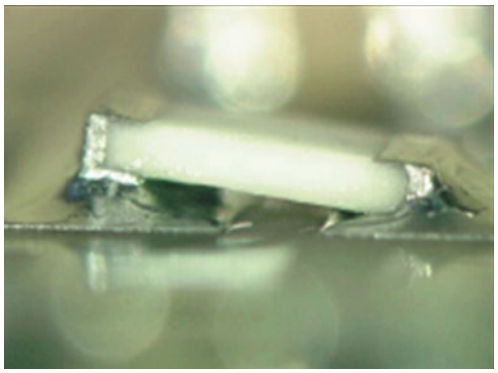
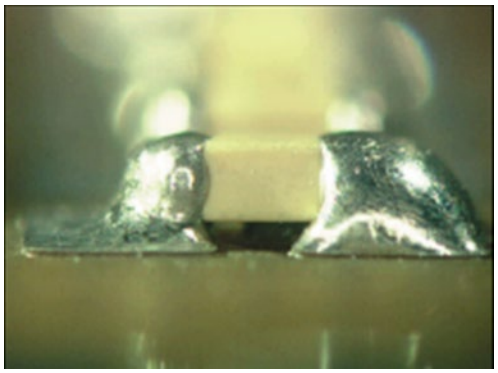
Annex F (informative) Visual and X-ray workmanship standards for SMDs

F.1 Workmanship illustrations for standard SMDs

F.1.1 Rectangular and square end-capped or end-metallized component with rectangular body

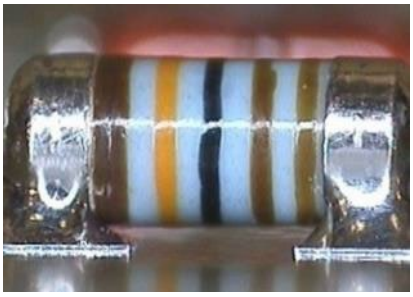
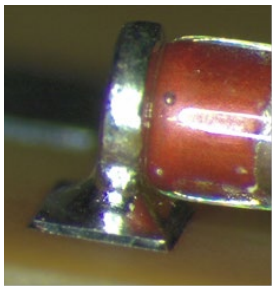
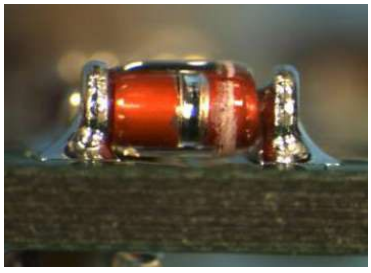
The following photos are provided as support material to the figures given in clause 10.4.2.

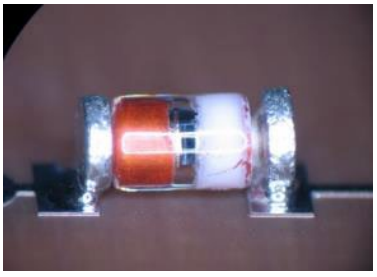
Criteria	Component	Picture
Preferred	Chip capacitor	
Acceptable (min)	Chip capacitor	
Acceptable (max)	Chip capacitor	

Criteria	Component	Picture	Comment
Unacceptable	Chip capacitor		No wetting
	Chip resistor		Excessive tilt
	Chip capacitor		Tombstone effect
	Chip capacitor		Excessive solder joint and asymmetry of solder joints

F.1.2 Cylindrical and square end-capped components with cylindrical body

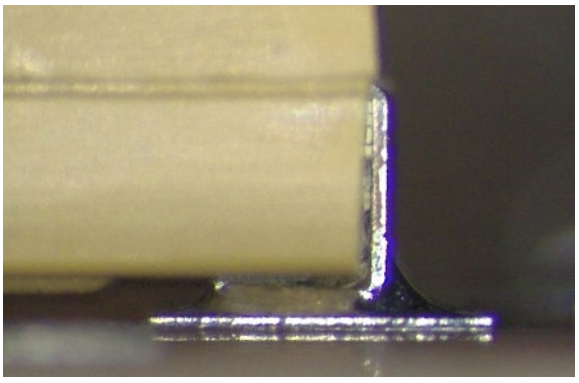
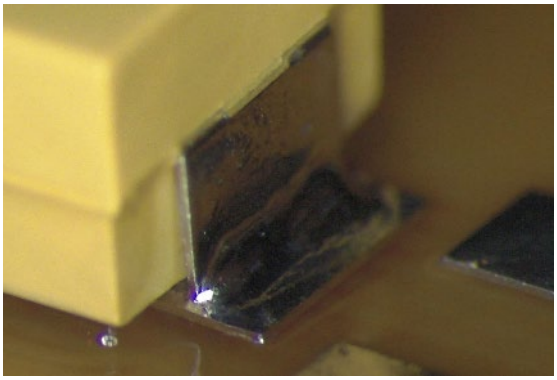
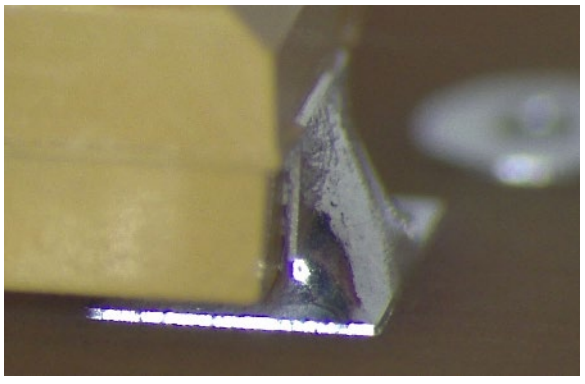
The following photos are provided as support material to the figures given in clause 10.4.3.

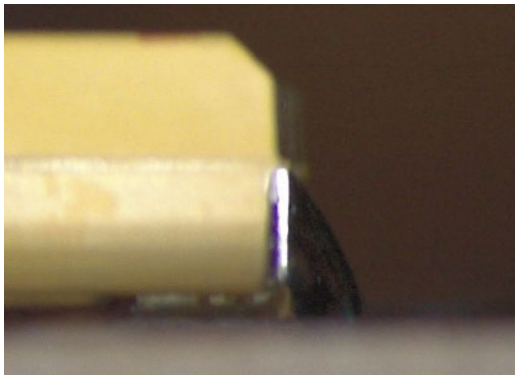
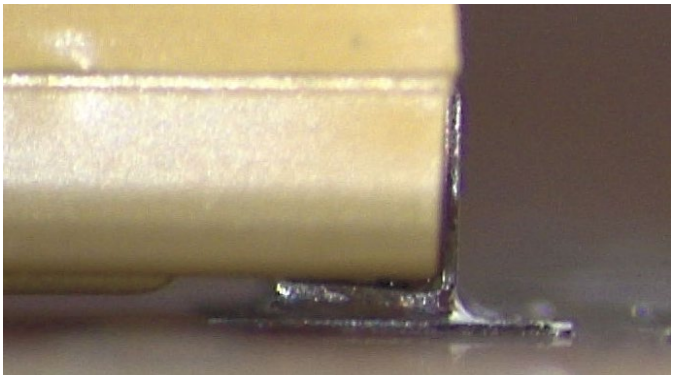
Criteria	Component	Picture
Preferred	MELF	
Acceptable (min)	MELF	
Acceptable (max)	MELF	

Criteria	Component	Picture	Comment
Unacceptable	MELF		Insufficient solder joint
	MELF		Excessive overhang

F.1.3 Component with Inward formed L-shaped leads

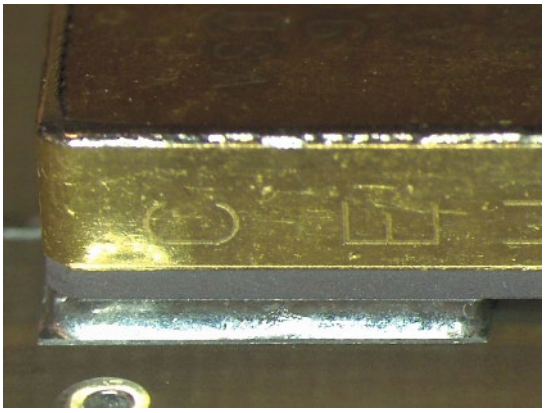
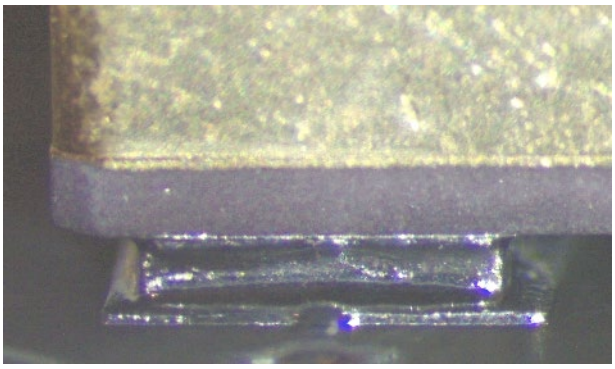
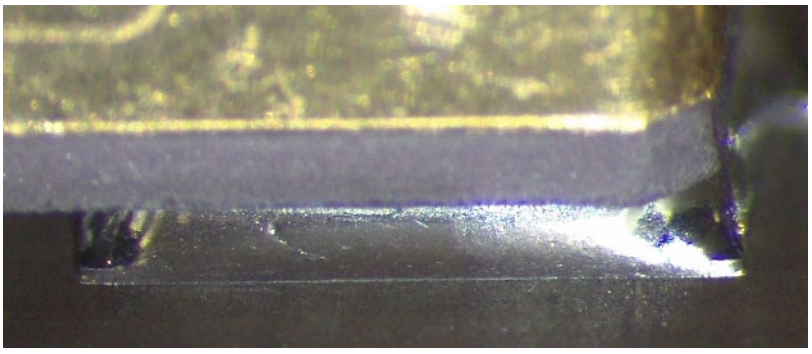
The following photos are provided as support material to the figures given in clause 10.4.5.

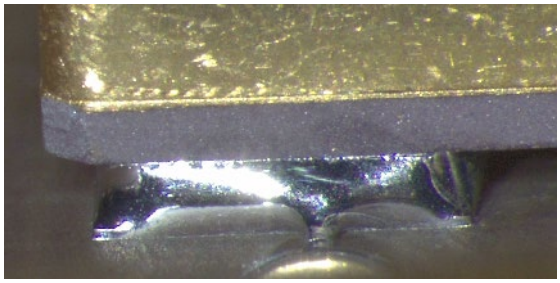
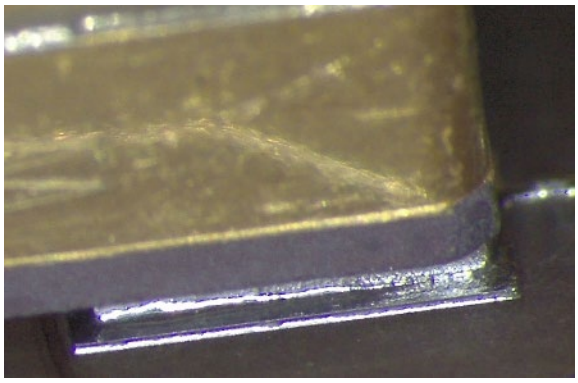
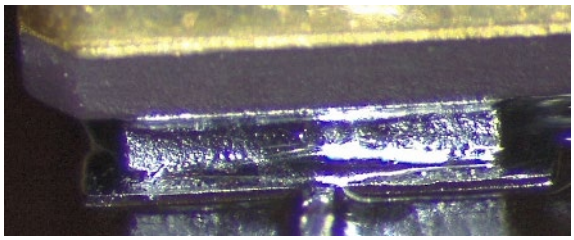
Criteria	Component	Picture
Preferred	Tantalum capacitor	
Acceptable (min)	Tantalum capacitor	 
Acceptable (max)	Tantalum capacitor	

Criteria	Component	Picture	Comment
Unacceptable	Tantalum capacitor		max
	Tantalum capacitor		min
	Tantalum capacitor		not adapted pad with associated insufficient solder fillet

F.1.4 Leadless component with plane termination

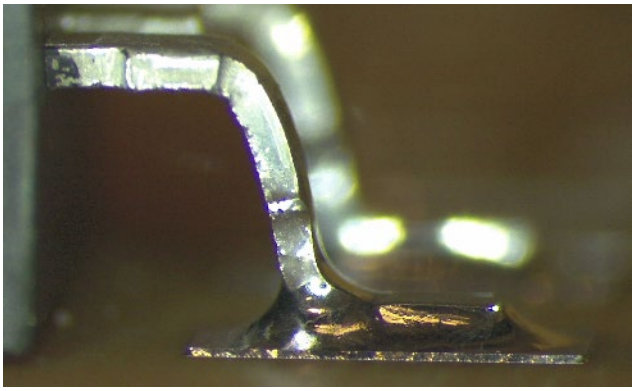
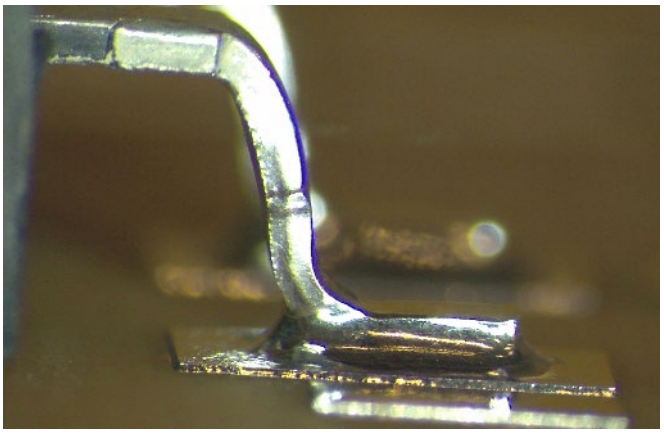
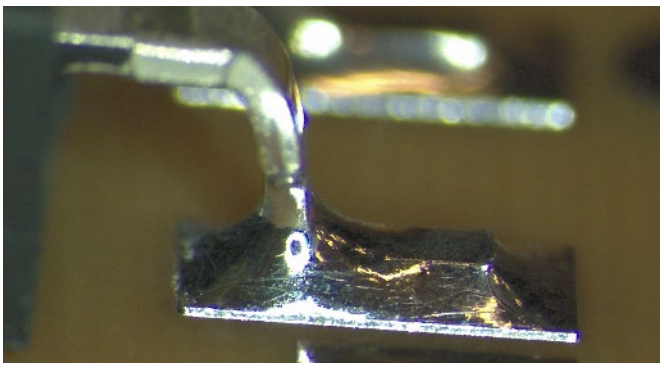
The following photos are provided as support material to the figures given in clause 10.4.6.

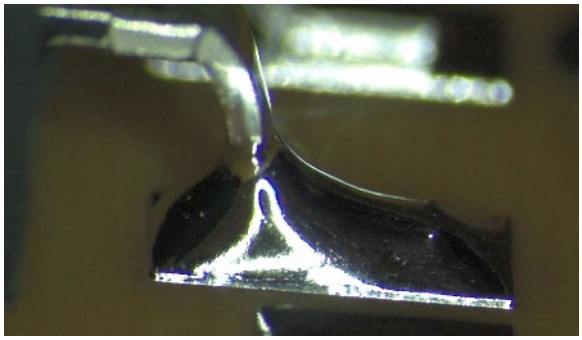
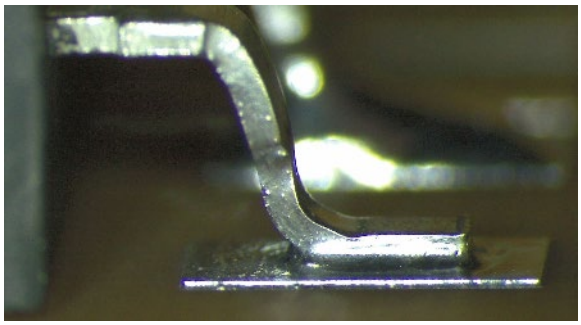
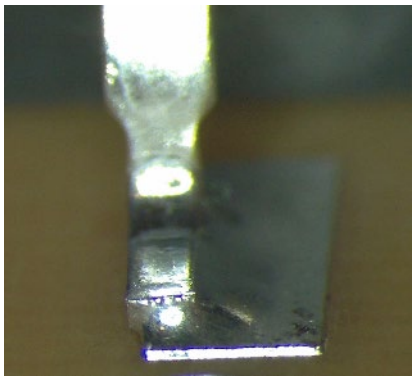
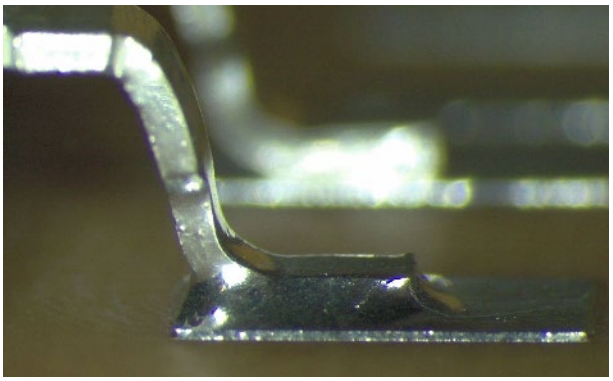
Criteria	Component	Picture
Preferred		
Acceptable (min)		
Acceptable (max)		

Criteria	Component	Picture	Comment
Unacceptable			max
			min
			

F.1.5 Leaded component with plane termination

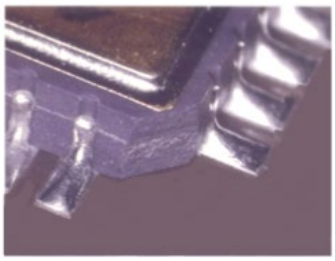
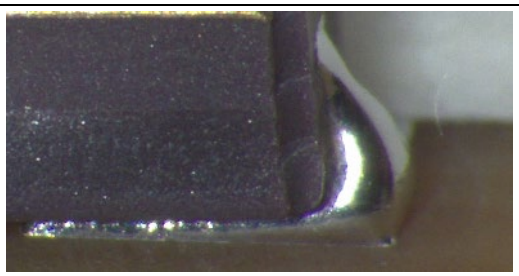
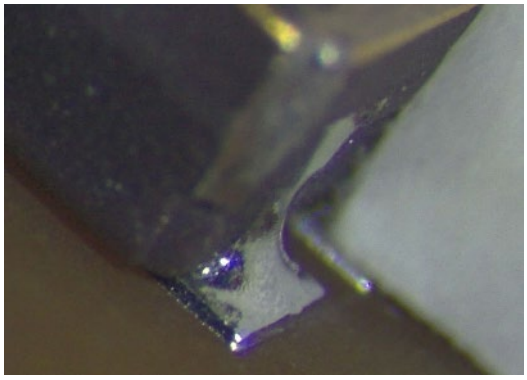
The following photos are provided as support material to the figures given in clause 10.4.7.

Criteria	Component	Picture
Preferred	D2Pack	
Acceptable (min)	D2Pack	
Acceptable (max)	D2Pack	

Criteria	Component	Picture	Comment
Unacceptable	D2Pack		Excessive solder
	D2Pack		Insufficient solder
	D2Pack		Excessive overhang
	D2Pack		Insufficient distance to footprint edge at heel

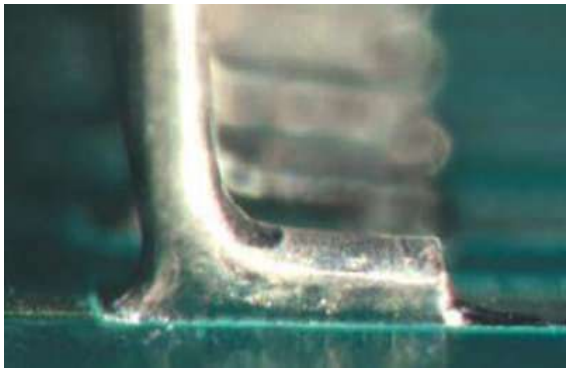
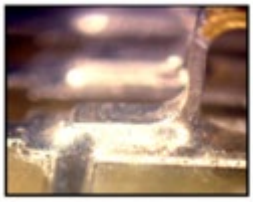
F.1.6 Leadless castellated ceramic chip carrier component

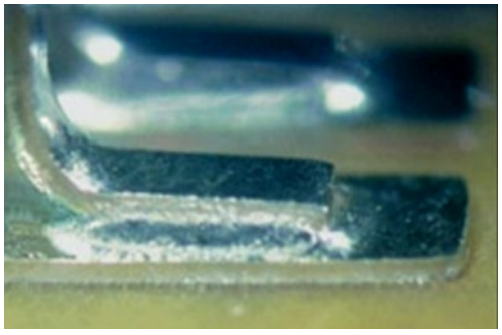
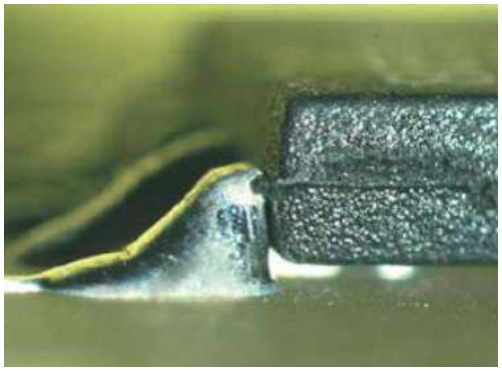
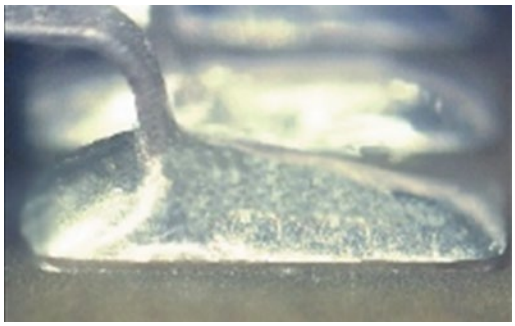
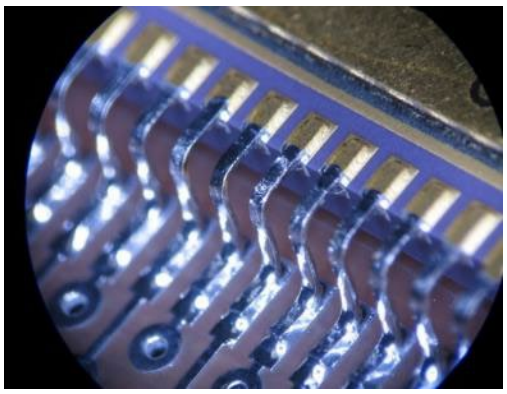
The following photos are provided as support material to the figures given in clause 10.4.8.

Criteria	Component	Picture	Comment
Preferred	LCCC	No photo available at this time	
Acceptable	LCCC		
Unacceptable	LCCC6		Excessive solder
	LCCC6		Insufficient solder
	LCCC6		Unacceptable overhang

F.1.7 Flat pack and Gull-wing leaded component with round, rectangular, ribbon leads

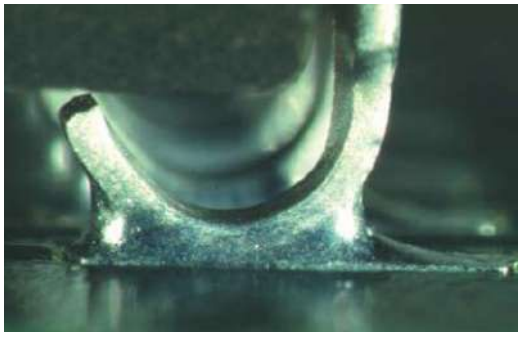
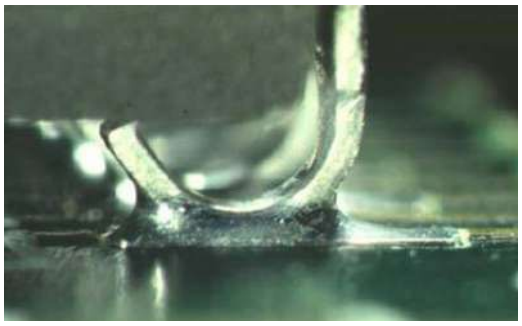
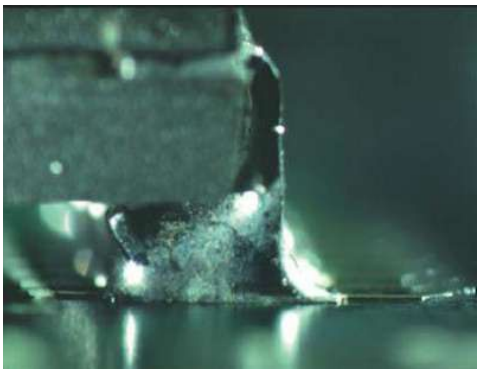
The following photos are provided as support material to the figures given in clause 10.4.10.

Criteria	Component	Picture
Preferred	Flat pack	
Acceptable (min)	Gull-wing package	
Acceptable (max)	Gull-wing package	 

Criteria	Component	Picture	Comment
Unacceptable			Insufficient heel fillet
			Excessive solder
			Excessive solder
	Flat pack		Excessing degoldin

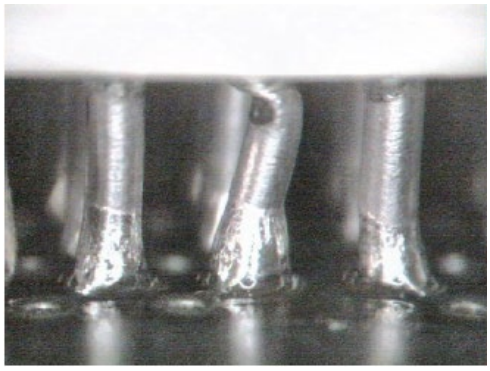
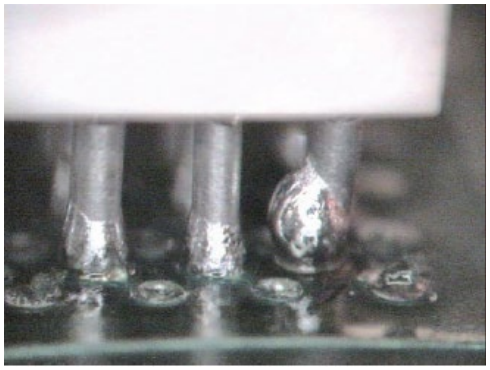
F.1.8 "J" leaded component

The following photos are provided as support material to the figures given in clause 10.4.11.

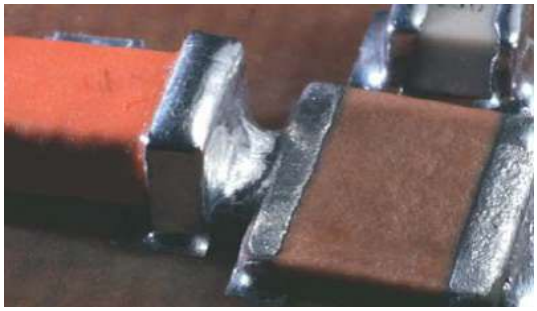
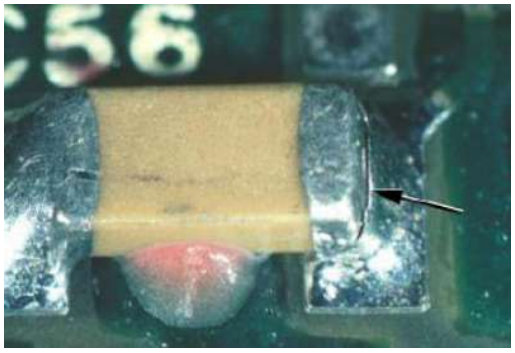
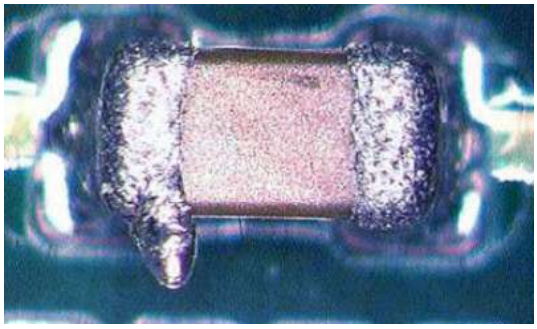
Criteria	Component	Picture	Comment
Preferred	"J" leaded package		
Acceptable (min)	"J" leaded package		
Acceptable (max)	"J" leaded package	No photo available at this time	
Unacceptable	"J" leaded package		Excessive solder joint

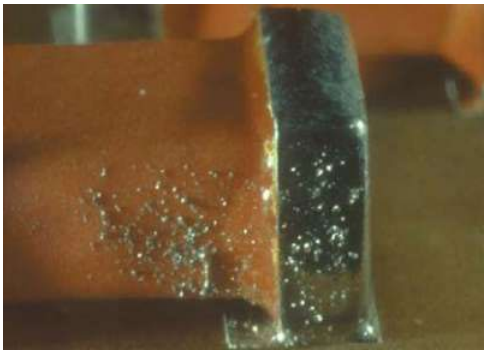
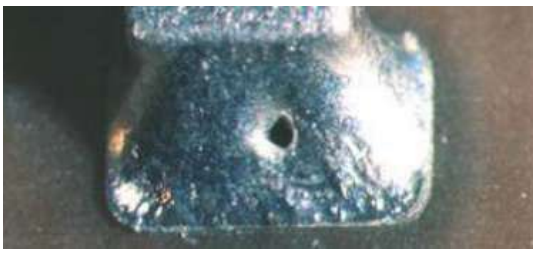
F.1.9 Area array components

The following photos are provided as support material to the figures given in clause 10.4.14.

Criteria	Component	Picture	Comment
Unacceptable	CCGA		Bent column
	CCGA		Excessive solder joint

F.1.10 Miscellaneous soldering defects

Criteria	Picture	Comment
Unacceptable		Solder bridge between terminals
		Melf misplacement and lack of insulation distance with other component
		Misplacement and fractured solder joint
		Icicle

Criteria	Picture	Comment
Unacceptable		Solder microballs
		Cold wetting
		Void bottom not visible

F.2 X Ray Workmanship illustrations for solder flow and voids

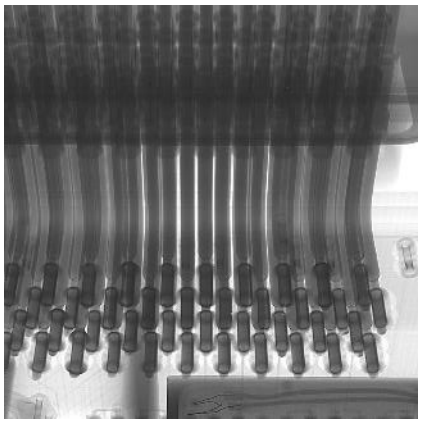
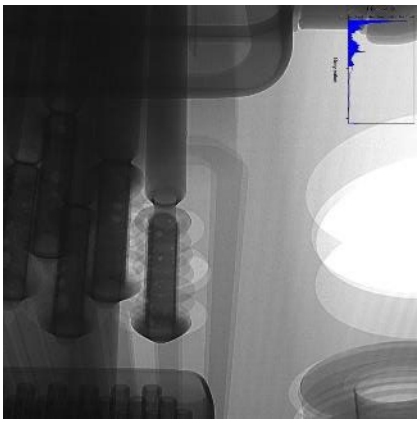
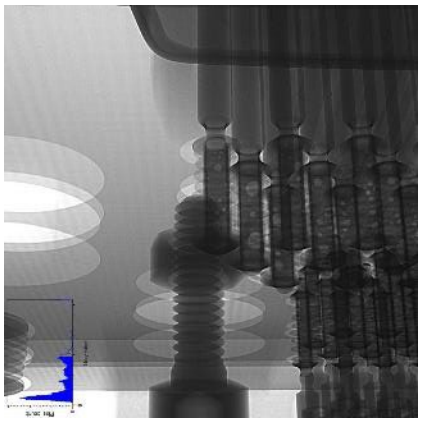
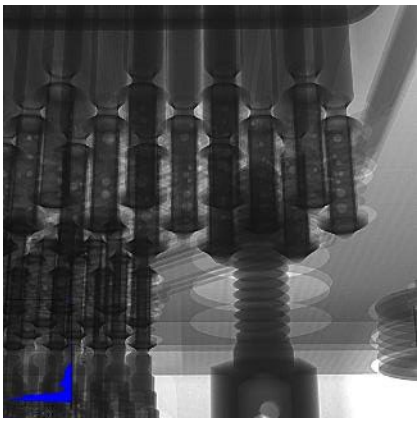
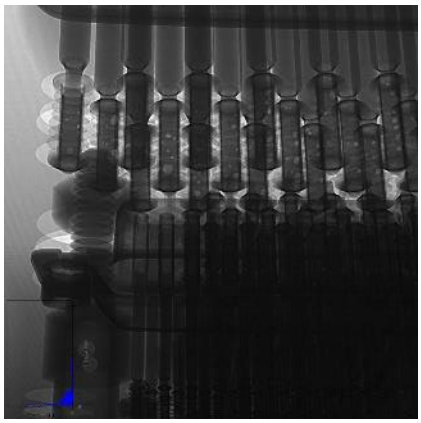
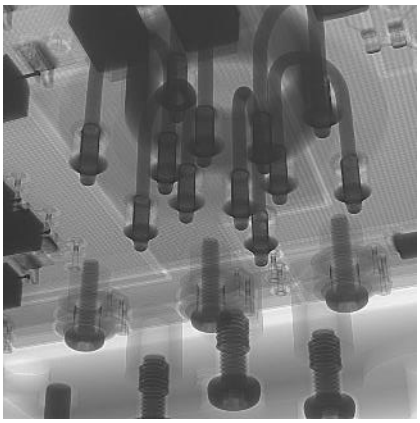
	
a) acceptable All 100% flow through, hardly any voids	b) acceptable Slightly below 100% flow through on the right pin, voids <<25%
	
c) acceptable Slightly below 100% flow through on the leftmost pin, voids <<25%	d) acceptable Slightly below 100% flow through on the third pin from right, voids <<25%
	
e) not acceptable 85% flow through on the first pin from left, voids <<25%	f) acceptable 100% flow through on all pins, voids <<25%

Figure F-1: Examples of acceptable and not acceptable solder flow through and maximum voids during X-ray

F.3 X Ray Workmanship illustrations for ball grid array devices

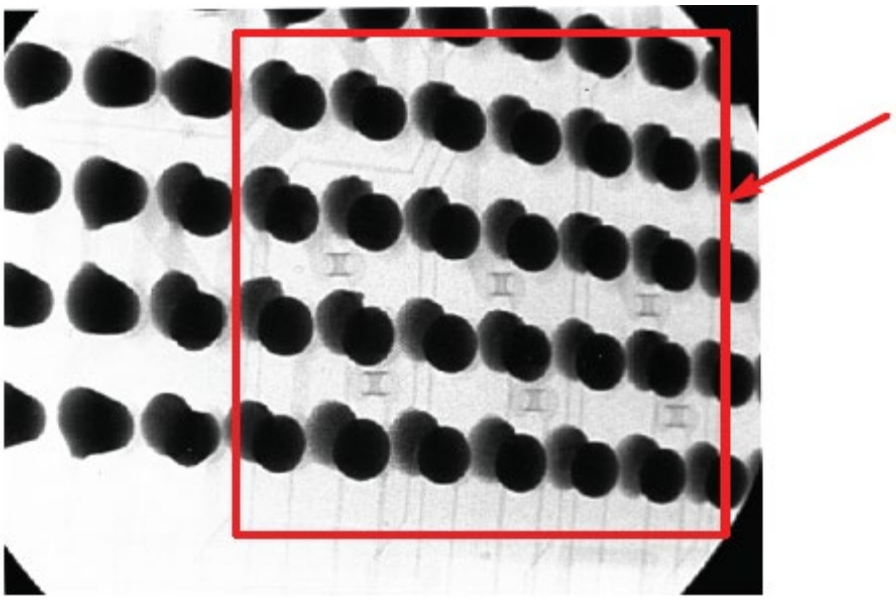
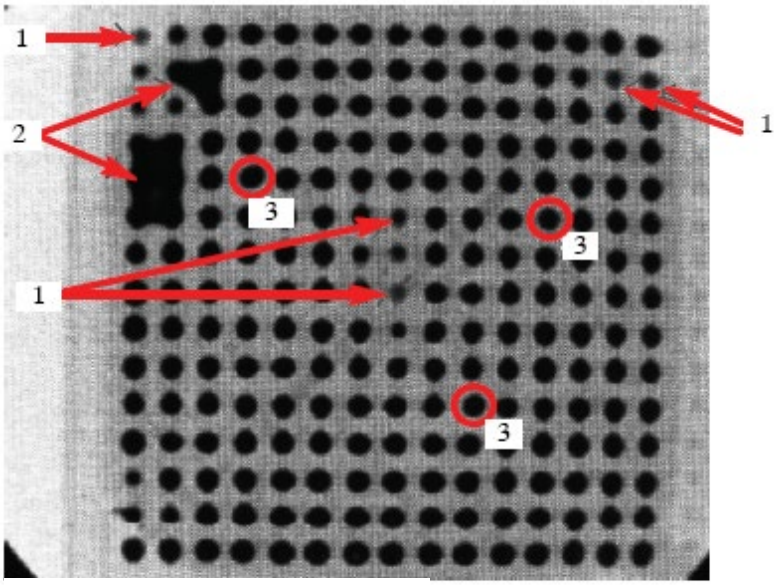
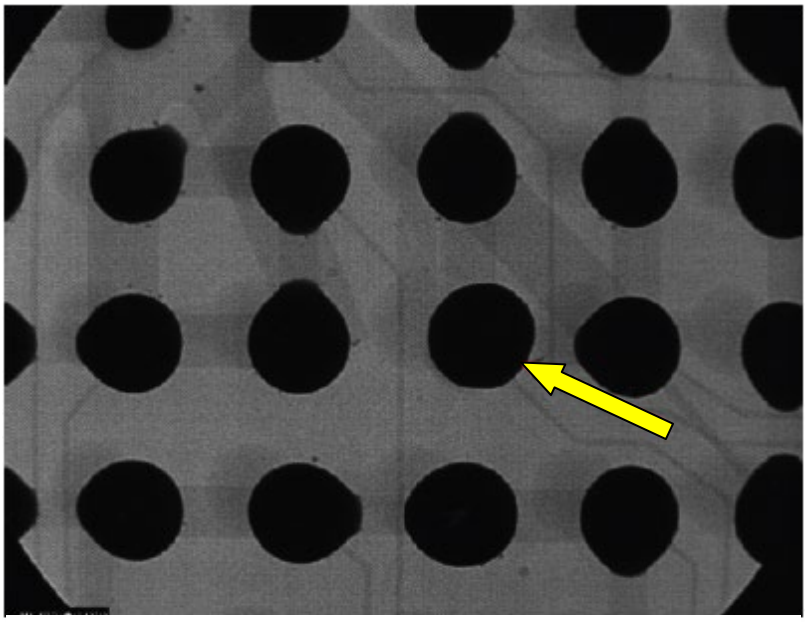


Figure F-2: Angled-transmission X-radiograph showing solder paste shadow due to partial reflow: Reject



1. missing balls: Reject
2. bridges: Reject
3. non-wetted pads: Reject

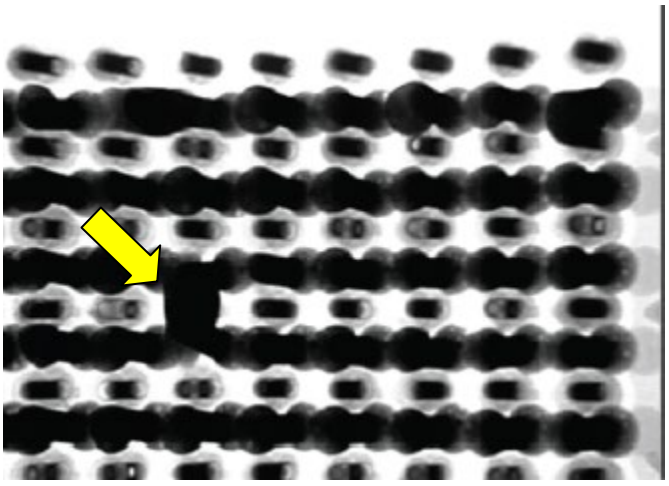
Figure F-3: Perpendicular transmission X-radiograph showing unacceptable defects



Solder has not flowed to extent of teardrop pad: Reject

Figure F-4: Perpendicular transmission X-radiograph showing non-wetted footprint

F.4 Workmanship illustrations for column grid array devices



:

Figure F-5: X-radiograph of CGA mounted on PCB showing solder bridge: Reject

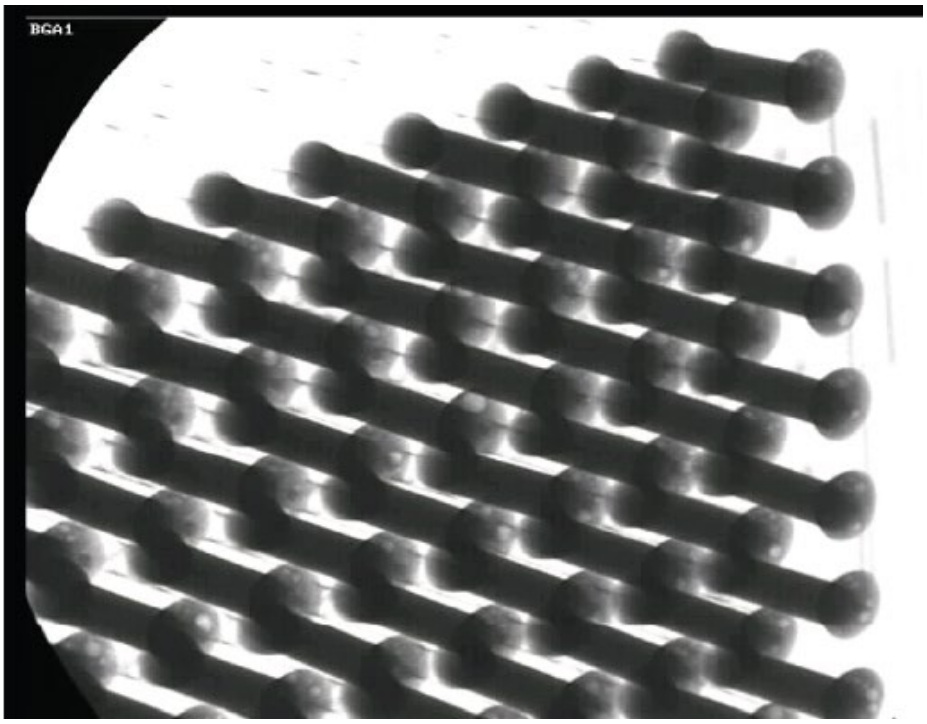


Figure F-6: X-radiograph of CGA showing solder fillets at base of columns: acceptable

Annex G (informative)
Example of an SMT audit report

ECSS-Q-ST-70-61C: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 1	**COMPANY DETAILS**				
1. NAME					
2. ADDRESS					
3. TEL					
4. EMAIL					
5. MANAGING DIRECTOR					
6. QUALITY MANAGER					
7. PRODUCTION MANAGER					
8. SMT CONTACT PERSON					
9. SMT PRODUCT RANGE AND HISTORY (brief summary)					
10. Numbers of SMT operators		Design Engineers		QA	

ECSS-Q-ST-70-61C Rev 1: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 2	**QUALITY SYSTEM**					
1. QUALITY MANUAL* Reference:						
Issue:						
Date:					Viewed	Y ☐ N ☐
2. ORGANISATION OF THE QUALITY DEPARTMENT FOR SMT						
3. INTERNAL QUALITY AUDIT SYSTEM Reference:						
Date of last audit:						
Comments:					Viewed	Y ☐ N ☐
4. NON-CONFORMANCE SYSTEM Reference:						
	No. of NCRs in previous 12 months:		No. open at audit date:		Viewed	Y ☐ N ☐
5. CURRENT QUALITY APPROVALS Date of last assessment						
6. COMMENT ON COMMITMENT TO ECSS-Q-ST-70-61						
7. REFERENCE TO GENERAL ESA AUDIT & Date						

* Note: Request that a copy of the Contents List of the Quality Manual be appended to this report (See Attachment 1).

ECSS-Q-ST-70-61C Rev.1: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 3	**PROCESS CONTROL**
1. SMT APPROVED (if any) Make reference to an existing list of SMT configurations considered already tested. Identify how the SMT was tested.	

2. Make reference to the procedures that have the following functions and identify current issue and date:	
Process Identification Document	
1. Process instructions	Viewed: Y ☐ N ☐
2. Workmanship acceptance/rejection criteria	Viewed: Y ☐ N ☐
3. Calibration of SMT tooling	Viewed: Y ☐ N ☐
4. Control of limited Shelf life materials	Viewed: Y ☐ N ☐
5. Material procurement control with CofC or CofTest	Viewed: Y ☐ N ☐

3. TRAINING Make reference to the procedure for operator and inspector training. Identify the number of certificated operators and inspectors.	Viewed:	Y ☐ N ☐	Certificates viewed:	Y ☐ N ☐

ECSS-Q-ST-70-61C Rev.1: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 4	**FACILITIES**
CHECK LIST	
Devices storage and kitting area.	
Humidity and temperature control	
ESD protection and control	
Cleanliness in assembly areas	
Calibration	ESD (floor, mat, chair, wrist, solder iron….):
	Degolding, pretinning bath:
	Lead forming:
	Machine reflow:
	Solder tip:
	Repair station:
	Ovens:
Lighting in Lux	Degolding:
	Pretinning:
	Lead forming:

	HS Assembly:
	Stacking, bonding:
	Conformal coating:
PCB drying ovens and procedure	Unpopulated:
	Populated without conformal coating:
	Populated with conformal coating:
Oven	Baking of naked PCB:
	Baking of populated PCB:
	Curing of adhesive:
	Curing of conformal coating:
	Repair prior conformal coating
	Repair after conformal coating:
Bending tools	
Magnification aids	Device preparation (degolding, pretinning, lead forming):
	After solder paste application:
	After assembly by machine reflow:
	During assembly by hand:
	Final inspection:
Degolding bath (250°C-280°C)	

Pretinning (210-260°C)	
Solder fluxes (internal and external) used. Flux activity and trademark.	Degolding, pretinning:
	Solder paste:
	Hand soldering:
Cleaning Solvents	PCB cleaning:
	Degolding, pretinning:
	Soldering by machine reflow:
	Solder screen
	Soldering by hand:
	Prior to bonding, stacking:
	Prior to conformal coating:
Solder alloys (chemical composition, supplier, trademark and associated flux	-Dispensing:
	Screen printing:
	HS:
Solder paste application	Stencil:
	Dispensing:
	Repair station:
Pick and place machine	
Machine reflow	
Is the soldering equipment well	Machine reflow:

controlled (temperature-time profile, speed control…). How is the temperature profile controlled on the FM?	Solder Iron:
Hand Soldering iron (280°C to 340°C max)	
Fume exhaust facilities	
Repair station	
Cleaning Equipment	Machine reflow
	Hand soldering:
Cleanliness Testing (< 1,6 µg/cm^2)	
Stacking, bonding compounds	
Refrigerators: check expiration dates for adhesives, conformal coatings	Solder paste:
	Adhesive:
	Conformal coating:
Conformal Coating used	Curing conditions:
Cleanliness in conformal coating facilities	
Areas for Non-Conforming Items (Quarantine)	
Laboratories exist for: - Temperature cycling - Vibration	

- Electrical testing - Microsectioning	
SMT Assembly Traveller (operator activities, inspector stamps)	

END OF SECTION 4

ECSS-Q-ST-70-61C: SURFACE MOUNT TECHNOLOGY PROCESS AUDIT REPORT

SECTION 5 FINAL ASSESSMENT

AN ASSESSMENT OF THE SURFACE MOUNT TECHNOLOGY LINE AT THE FOLLOWING SUPPLIERS FACILITY HAS BEEN UNDERTAKEN AND THE FOLLOWING CONCLUSIONS MADE:

Supplier:
Address:

THE FACILITIES FOR THE ASSEMBLY OF SURFACE MOUNT TECHNOLOGY (ACCORDING TO ECCS-Q-ST-70-61C AT THE ABOVE SUPPLIER'S SITE ARE CONSIDERED:

SUITABLE CONDITIONALLY SUITABLE NOT SUITABLE

SUMMARY OF FINDINGS/CONDITIONS OF APPROVAL/SUMMARY OF CORRECTIVE ACTIONS NECESSARY:

Actions	Findings	Due date

NAME SIGN

PROCESS ASSESSMENT CARRIED OUT BY (Approval Authority):

IN PRESENCE OF (CONTRACTOR):

DATE:

Approval Authority: DATE:

END OF DOCUMENT

Annex H (informative) Solder Alloys melting temperatures and choice

H.1 Melting temperatures and choice

Table H-1: Guide for choice of solder type

Solder type	Melting range (°C)		Uses
	Solidus	Liquidus	
63 tin solder (eutectic)	183	183	Soldering printed circuit boards where temperature limitations are critical and in applications with an extremely short melting range. Preferred solder for surface mount components.
62 tin silver loaded	179	190	Soldering of terminations having silver metallization. This solder composition decreases the scavenging of silver surfaces.
60 tin solder	183	188	Soldering electrical wire/cable harnesses or terminal connections and for coating or pretinning metals.
96 tin silver (eutectic)	221	221	Can be used for special applications, such as soldering terminal posts.
75 indium lead	145	162	Special solder used for low temperature soldering process when soldering gold and gold-plated finishes. Can be used for cryogenic applications.
70 indium lead	165	175	For use when soldering gold and gold-plated finishes when impractical to degold.
50 indium lead	184	210	This solder has low gold leaching characteristic.

Bibliography

ECSS-S-ST-00	ECSS system - Description, implementation and general requirements
ECSS-E-ST-10-03	Space engineering - Testing
ECSS-E-HB-20-05	Space engineering - High voltage engineering and design handbook
ECSS-E-HB-32-25	Space engineering - Mechanical shock design and verification handbook
ANSI/ESD S20.20-2014	Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)
EIA-469 issue E	Standard Test Method for Destructive Physical Analysis (DPA)of Ceramic Monolithic CAPA
EN-IEC 61190-1-2	Attachment materials for electronic assembly - Part 1-2: Requirements for soldering pastes for high-quality interconnects in electronics assembly
EN-IEC 61190-1-3	Attachment materials for electronic assembly - Part 1-3: Requirements for electronic grade solder alloys and fluxed and non-fluxed solid solders for electronic soldering applications
EN-IEC 61340-5-2	Electrostatics - Part 5-2: Protection of electronic devices from electrostatic phenomena - User guide
ESA-TECMSP-MO-018961 (latest release)	Devices that have shown anomalies during assembly verification
ESA-TECMSP-MO-013161 (last release)	Procedure for approval of laboratories for microsectioning of electronic assemblies for ESA programmes
ESA TECMSP-MO-013162 (latest release)	Requirements for outsourcing laboratories performing microsectioning of electronic assemblies
ESA TECMSP-MO-013165	ESA recommended microsectioning facilities
ESA-TECQTM-MO-1931 Issue 3	Guideline for the review of Approval status of electronics assembly configurations during MPCB
MIL-PRF-28861	FILTERS: Filters, Radio Interference/Electromagnetic Interference Suppression
MIL-PRF-39003	CAPACITORS: Fixed, Tantalum, Electrolytic (Solid Electrolyte), Polarized, Established Reliability
MIL-PRF-39010	COILS: Coils, Fixed, Radio Frequency, Established Reliability
MIL-PRF-49470	CAPACITORS: Fixed, Ceramic Dielectric, Switch Mode Power Supply
MIL-PRF-83421	CAPACITORS: Fixed, Metallized, Plastic Film Dielectric, Hermetically Sealed, Established Reliability