ECSS-Q-ST-70-12C Rev.1 DIR1
30 October 2024

Space product assurance

Design rules for printed circuit boards

This document is distributed to the ECSS community for Public Review.
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Foreword

ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards. Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

This Standard has been prepared by the ECSS-Q-ST-70-12C Rev.1 Working Group, reviewed by the ECSS Executive Secretariat and approved by the ECSS Technical Authority.

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Next steps	
DIR + impl. DRRs	Draft with implemented DRRs
DIR + impl. DRRs	DRR Feedback (plus first DOORS test)
DIR + impl. DRRs +impl of comments	Implementation of comments from DRR Feedback and DOORS test conversion
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30 September 2024	Changes with respect to ECSS-Q-ST-70-12C (14 July 2024) are the following and identified in the document with revision tracking. Main changes are: • xxxxx • xxxx Detailed changes Added requirements: • xxxx Modified requirements: • xxxx Deleted requirements: • xxxx

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Introduction

PCBs are used for the mounting of electronic components to produce PCB assemblies that perform electrical functions. The PCBs are subjected to thermo-mechanical stress during assembly such as soldering of components, rework and repair under normal terrestrial conditions. In addition the assembled PCBs are exposed to the launch and space environment. The reliability of the circuit depends on the robustness of the design, among other factors. Moreover, PCB design with high technological complexity enables the use of complex components with advanced functionality.

1 Scope

This standard specifies the requirements for the supplier and PCB manufacturer for PCB design.

This standard is applicable for all types of PCBs, including sequential, rigid and flexible PCBs, HDI and RF PCBs.

This standard can be made applicable for other products combining mechanical and electrical functionality using additive or reductive manufacturing processes, as used in PCB manufacturing. Examples of such products are slip rings and bus bars.

This standard may be tailored for the specific characteristics and constraints of a space project in conformance with ECSS-S-ST-00.

2
Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revision of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the more recent editions of the normative documents indicated below. For undated references, the latest edition of the publication referred to applies.

ECSS-S-ST-00-01	ECSS system – Glossary of terms
ECSS-Q-ST-70-02	Space product assurance - Thermal vacuum outgassing test for the screening of space materials
ECSS-Q-ST-70-60	Space product assurance - Qualification and procurement of printed circuit boards
ECSS-Q-ST-70-61	Space product assurance – High reliability assembly for surface mount and through hole connections
ECSS-E-ST-20	Space engineering – Electrical and electronic
ECSS-E-ST-20-06	Space engineering - Spacecraft charging
IPC-2152, August 2009	Standard for determining current carrying capacity in printed board design
IPC-4101E, January 2017	Specification for base materials for rigid and multilayer printed boards
IPC-4562A, April 2008	Metal foil for printed wiring applications

3
Terms, definitions and abbreviated terms

3.1 Terms from other standards

For the purpose of this Standard, the terms and definitions from ECSS-S-ST-00-01 apply, and in particular for the following terms:

supplier

NOTE In the context of this standard the supplier is also responsible for the design of the PCB.

3.2 Terms specific to the present standard

3.2.1 annular ring

ring of copper pad surrounding the drilled hole

NOTE The measurement of annular ring is different on internal and external layers. See clause 10.6.1 from ECSS-Q-ST-70-60.

3.2.2 area array device (AAD)

surface mount package wherein the solder terminations are formed in a grid on the bottom of the package

NOTE BGA and CGA are specific types of AAD.

3.2.3 artwork

graphical representation of individual layers

NOTE Examples of artwork are: conductive layers, solder mask, silk screen, selective finishes, heat sink.

3.2.4 as-designed

state of the PCB in the design phase

NOTE This typically refers to dimensions associated with the designed PCB, which does not take into account manufacturing tolerances.

3.2.5 as-manufactured

state of the PCB after manufacturing

NOTE This typically refers to dimensions measured on the manufactured PCB, the final product. The

dimensions are measurements that include manufacturing tolerances.

3.2.6 as-manufactured hole

hole in as-manufactured PCB after all process steps

NOTE In case of a plated through-hole, an as-manufactured hole includes plating and surface finish.

3.2.7 aspect ratio

ratio of the as-designed thickness of the build-up and the diameter of the drilled hole

3.2.8 assembled PCB

PCB with all its electronic and mechanical components mounted, having undergone all the manufacturing operations

NOTE Examples of manufacturing operations are wiring, soldering, wire-bonding, gluing, screwing, potting and conformal coating.

3.2.9 assembly house

company performing assembly of PCB

3.2.10 back-drilled hole

via with part of its metallisation removed on one side by depth controlled mechanical drilling with a larger diameter drill

3.2.11 ball grid array (BGA)

surface mount package wherein the solder balls for terminations are formed in a grid on the bottom of the package

NOTE BGA is a specific type of AAD.

3.2.12 basic copper

copper foil layer that excludes etching and plating steps

3.2.13 blind via

type of via exposed only on one side of the PCB

NOTE One method to manufacture a blind via can be by depth controlled drilling. A second method can be by sequential lamination of minimum 2 half-stacks. See Figure 3-2.

3.2.14 bondply

type of cover layer with adhesive on both sides for the purpose of bonding flex laminate

NOTE Bondply is a trademark manufactured by DuPont.

3.2.15 build-up

technical representation of individual conductive layers and dielectric materials of the specific PCB design

NOTE Examples of a build-up are given in Figure 3-1 and Figure A-4

3.2.16 buried via

type of via connecting internal layers without being exposed on either surface

NOTE See Figure 3-2.

3.2.17 column grid array (CGA)

surface mount package wherein the columns for terminations are formed in a grid on the bottom of a package

NOTE CGA is a specific type of AAD.

3.2.18 conductive layer

electrically conductive parts of a PCB on the same layer

NOTE The conductive layer can contain tracks, planes or pads.

3.2.19 conductor

conductive elements within the PCB

NOTE Elements within the conductive layer and vias are conductors.

3.2.20 core via

type of buried via in the core of an HDI PCB

NOTE Examples of via types are shown in Figure 3-2.

3.2.21 critical net

conductive circuit with a specific functionality that requires redundant solutions to avoid loss of functionality in case of any credible single failure

NOTE Redundant solutions can be double insulation, increased copper cross section, multiple vias.

3.2.22 critical track

track that is part of a critical net

3.2.23 double insulation

barrier between tracks or elements of an electronic circuit that provides insulation of tracks or elements of an electronic circuit in case of any credible single failure

3.2.24 drilled hole

hole after drilling and before plating

NOTE In case of a plated through-hole, drilled hole excludes plating and surface finish

3.2.25 electrical field

voltage per insulation distance between two conductors

NOTE This is a simplified representation of electrical field applicable for PCB design.

3.2.26 fine pitch

spacing of tracks or pads that is more dense than for normal pitch

NOTE The exact perimeter of fine pitch on external and internal layers is described in clause 7.4.

3.2.27 FR4

type of laminate and prepreg with a specific epoxy resin

3.2.28 half-stack

sequence of laminated layers that are included in further lamination sequences to form the finished PCB

3.2.29 heat sink

layer of thick metal with the purpose of thermal dissipation internal or external of the PCB

NOTE Term “thermal drain” is synonymous with the word “heat sink”.

3.2.30 high density interconnect (HDI)

technology on PCB related to the pattern that allows a smaller pitch in the footprint on the surface pattern and a higher density of internal signal routing than for conventional PCBs

NOTE 1 The exact perimeter of HDI technology is described in clause 11.

NOTE 2 This technology can be required for assembly of AAD.

NOTE 3 An example of HDI build-up is shown in Figure 3-1.

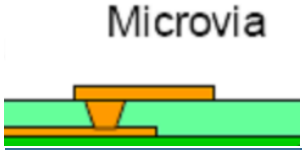


Figure 3-1: Simplified build-up of HDI PCB

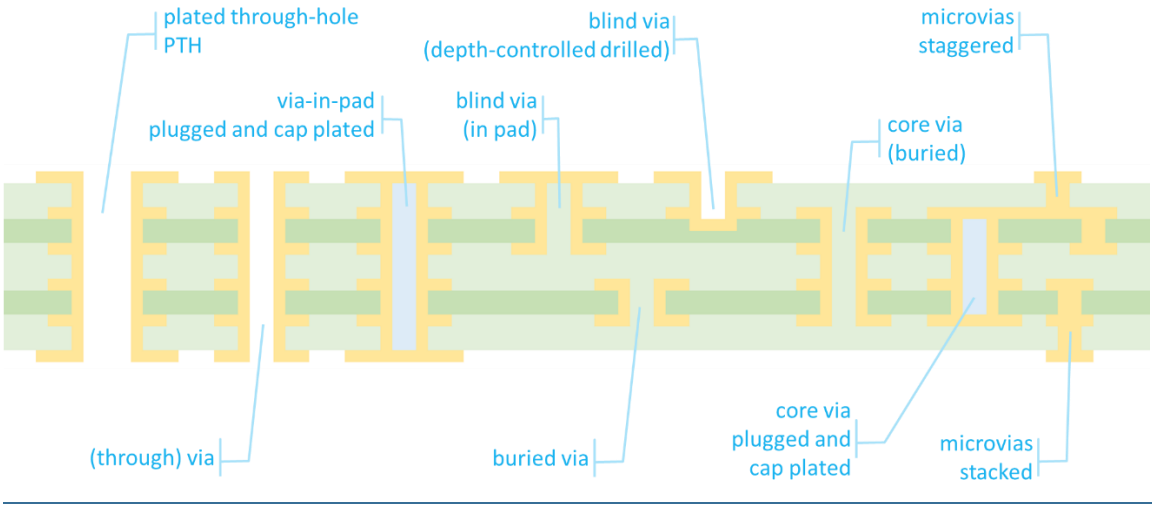


Figure 3-2: Via types

3.2.31 high speed signal

electronic functionality that requires specific design precautions to maintain time dependant signal integrity

NOTE This is further specified in IPC-2251 and IPC-2141A.

3.2.32 hole wall pull away

adhesion defect between copper of the hole wall and resin

3.2.33 HTE

grade of copper foil with the grade designation “high temperature elongation electrodeposited”

NOTE This is specified in IPC-4562A.

3.2.34 intralayer

within the same layer in X,Y direction

3.2.35 interlayer

in between two superpositioned layers in Z direction

3.2.36 JTC

grade of copper foil

NOTE This grade of copper foil is produced by GOULD Electronics GmbH.

3.2.37 laminate

sheets of fully cured, C-stage, resin with copper cladding

NOTE Rigid laminate includes reinforcement, for example by woven glass fibres or non-woven aramid fibres.

3.2.38 landing pad

internal pad of microvia

3.2.39 microvia

blind via manufactured with a diameter smaller than 250 µm

NOTE 1 Microvias are required for routing internal signals in HDI PCBs.

NOTE 2 Example of microvia configuration is shown in Figure 3-1 and Figure 3-2.

NOTE 3 Microvias are drilled by laser ablation.

3.2.40 microvia layers

layers of conductive pattern that contain microvias

NOTE 1 Microvia layers are layers 1 and 2 and opposite layers.

NOTE 2 A full microvia layer is laminated sequentially using copper foil and prepreg, before laser drilling the microvia. A half microvia layer is not separately laminated. Instead, the laser drilling of the microvia occurs in the first dielectric layer of the core PCB. The layer 2 of the core PCB is copper foil that is usually not plated. See Figure 3-3 for an example of full and half microvia layers.

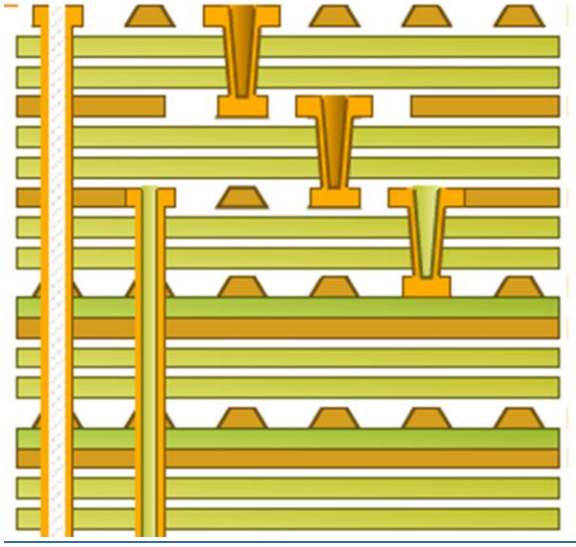


Figure 3-3: Example of build-up with two full and one half microvia layer.

3.2.41 mil

unit of length equal to 25,4 μm

NOTE The unit mil is in some cases customary in PCB design and therefore preferred above the SI unit.

3.2.42 no-flow prepreg

type of prepreg that has a reduced flow of resin during press cycle

NOTE The term "low-flow prepreg" is synonymous with the word "no-flow prepreg". The terms do not specify the exact amount of flow.

3.2.43 non-functional pad

pad on internal copper layer without electrical connection

3.2.44 non-plated hole

hole in a PCB that does not contain plating or other type of conductive reinforcement

3.2.45 normal pitch

standard spacing of tracks and pads

NOTE See "fine pitch" for another category of pitch.

3.2.46 number of layers

number of layers in a PCB containing conductive elements

NOTE For example, the numbering convention is from top to bottom layer: L1, L2, …,Ln-1, Ln.

3.2.47 panel

area of laminated layers that contains PCBs and coupons processed as a single unit

3.2.48 PCB manufacturer

entity that manufactures the PCB

3.2.49 peelable

areas of photo resist or copper that have poor adhesion to underlying substrate because of a tapered shape with a narrow dimension on one end

3.2.50 plated through-holes (PTH)

metal-plated holes drilled through all the layers used for assembly of components

NOTE Examples of via types are shown in Figure 3-2.

3.2.51 printed circuit board (PCB)

product resulting from the process of selectively etching unwanted copper from surfaces of copper clad insulating substrates to form a desired circuitry pattern which is metal-plated and laminated

NOTE Examples of specific PCB technologies are rigid, flexible, rigid-flex, double sided, multilayer, sequential, RF and HDI PCBs

3.2.52 prepreg

sheets of partly cured, B-stage, resin with reinforcement

NOTE Examples of reinforcement are woven glass fibres and non-woven aramid fibres.

3.2.53 RF elements

conductive pattern on PCB with specific RF functionality

NOTE For example filters, combiners, splitters, couplers. RF elements do not have voltage ratings or solder connections.

3.2.54 resin starvation

region in a PCB that has an insufficient amount of resin to wet out completely the reinforcement

NOTE This is shown by low gloss, dry spots or exposed fibres.

3.2.55 review item

design feature to be included into the PCB definition dossier and reviewed during the PCB design review

3.2.56 projected peak-to-peak insulation distance

worst-case minimum thickness of dielectric material that includes thickness tolerance of the laminate core and the maximum roughness of copper surface treatment

NOTE Figure 3-4 specifies how this is measured.

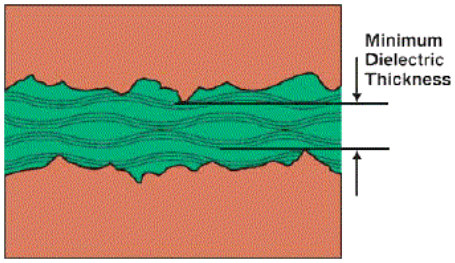


Figure 3-4: Projected peak-to-peak insulation distance

3.2.57 serialization

process of numbering of each unique PCB by the PCB manufacturer for traceability

3.2.58 sliver

pieces of photo resist or copper that have poor adhesion to underlying substrate because of the small surface area.

NOTE For example, a surface area below 0,01 mm^2

3.2.59 soldering pad

conductive part intended for soldering components on the PCB

3.2.60 spacing

insulation distance

NOTE The term "gap" is synonymous with the word "spacing", but this term is not used in the present standard.

3.2.61 stack

assembly comprising of one sequence of laminated layers

NOTE Half-stack identifies the sub-assembly.

3.2.62 test pad

pad that is dedicated for electrical testing on the PCB

3.2.63 track

conductive part routing the electrical connection between the pads

NOTE The term "line" and the term "conductive track" are synonyms with the word "track"

3.2.64 via

metal-plated hole drilled through all layers, only used for interconnection between layers

NOTE A via is not used for assembly. Examples of via types are shown in Figure 3-2.

3.2.65 X,Y direction

orientation in the plane of the PCB, along length and width of the PCB

3.2.66 Z direction

orientation perpendicular to the plane of the PCB, along height of the PCB

3.3 Abbreviated terms

For the purpose of this Standard, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
AAD	area array device
AC	alternating current
AOI	automated optical inspection
BGA	ball grid array
CAD	computer aided design
CAE	computer aided engineering
CGA	column grid array
CIC	Copper – Invar - Copper
CoC	certificate of conformance
CRC	cyclic redundancy check
CTE	coefficient of thermal expansion
Cu	copper (element)
DC	direct current
DRD	document requirements definition
DWV	dielectric withstanding voltage
GND	electrical signal to ground
EMC	electromagnetic compatibility
FAI	first article inspection
FP	flat pack
FR4	type of epoxy resin for PCBs
HDI	high density interconnect
i.a.w.	in accordance with
I/O	input/output
LCC	leadless chip carrier
LF	low frequency
MRR	manufacturing readiness review
PCB	printed circuit board
PID	process identification document
ppm	parts per million (10^{-6})
PTH	plated through hole
PTFE	polytetrafluoroethylene
QFP	quad flat pack
RF	radio frequency (high frequency)

Abbreviation	Meaning
SOIC	small outline integrated circuits
SPF	single point failure
sq	square (in unit Ω/sq)
TDR	time domain reflectometry
Tg	temperature of glass transition
Th	thickness
Vcc	power supply voltage
Vrms	voltage root mean square

4
Principles

4.1 Qualified PCBs

The conditions of qualification of PCB technology are described in 5.1a of ECSS-Q-ST-70-60.

PA requirements of space projects use this standard as applicable document. Based on their heritage, suppliers can propose the re-use of existing PCB designs that are "recurrent" and that are not in compliance with all design requirements of this standard. The possible acceptability of those cases is reviewed by the project on case by case basis. The PCB design is "recurrent" only when no changes are made in the artwork, routing, lay-out, build-up, material selection.

4.2 Manufacturing tolerances

Dimensional measurements of PCBs are "as-designed" except when explicitly mentioned "as-manufactured".

Design values are affected by the manufacturing tolerances. The minimum value on the PCB as-manufactured equals the design value subtracted with the manufacturing tolerance. See definition of terms in clause 3.2.

4.3 Reliability of design

Specific design features of PCBs are recorded as Review Items in the PCB definition dossier. This is done when the design features include a higher technological complexity that can affect manufacturability or (thermal) reliability. These design features are specifically evaluated by qualification prior to inclusion in the PID.

Requirements in this standard generally state minimum dimensions permitted. It is good practice to use minimum dimensions only when necessary to achieve the desired functionality and to design with margin when possible. For instance, it is recommended to implement minimum insulation distance between tracks only when space limitations prevent larger insulation distance. It is recommended to implement fan out of tracks which allows for larger insulation distances where more space is available.

The robustness of the PCB can be affected when combining multiple design features at the limit of the requirement or recorded as Review Item. The PCB manufacturer and the supplier evaluate this risk during the design review and provide formal approval during the MRR. The reliability of the manufactured PCB is evaluated by inspection on representative coupons.

5
Design review and MRR

5.1 Overview

This clause specifies the iterative process of designing a PCB in collaboration with the PCB manufacturer and specifies associated documentation for the formal authorization for manufacture.

5.2 Documentation

ECSS-Q-ST-70-12_1200001

a. The supplier shall issue the PCB definition dossier in conformance with the DRD in Annex A.

ECSS-Q-ST-70-12_1200002

b. The supplier shall list design features as Review Items in conformance with clause A.2.1<7> from the DRD of the Annex A.

ECSS-Q-ST-70-12_1200374

c. The supplier may list other design features as Review Items .

ECSS-Q-ST-70-12_1200003

d. The supplier shall submit the PCB definition dossier to the PCB manufacturer for the design review.

ECSS-Q-ST-70-12_1200375

e. The supplier should submit to the PCB manufacturer the draft PCB definition dossier or a list of specific Review Items specified in the requirement 5.2b in the design phase, when those Review Items are at the limit of the PID capability.

NOTE 1 HDI technology is an example of PCB design that is at the limit of the PID capability.

NOTE 2 Examples of Review Items that can be on the limit of PID capability are: dimensions, number of layers, maximum aspect ratio, number of sequences, material selection or a combination of these. Consultation with PCB manufacturer at this early design stage is recommended to avoid unnecessary risks. Multiple iterations can be

performed to achieve an agreed PCB definition dossier.

ECSS-Q-ST-70-12_1200004

f. The PCB manufacturer shall review the PCB definition dossier including Review Items for compliance with the PID.

ECSS-Q-ST-70-12_1200376

g. As a result of the design review, the PCB manufacturer may identify to the supplier additional Review Items in the PCB definition dossier.

NOTE Review Items can exist for PCB designs even within the capability of the PID. These Review Items and methods to mitigate them are specified in this standard as best practices and recommendations.

ECSS-Q-ST-70-12_1200005

h. The PCB manufacturer shall provide the PCB manufacturing dossier in conformance with DRD in the Annex B.

ECSS-Q-ST-70-12_1200006

i. The PCB manufacturer shall issue to the supplier a MRR checklist, which is part of the PCB manufacturing dossier, in conformance with the DRD in the Annex B.

NOTE An example of a MRR checklist is given in Annex G.

ECSS-Q-ST-70-12_1200007

j. During the MRR, supplier and PCB manufacturer shall approve the PCB manufacturing dossier, the PCB definition dossier and all Review Items.

NOTE The approvals are recorded in the MRR checklist.

ECSS-Q-ST-70-12_1200008

k. The MRR shall provide authorisation for manufacture to the PCB manufacturer, except the case specified in 5.2l.

l. An MRR need not to be performed in case the following conditions are met:

1. the PCB part number is recurrent,
2. an MRR was signed for the initial procurement with risk rating ≤ 2,
3. no change occurred in the definition dossier and PID,
4. it is accepted by customer and PCB manufacturer.

6
General design and production requirements

6.1 Reliability of design

ECSS-Q-ST-70-12_1200009

a. The supplier shall design the PCB with margin.

NOTE This is also described in clause 4.3.

6.2 Choice of materials and build-up

6.2.1 Overview

For the selection of materials for PCB a number of physical properties are important, such as Tg, Young's modulus, dielectric constant, CTE, hygroscopy. Table 6-1 provides an overview of some commonly used materials and their physical properties. The CTE of the as-manufactured PCB depends on the total copper thickness, which has a CTE of about 16 ppm/K.

It is important that for the selection of the technology for the PCB design the following is taken into account:

- CTE mismatch between devices and PCB,
- moisture sensitivity of PCB function,
- interconnection constraints,
- lay-out constraints.

Rigid-flex boards can be preferred to reduce the interconnection constraints.

Polyimide and epoxy are the most commonly used materials. Polyimide has an advantage over epoxy because it is more thermally stable and outperforms epoxy in thermal cycling and assembly. At the same time, polyimide is more hygroscopic than epoxy, which affects PCB ground use and assembly. Epoxy is available with different glass transition temperatures (Tg). Higher glass transition temperature is recommended for epoxy because it provides better thermal stability. Thermal expansion of resin in Z direction below and above Tg is typically higher than expansion of copper. Therefore it is beneficial for thermal endurance to use materials with low CTE in Z direction. Flame retardants in base materials are commonly required for ground based applications but are not necessary for space based PCBs.

For high frequency performance typically PTFE based materials are used. These materials require special lamination cycles as adhesion is generally poorer compared to polyimide and epoxy.

IPC-4121 provides a comparison of various properties for core constructions as function of resin and glass type.

Table 6-1: Characteristics of some example dielectric materials for laminates

Type of material	Dielectric constant		Dissipation Factor		Tg (°C)	water absorption (%)	Volume density (g/cm^3)	CTE (ppm/K) below Tg			CTE (ppm/K) above Tg			Thermal conductivity (W/m.K)	Example
	at 1 MHz	at 10 GHz	at 1 MHz	at 10 GHz				X	Y	Z	X	Y	Z		
Epoxy HTg	4,24	3,92	0,015	-	180	0,15	-	13 - 14	13 - 14	45	14 - 17	14 - 17	230	0,4	370 HR (Isola)
	4,24	3,92	0,015	-	170	0,15	-	13 - 14	13 - 14	45	14 - 17	14 - 17	230	0,4	IS420 (Isola)
Polyimide / Glass	4,2	-	0,01	-	> 250	0,26	1,6	16	16	51	-	-	158	0,2	35N (Arlon)
	4,2	-	0,01	-	250	0,27	1,6	16	16	55	-	-	149	0,2	85N (Arlon)
Polyimide / Aramid	3,6	-	0,014	-	250	0,6	1,37	6 - 9	6 - 9	93	-	-	279	0,2	85NT (Arlon)
Polyimide flex laminate	3,4	3,3	0,003	-	220	0,8	-	25	25	-	-	-	-	-	AP (DuPont)
Ceramic reinforced PTFE	-	2,94	-	0,0012	-	0,02	2,1	16	16	24	-	-	-	0,6	RT/Duroid 6002 (Rogers)
Hydrocarbon and ceramic reinforced glass	-	3,38	-	0,0027	> 280	0,06	1,79	11	14	46	-	-	-	0,71	RO 4003 (Rogers)
Glass reinforced PTFE	2,20	2,20	0,0004	0,0009	-	0,02	2,2	31	48	237	-	-	-	0,2	RT/Duroid 5880 (Rogers)
Ceramic thermoset	-	9,8	-	0,002	-	0,16	2,77	19	19	20	-	-	-	0,76	TMM10i (Rogers)

6.2.2 Material selection

ECSS-Q-ST-70-12_1200010

a. Selection of materials shall be performed in compliance with the requirements from the clause 6.5 of the ECSS-Q-ST-70-60.

ECSS-Q-ST-70-12_1200011

b. <<deleted>>

ECSS-Q-ST-70-12_1200012

c. The as-manufactured PCB shall be in conformance with the outgassing requirements of the clause 5.5.3 from the ECSS-Q-ST-70-02 or project specific requirements on cleanliness.

NOTE The outgassing requirements are CVCM<0,1% and RML<1,0%.

6.3 <<deleted>>

ECSS-Q-ST-70-12_1200013

a. <<deleted>>

ECSS-Q-ST-70-12_1200014

b. <<deleted>>

6.4 Traceability and marking

ECSS-Q-ST-70-12_1200015

a. The PCB shall be marked with part number and revision number from the PCB definition dossier as given by the supplier.

ECSS-Q-ST-70-12_1200016

b. All individual PCBs within the panel shall be identified by a serial number.

ECSS-Q-ST-70-12_1200017

c. The serialization of the PCB shall be established before the start of the fabrication.

ECSS-Q-ST-70-12_1200018

d. The serial number shall identify the position of the PCB on the panel.

ECSS-Q-ST-70-12_1200019

e. The serial number methodology shall be identified in the PID of the PCB manufacturer.

7
Rigid PCBs

7.1 PCB build-up

7.1.1 General

ECSS-Q-ST-70-12_1200377

a. The build-up of the PCB and each sub-assembly should be symmetric.

NOTE This is done to avoid warp and twist.

ECSS-Q-ST-70-12_1200020

b. The supplier shall record asymmetric build-up as a Review Item in the PCB definition dossier.

NOTE The build-up includes the copper thickness and its distribution.

ECSS-Q-ST-70-12_1200021

c. In case Molybdenum or CIC layers are used, they shall be included in the build-up and recorded as a Review Item in the PCB definition dossier.

NOTE 1 Specific requirements for the build-up are listed in the PCB definition dossier in A.2.1<5>a.3(h).

NOTE 2 On external layers, copper clad laminate typically achieves better peel strength whereas copper foil achieves better registration.

d. Sequential and non-sequential vias may be filled with prepreg resin or plugging paste.

7.1.2 Copper styles

ECSS-Q-ST-70-12_1200378

a. The thickness of the copper cladding on both sides of the laminate should be equal except on outer layers of the PCB or half-stack.

NOTE Equal copper thickness is needed when laminate is etched in same process steps, as is the case for internal layers. The exception on outer layers is made because each side is etched in different process steps and because thin copper on external layers decreases the total thickness after plating.

ECSS-Q-ST-70-12_1200022

b. In case the thickness of the copper cladding on the laminate is asymmetric, this asymmetric build-up of the PCB shall be recorded as a Review Item in the PCB definition dossier.

NOTE 17/70 copper thickness is more risky than 17/35 or 35/70 copper thickness. The presence of fine pitch tracks in combination with asymmetric copper further increases the difficulty to process.

ECSS-Q-ST-70-12_1200023

c. Except the case specified in the requirement 11.4.1e, the external and internal layers shall use basic copper thickness 70 µm, 35 µm or 17 µm.

NOTE 1 Copper layers can be implemented as copper clad laminate or as separate copper foils.

NOTE 2 Requirement 11.4.1e specifies microvia layers on HDI PCBs.

ECSS-Q-ST-70-12_1200379

d. Copper distribution within a layer should be homogeneous.

NOTE This is done to ensure even pressure distribution during lamination, which can cause filling voids, cracks or glass compression.

ECSS-Q-ST-70-12_1200380

e. Balancing of copper should be performed by including dummy non-functional copper.

NOTE This is more important for partial planes on thick copper layers such as 70 µm.

ECSS-Q-ST-70-12_1200381

f. Signal tracks should not be routed on copper plane layers.

ECSS-Q-ST-70-12_1200024

g. In case the total as-designed thickness of copper is above 700 µm, this shall be recorded as a Review Item in the PCB definition dossier.

NOTE High layer count in combination with thick copper layers can have significant impact on manufacturability and long-term reliability.

ECSS-Q-ST-70-12_1200025

h. Copper quality “HTE” shall be used for copper clad laminate.

NOTE Type HTE can be procured in conformance with IPC-4562 Type E, grade 3.

ECSS-Q-ST-70-12_1200026

i. Copper quality “JTC” or “HTE" shall be used for copper foils.

ECSS-Q-ST-70-12_1200382

j. The values from the Table 7-1 should be used in the design calculations for copper foil thickness.

NOTE The values indicated in Table 7-1 are minimum as-manufactured thickness for the specified as-designed foil thickness.

ECSS-Q-ST-70-12_1200383

Table 7-1: As-designed versus as-manufactured copper foil thickness

As-designed foil thickness (µm)	Minimum as-manufactured thickness for non-plated inner layers (µm)	Minimum as-manufactured thickness for plated layers with ≥25 µm plating (µm)
9	6	31
12	9	34
17	11	38
35	25	53
70	56	84

7.1.3 Dielectric thickness

ECSS-Q-ST-70-12_1200027

a. A minimum of two sheets of prepreg shall be used for insulation between two layers, except for requirement 11.4.1k.

ECSS-Q-ST-70-12_1200384

b. A minimum of two sheets of glass should be used in glass-reinforced laminates.

ECSS-Q-ST-70-12_1200028

c. In case a single sheet of glass is used in a glass-reinforced laminate it shall be recorded as Review Item in the PCB definition dossier.

NOTE Two sheets of glass reinforcement are specified to mitigate the risk of reduced insulation caused by contamination. This is also specified for laminates for class 3/A in accordance with IPC-6012 Appendix A. In case a single reinforcement in laminate is used, it is recommended to implement other means to mitigate the risk of contamination in laminate. IPC-4121 provides various properties, such as resin-to-glass ratio, for core laminate constructions.

ECSS-Q-ST-70-12_1200385

d. The insulation distance as-designed between two layers in rigid laminate or prepreg in Z direction should be in conformance with the values from Table 13-7.

NOTE This table specifies a minimum distance of 100 µm.

ECSS-Q-ST-70-12_1200029

e. Except the case specified in the 11.4.1h, the insulation distance as-manufactured between two layers in rigid laminate or prepreg in Z direction shall be in conformance with the values from Table 13-7.

NOTE 1 This table specifies a minimum projected peak-to-peak distance of 70 µm.

NOTE 2 Requirement 11.4.1h specifies microvia layers on HDI PCBs.

ECSS-Q-ST-70-12_1200030

f. Double-sided copper clad laminate with a thickness as-designed of 4 mil (~100 µm) shall not be used unless:

1. the voltage is less than 30V,
2. the copper foil thickness on both sides of the laminate is 17 µm or 35 µm,
3. the insulation distance as-manufactured is verified by the PCB manufacturer to be in compliance with requirement 7.1.3e, and
4. it is recorded as a Review Item in the PCB definition dossier.

NOTE 1 Requirement 7.1.3f.1 is in compliance with the values from Table 13-3.

NOTE 2 The nominal thickness of etched laminate can be read from the CoC. However, this does not indicate worst-case thickness as mentioned in the requirement 7.1.3e. Therefore the use of 4 mil laminate on the lower end of the tolerance between 3,5 mil and 3,8 mil is prohibited by this requirement.

NOTE 3 The precautions specified in this requirement are defined to prevent a worst-case insulation value of less than 70 µm due to high tolerances with rough copper surface treatment as indicated in Table 7-2.

ECSS-Q-ST-70-12_1200031

g. Double-sided copper clad laminate with a thickness as-designed of 5 mil (~125 µm) shall not be used above 30 V unless:

1. the thickness of laminate as-manufactured is in conformance with the Table 13-3,
2. the as-manufactured insulation distance is verified by the PCB manufacturer to be in compliance with requirement 7.1.3g.1,
3. it is recorded as a Review Item in the PCB definition dossier.

NOTE 1 The thickness value of the requirement 7.1.3g.1 is ≥100 µm.

NOTE 2 The lamintate thickness can be read from the CoC. It does not indicate worst-case thickness as mentioned in the requirement 7.1.3g.1. This prohibits the use of 5 mil laminate on the lower end of the tolerance between 4,5 mil and 4,8 mil.

NOTE 3 Precautions specified in this requirement are defined to prevent a worst-case insulation value

of less than 100 µm due to high tolerances with rough copper surface treatment as indicted in Table 7-2.

ECSS-Q-ST-70-12_1200032

h. For insulation distance in Z direction of a laminate, the minimum projected peak-to-peak insulation distance specified in the requirement 7.1.3i shall be used.

ECSS-Q-ST-70-12_1200033

i. The minimum projected peak-to-peak insulation distance shall include the thickness tolerance of the laminate core and the maximum roughness of copper surface treatment.

NOTE Projected peak-to-peak insulation distance is specified in Figure 3-1 of IPC-4101.

ECSS-Q-ST-70-12_1200386

j. If available, laminates should be class D in conformance with requirements from the IPC-4101 except the cases specified in the requirement 7.1.3k.

NOTE 1 Class D guarantees a minimum projected peak-to-peak insulation distance.

NOTE 2 Typically used materials can be unavailable in class D even though this specification exists.

ECSS-Q-ST-70-12_1200034

k. In case other laminate classes are used, the PCB manufacturer shall calculate minimum projected peak-to-peak insulation distance in conformance with requirement 7.1.3i.

NOTE An example of this is shown in Table 7-2 for class C laminate and commonly used copper profiles.

ECSS-Q-ST-70-12_1200035

l. The PCB manufacturer shall define laminate and prepreg styles and amount to achieve the insulation distances as designed by the supplier in conformance with requirements of the clause 13.8.

NOTE The supplier is responsible to design insulation distances required to meet design voltages in conformance with the requirement 13.8.2c.

Table 7-2: Example of worst case as-manufactured insulation distance for laminate with double-sided copper cladding

As-designed laminate thickness	Laminate thickness tolerance i.a.w. IPC4101 Table3.7 class C.	Copper foil 18 or 35 µm		Copper foil 70 µm	
		"Very low profile" i.a.w. IPC4562 Table3.1	Worst-case as-manufactured projected peak-to-peak insulation distance	"Low profile" i.a.w. IPC4562 Table3.1	Worst-case as-manufactured projected peak-to-peak insulation distance
101,6 µm (4 mil)	±13 µm	5,1 µm	78,4 µm	10,2 µm	68,2 µm
127 µm (5 mil)	±18 µm	5,1 µm	98,8 µm	10,2 µm	88,6 µm
152 µm (6 mil)	±18 µm	5,1 µm	123,8 µm	10,2 µm	113,6 µm
203 µm (8 mil)	±25 µm	5,1 µm	167,8 µm	10,2 µm	157,6 µm
254 µm (10 mil)	±25 µm	5,1 µm	218,8 µm	10,2 µm	208,6 µm

7.2 PCB dimension

The maximum dimensions of the PCB depend on the panel dimensions used and qualified by the PCB manufacturer. A typical large panel size is 45x60 cm (18x24 inch). Not all surface area of the panel is available for the PCB design as mandatory coupons are included in the panel.

7.3 Thickness of PCB

7.3.1 General

ECSS-Q-ST-70-12_1200036

a. PCB thickness shall be measured from bottom insulation to top insulation.

NOTE 1 The manufacturing tolerance is provided by the PCB manufacturer.

NOTE 2 It is important to include the manufacturing tolerance of 10% in conformance with the requirement 6.2.3.f.2 from the ECSS-Q-ST-70-60.

NOTE 3 Tolerances on individual copper clad laminate of 100 µm is about ± 18%. Tolerance on the total PCB stack is typically lower.

NOTE 4 Specific requirements for maximum thickness over metal surface finish are specified in the PCB definition dossier.

7.3.2 Polyimide PCB

ECSS-Q-ST-70-12_1200037

a. The thickness as-manufactured of a rigid and rigid-flex polyimide PCB should be ≤ 4,0 mm.

ECSS-Q-ST-70-12_1200387

b. The as-designed thickness of a rigid and rigid-flex polyimide PCB should be ≤ 3,6 mm, except the case specified in the requirement 7.3.2c.

ECSS-Q-ST-70-12_1200388

c. The as-designed thickness of a rigid and rigid-flex polyimide PCB may be > 3,6 mm in case:

1. the thickness as-manufactured is in conformance with requirement 7.3.2a,
2. the manufacturing tolerance is < 10%, and
3. it is recorded as a Review Item in the PCB definition dossier.

7.3.3 Epoxy PCB

ECSS-Q-ST-70-12_1200038

a. The thickness as-manufactured of a rigid and rigid-flex epoxy PCB should be ≤ 2,4 mm.

ECSS-Q-ST-70-12_1200389

b. The as-designed thickness of a rigid and rigid-flex epoxy PCB should be ≤ 2,2 mm, except the case specified in the requirement 7.3.3c.

ECSS-Q-ST-70-12_1200390

c. The as-designed thickness of a rigid and rigid-flex epoxy PCB may be >2,2 mm in case:

1. the thickness as-manufactured is in conformance with requirement 7.3.3a,
2. the manufacturing tolerance is < 10%, and
3. it is recorded as a Review Item in the PCB definition dossier.

7.3.4 Number of copper layers in PCB

ECSS-Q-ST-70-12_1200039

a. Number of copper layers for polyimide PCB should be ≤ 26.

ECSS-Q-ST-70-12_1200040

b. Number of copper layers for epoxy PCB should be ≤ 20.

7.3.5 Aspect ratio of vias

ECSS-Q-ST-70-12_1200041

a. Except the case specified in the recommendation 11.6b, the aspect ratio of vias on a rigid and rigid-flex PCB shall be ≤ 7.

NOTE 1 There is no additional requirement for the minimum diameter of plated via in case the diameter conforms to the aspect ratio of ≤ 7.

7.4 Track width and spacing

7.4.1 General

ECSS-Q-ST-70-12_1200391

a. A verification should be performed to prevent non-functional changes of direction of tracks.

NOTE Some automated routing software can cause unnecessary changes of direction that have no function.

7.4.2 Manufacturing tolerances for width and spacing

ECSS-Q-ST-70-12_1200042

a. The relative manufacturing tolerances on the track width and spacing of internal and external layers shall be as specified in Table 7-3.

ECSS-Q-ST-70-12_1200043

b. The maximum absolute manufacturing tolerances on the track width and spacing of internal and external layers should be as specified in Table 7-3.

NOTE 1 For example, an internal track width of 400 µm on 35 µm copper thickness has a relative tolerance of ± 20 %, i.e. 80 µm, which is limited by the maximum absolute tolerance of 50 µm.

NOTE 2 The tolerance applies to as-designed dimensions. For example, a spacing as-designed of 200 µm with a tolerance of ± 20 % results in a spacing as-manufactured of 160 µm - 240 µm. Typically, the minimum spacing of 160 µm is important for PCB design.

ECSS-Q-ST-70-12_1200044

c. The use of planarization, copper reduction or surface preparation processes shall be excluded in the definition of the total copper thickness.

NOTE 1 Plating of sequential half stacks can be done with different plating methods, like panel plating, selective pattern plating or a combination and can include copper surface reduction processes to reduce copper surface thickness and give best options for fine pitch etching.

NOTE 2 The plated copper thickness as-designed is 25 µm. This can be a thicker layer as-manufactured.

ECSS-Q-ST-70-12_1200045

Table 7-3: Tolerance on track width and spacing of internal and external layers

Thickness category [µm]	Basic Cu [µm]	Plated Cu [µm]	Total Cu thickness [µm]	Relative tolerance on track width and spacing	Maximum absolute tolerance on track width and spacing
Th≤17	≤ 17	0	≤ 17	± 20 % FOR 11.5.5a.5: -10% to +20%	± 30 µm
17<Th≤60	≤ 17 35 35	1x25 0 1x25	≤ 42 35 60	± 20 %	± 50 µm
60<Th≤70	≤ 17 70	2x25 0	≤ 67 70		± 50 µm
70<Th≤95	35 70	2x25 1x25	85 95		± 70 µm
Note: Explanation of "FOR" is given in Table 13-1.					

7.4.3 External layers

ECSS-Q-ST-70-12_1200046

a. The as-manufactured track width and spacing as a function of copper thickness for external layers of rigid PCB shall be in conformance with the values specified in the Table 7-4.

ECSS-Q-ST-70-12_1200392

b. The as-designed track width and spacing for external layers of rigid PCB should be in conformance with the values specified in the Table 13-7 except the case specified in the requirement 7.4.3c.

ECSS-Q-ST-70-12_1200047

c. In case the as-designed track width and spacing for external layers of rigid PCB is less than the values specified in the requirement 7.4.3b, the following conditions shall be met:

1. the manufacturing tolerances as specified in the PID are smaller than as specified in Table 7-3,
2. the as-manufactured dimensions specified in Table 7-4 and Table 13-7 are met, and
3. it is recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200393

d. Tracks should not be routed on external layers.

ECSS-Q-ST-70-12_1200394

e. In case tracks are routed on external layers they should not be routed under components.

ECSS-Q-ST-70-12_1200048

f. The basic copper foil thickness of fine pitch shall be ≤ 17 µm.

ECSS-Q-ST-70-12_1200395

g. Fine pitch track width and spacing may be used in case:

1. fine pitch tracks are used to route to the footprint of a fine pitch component,
2. the length of fine pitch tracks is ≤ 20 mm from the solder pad,
3. conformal coating is applied on fine pitch tracks or pads in conformance with the requirement 13.8.4b,
4. the voltage is ≤ 30V, and
5. it is recorded as a Review Item in the PCB definition dossier.

NOTE A long fine pitch track can cause solder pearls.

ECSS-Q-ST-70-12_1200049

h. Spacing and width of pads shall be in conformance with the requirements for tracks specified in 7.4.3a, 7.4.3b, 7.4.3c, 7.4.3f and 7.4.3g.

ECSS-Q-ST-70-12_1200050

Table 7-4: Minimum as-manufactured track width and spacing for external layers as a function of copper thickness for standard technology

Basic Cu [µm]	Plated Cu [µm]	Thickness category [µm]	Pitch	As-manufactured	
				width [µm]	spacing [µm]
17	1x 25	17<Th≤60	fine/normal	120/160	120/160
17	2x 25	60<Th≤70	fine/normal	120/160	120/160
35	1x25	17<Th≤60	normal	160	160
35	2x25	70<Th≤95	normal	240	240
70	1x25	70<Th≤95	normal	240	240

7.4.4 Normal pitch tracks on internal layers

ECSS-Q-ST-70-12_1200051

a. The as-manufactured track width and spacing as a function of copper thickness for internal layers of rigid PCB shall be in conformance with the values specified in the Table 7-5.

ECSS-Q-ST-70-12_1200396

b. The as-designed track width and spacing for internal layers of rigid PCB should be in conformance with the values specified in the Table 13-7 except the case specified in the requirement 7.4.4c.

ECSS-Q-ST-70-12_1200052

c. In case the as-designed track width and spacing for internal layers of rigid PCB is less than the values specified in the requirement 7.4.4b, the following conditions shall be met:

1. the manufacturing tolerances as specified in the PID are smaller than as specified in Table 7-3,
2. the as-manufactured dimensions specified in Table 7-5 and Table 13-7 are met, and
3. it is recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200053

d. The thickness category of copper on internal layers shall be as specified in Table 7-3.

ECSS-Q-ST-70-12_1200054

Table 7-5: Minimum as-manufactured track width and spacing for internal layers as a function of copper thickness for standard technology

Thickness category [µm]	Pitch	As-manufactured	
		width [µm]	spacing [µm]
Th≤17	fine/normal	80/104	96/104
17<Th≤60	normal	120	120
60<Th≤70	normal	160	160
70<Th≤95	normal	240	240

7.4.5 Fine pitch tracks on internal layers

ECSS-Q-ST-70-12_1200055

a. Except the case specified in the requirement 11.5.5a, the track width and spacing for fine pitch on internal layers shall be in conformance with the as-manufactured dimensions specified in Table 7-5.

NOTE Requirement 11.5.5a specifies track width and spacing for impedance controlled routing to AAD with 1 mm pitch on HDI PCBs .

ECSS-Q-ST-70-12_1200056

b. In case fine pitch tracks are used, this shall be recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200057

c. Fine pitch shall be limited to the functionality of impedance control or signal routing to AAD.

ECSS-Q-ST-70-12_1200058

d. Fine pitch tracks shall be limited to ≤ 30 V.

ECSS-Q-ST-70-12_1200059

e. For routing to AAD, fine pitch tracks should fan out to normal pitch as soon as they are outside the AAD footprint.

ECSS-Q-ST-70-12_1200060

f. In case no other circuitry is adjacent that requires the use of fine pitch, the routing of fine pitch tracks should increase the insulation distance and track width as specified for normal pitch in the Table 7-5.

NOTE 1 CAD software can implement different minimum insulation distances and track widths in areas with different space available.

NOTE 2 The Figure 7-1 shows examples of possible improvements in routing.

ECSS-Q-ST-70-12_1200061

g. Fine pitch shall be manufactured by using ≤ 17 µm basic copper thickness without plating steps.

7.4.6 Routing to AAD footprint on internal layers

ECSS-Q-ST-70-12_1200062

a. Tracks in AAD footprint shall be placed equidistant between pads to increase insulation distance to both pads.

NOTE See example of nonconformance indicated by blue arrow in Figure 7-1.

ECSS-Q-ST-70-12_1200063

b. Tracks shall exit from AAD footprint before changing direction to keep the insulation distance to the pad in compliance with normal pitch as specified in Table 7-5.

NOTE See example of nonconformance indicated by green arrow in Figure 7-1.

ECSS-Q-ST-70-12_1200064

c. Widening of tracks should occur close to AAD footprint to provide a wider track where no other circuitry is adjacent that requires the use of fine pitch.

NOTE See example of nonconformance indicated by yellow arrow in Figure 7-1.

ECSS-Q-ST-70-12_1200397

d. Changing of direction of track should be in compliance with the requirement 7.4.1a.

NOTE See example of nonconformance indicated by white arrow in Figure 7-1

ECSS-Q-ST-70-12_1200398

e. Pads of AAD footprint should be designed with teardrop reinforcement

NOTE Pads in Figure 7-1 are not designed with teardrop reinforcement.

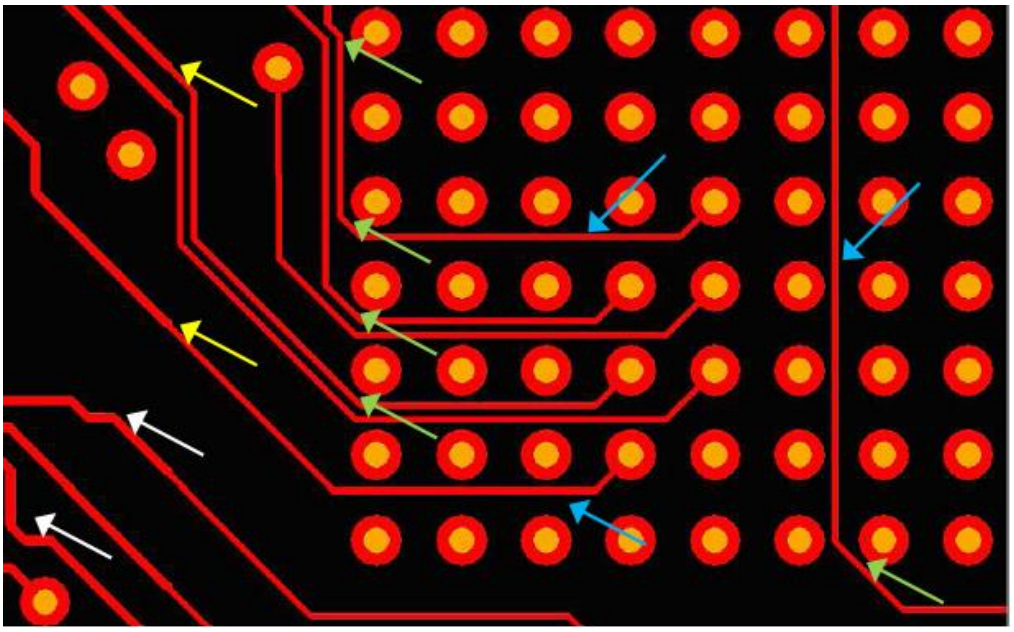


Figure 7-1: Example of automated fine pitch routing and possible improvements

7.5 Pad design

7.5.1 Overview

Pad sizes from clause 7.5.3 are specified using minimum dimensions. It is good practice to allow for higher manufacturing tolerances in case of complex technology, such as high layers count, dissimilar materials, sequential lamination. Such larger tolerances lead to larger designed pad dimensions. This is also described in clause 4.3 and the note 2 of requirement 7.5.3h. The tolerances that affect capability to manufacture small pads are specific to each PCB manufacturer. It is, therefore, important to consult with the PCB manufacturer during the design process for pad dimensions to ensure it is within capability and with minimum risk. This early interaction between PCB manufacturer and designer is also described in requirement 5.2e and its NOTE 2.

7.5.2 Non-functional pad removal

ECSS-Q-ST-70-12_1200065

a. Non-functional pads in PTH shall be present on all layers, except two cases specified in the requirement7.5.2b.

NOTE The presence of non-functional pads reduce the risk of hole wall pull-away and reduce the risk of cracks in resin-rich areas.

ECSS-Q-ST-70-12_1200399

b. Non-functional pads in PTH may be removed:

1. when the presence of the pads degrade the electrical performance, they can be removed by the supplier, or

2. to prevent high pressure area during lamination that cause resin starvation in the prepreg, the pads can be removed by the PCB manufacturer.

NOTE Removal of non-functional pads is approved by supplier and PCB manufacturer during MRR in conformance with the requirement 7.5.2c.5.

ECSS-Q-ST-70-12_1200066

c. When non-functional pads in PTH are removed as specified in the requirement 7.5.2b, the following conditions shall be met:

1. non-functional pads are present on all copper plane layers,

2. non-functional pads are present on flex laminate,

3. maximum half of the non-functional pads in the pad stack are removed,

4. non-functional pads are removed on maximum two consecutive layers,

5. it is recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200400

d. Non-functional pads in PTH should not be removed on layer 2 and n-1.

e. Non-functional pads in core vias, buried vias and through-going vias may be removed in case the following conditions are met:

1. non-functional pads are present in clearance holes of plane layers of ≥70µm copper thickness,

2. it is recorded as a Review Item in the PCB definition dossier,

3. IST coupon design is representative for both via configurations with pads in and pads out.

NOTE Pads in plane layers and/or thick copper layers are kept to avoid a large resin-rich volume that is prone to resin cracks. Resin cracks can be screened by dark field microscopy. Presence of pads can provide anchor points for the via, which is of importance for soldering and prevents hole wall pull away in PTH. Absence of pads can improve thermal cycling fatigue, because stresses are more uniformly distributed. Barrel cracks can be screened by IST.

f. When non-functional pads are removed, the spacing of conductors to a via hole wall shall be as if the pad was present.

NOTE The extra space available due to removal of the pad is not used for routing.

g. For blind-via-in-pad assembly, non-functional pads should be kept in.

7.5.3 Pad dimensions

ECSS-Q-ST-70-12_1200067

a. The annular ring as-manufactured shall be in conformance with the requirements 10.2a and 10.2b of ECSS-Q-ST-70-60.

NOTE The drilled diameter is typically 0,2 mm larger than the as-manufactured minimum hole diameter.

ECSS-Q-ST-70-12_1200068

b. <<deleted>>

ECSS-Q-ST-70-12_1200069

c. <<deleted>>

ECSS-Q-ST-70-12_1200401

d. For component holes on solder side the minimum diameter of external pads should be the diameter of as-manufactured hole plus ≥ 0,8 mm.

ECSS-Q-ST-70-12_1200402

e. For component holes on solder side the minimum diameter of external pads may be the diameter of as-manufactured hole plus ≥ 0,6 mm in case:

1. the as-manufactured annular ring as specified in the requirement 7.5.3c,
2. the component holes are a footprint for a nano D connector,
3. it is recorded as Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200403

f. For via holes and component holes on component side the diameter of external pads should be the diameter of as-manufactured hole plus ≥ 0,6 mm.

ECSS-Q-ST-70-12_1200404

g. For via holes and component holes on component side the diameter of external pads may be the diameter of as-manufactured hole plus ≥ 0,5 mm in case:

1. the as-manufactured annular ring as specified in the requirement 7.5.3b, and
2. it is recorded as a Review Item in the PCB definition dossier.

h. The diameter of internal pads should be the diameter of drilled hole plus ≥ 0,3 mm.

NOTE It is important to consider the number of drilling and lamination sequences and the PCB manufacturing tolerances for the design of the diameter of the pads. It is recommended to contact the PCB manufacturer to review pad design for complex and cumulative lamination sequences, as this will require larger pad as-designed. It is good practice to design with the most conservative internal pad diameter and not to design to the lower limits.

i. Internal pad diameters D_{pad} of mechanically drilled holes should be designed in accordance with the following guideline:

$D_{pad} \geq FHS + a + 2xb + c + (d_1 + d_2 \ldots + d_N)$

where:

FHS = finished hole size (with centred mechanical tolerance)

a = increase of the drill diameter to compensate for hole wall plating and surface finish:

- +0,15 mm to +0,20 mm for tin-lead finish of PTH
- +0,10 mm for ENIG (and similar) of PTH
- can be zero for vias.

b = minimum annular ring: the following values are specified in this standard 0,025 mm or 0,050 mm

c = cumulative manufacturing tolerance for drilling, registration and etching: standard tolerance 0,25 mm / reduced tolerance 0,20 mm.

(d1 + d2 … + dN) = build-up tolerance for additional and cumulative technology features, such as:

- second lamination and each additional lamination +0,05 mm,
- use of rigid-flex +0,10 mm,
- more than 8 copper layers +0,05 mm,
- asymmetric build-up +0,05 mm.

NOTE As an example: A 0,8 mm finished hole size with tin-lead finish with no added complexity would result in a pad diameter = 0,80 + 0,20 + 2x0,05 + 0,25 = 1,35 mm pad diameter. Figure 7-2 shows dimensional features of a via.

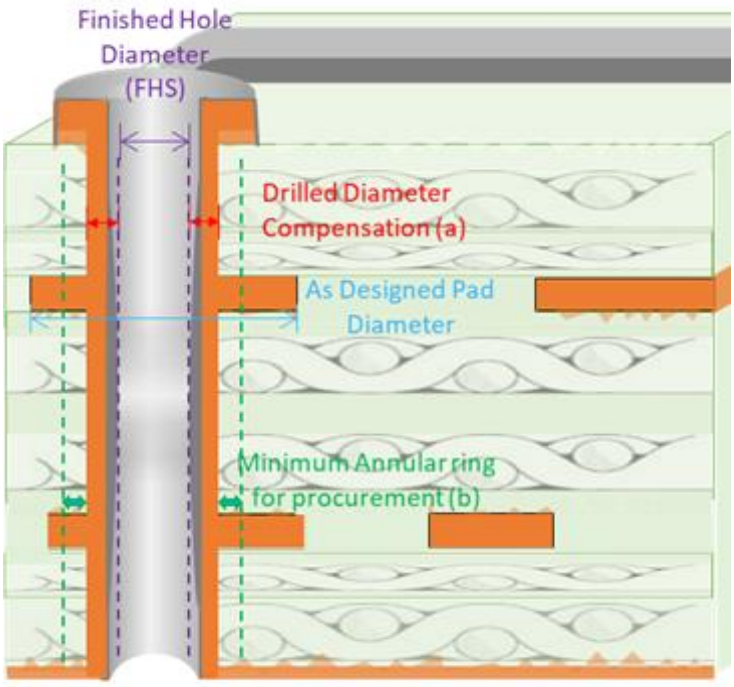


Figure 7-2: Via dimensions

ECSS-Q-ST-70-12_1200406

j. The diameter of pads may be the diameter of the drilled hole plus < 0,3 mm in case this is recorded as a Review Item in the PCB definition dossier.

NOTE Tear drop reinforcement of pads to tracks can be used for a more robust design and to mitigate the risk of a smaller designed diameter, or design to the smaller limits as per 7.5.3i.

k. Teardrop reinforcement should be designed on all internal pads.

NOTE This can be implemented by the designer or by the PCB manufacturer. In the latter case it is good practice to review during MRR. An example of teardrop pad design is shown in Figure 11-4. In this figure "A" is the minimum annular ring between hole and circular pad design; "B" is the effective annular ring with teardrop reinforcement applied.

l. The diameter of internal pads may be reduced in case the following conditions are met:

1. the annular ring as-manufactured is ≥ 25 µm,
2. teardrop reinforcement is implemented,
3. length of wicking and drilling cracks is in conformance with Ref B of Table 10-6 of ECSS-Q-ST-70-60,
4. electrical registration coupons are added in conformance with 10.6.1.d of ECSS-Q-ST-70-60,

5. it is recorded as a Review Item in the PCB definition dossier.

NOTE 1 ECSS-Q-ST-70-60 Table 10-6 and Table 10-26 specify that cracks and wicking cannot exceed the minimum annular ring.

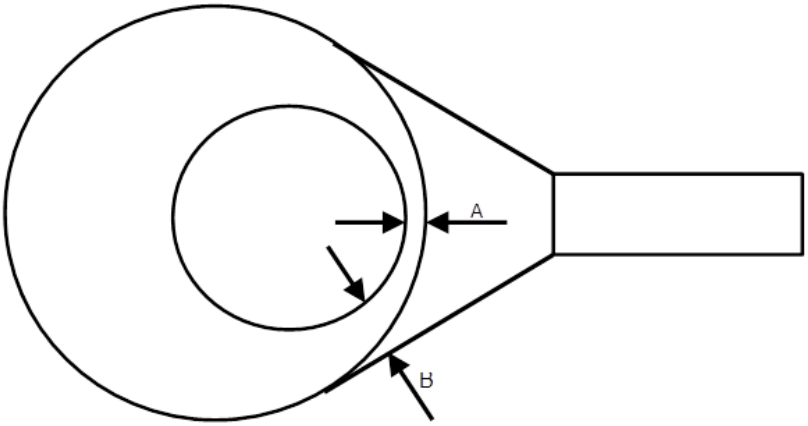


Figure 7-3: Tear drop pad design

7.5.4 Non-circular external pads

ECSS-Q-ST-70-12_1200070

a. Pads for component holes on external layers shall be circular, except cases specified in the requirement 7.5.4b.

ECSS-Q-ST-70-12_1200407

b. Non-circular pads may be used for component holes, in case the following conditions are met:

1. the surface area of the oblong pad is not smaller than the surface area of the circular pad as specified in the requirements from the clause 7.5.3,
2. the oblong pad meets the requirement for annular ring of 100 µm as-manufactured, and
3. it is recorded as a Review Item in the PCB definition dossier.

NOTE 1 For the requirement 7.5.4b.1 $A_{(oblong)}$ in Figure 7-4 is the surface area of the oblong pad and $A_{(circular)}$ in Figure 7-4 is the surface area of a circular pad

NOTE 2 For the requirement 7.5.4b.2 see Annular $ring_{(oblong)}$ in Figure 7-4

NOTE 3 The design in the requirement 7.5.4b.2 is a deviation of Ref b and Ref c of Table 10-2 of ECSS-Q-ST-70-60, which specifies 200 µm and 130 µm annular ring on solder side (see Annular $ring_{(circular)}$ in Figure 7-4). This is a reduced

annular ring in one direction, compensated by a larger annular ring in the other direction.

NOTE 4 Other non-circular pad designs are possible and typically used on external layers for AAD and SMT components. Dog-bone shapes or key hole shapes can be used for the verification of solder joint quality or to prevent thermal stress on (blind or micro) vias.

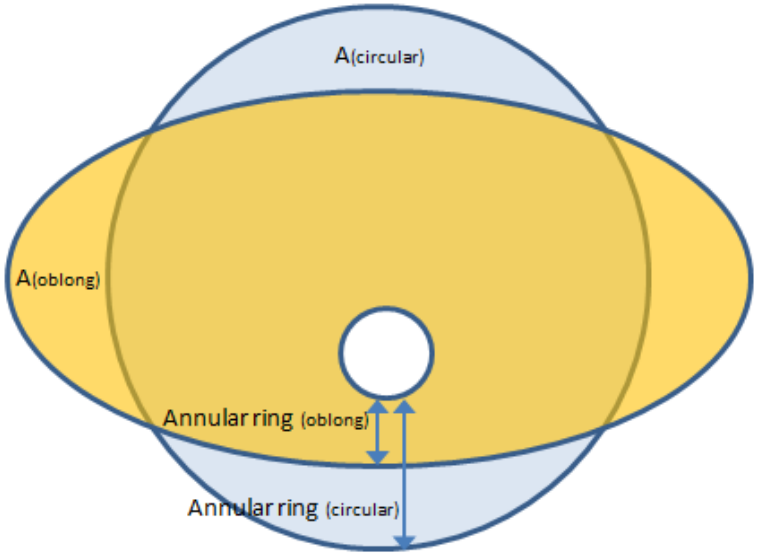


Figure 7-4: Comparison between circular and oblong pads showing annular ring and the centre of the hole misregistered with the centre of the pad

7.6 Copper planes in rigid PCB

ECSS-Q-ST-70-12_1200408

a. Copper planes should have additional openings in a grid format.

NOTE 1 For example, planes larger than 10 cm^2 can be designed using a grid.

NOTE 2 An example of a grid plane is shown inFigure 7-5.

ECSS-Q-ST-70-12_1200409

b. The grid should be offset between layers.

NOTE These additional openings act as venting holes for desorption of humidity out of the PCB. For example, a grid can be 0,4 mm lines at a pitch of 0,6 mm and at 45° angle. The thermal and electrical resistance across such hatch plane is a factor of 2,5 larger than across a solid plane, assuming pattern as specified above. This can affect both power distribution and signal integrity, in particular for RF or digital PCB.

ECSS-Q-ST-70-12_1200410

c. For partial copper planes, balancing of copper should be performed in conformance with requirements 7.1.2d and 7.1.2e.

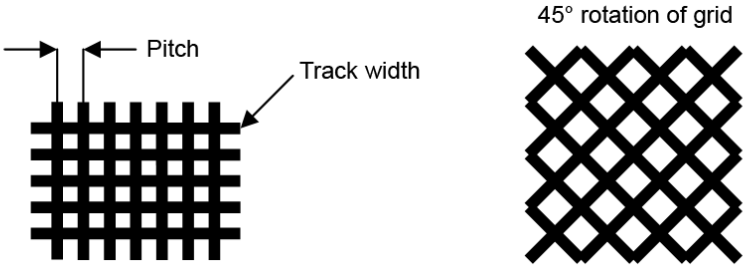
ECSS-Q-ST-70-12_1200411

d. Copper layers should be placed symmetrically within the build-up.

NOTE This is done to limit warp and twist.

ECSS-Q-ST-70-12_1200071

e. In case copper layers are placed asymmetrically within the build-up, this shall be recorded as a Review Item in the PCB definition dossier.



ECSS-Q-ST-70-12_1200412

Figure 7-5: Grid copper plane with openings

7.7 Design considerations for the prevention of sliver and peelable

ECSS-Q-ST-70-12_1200072

a. All areas of the conductive patterns as well as areas of insulating dielectric shall have a dimension of ≥ 0,1 mm in X and Y direction after etch compensation, except for the case of fine pitch track width and spacing as specified in the clause 7.4.5 and 11.5.5.

NOTE This is done to prevent sliver or peelable see Figure 7-6.

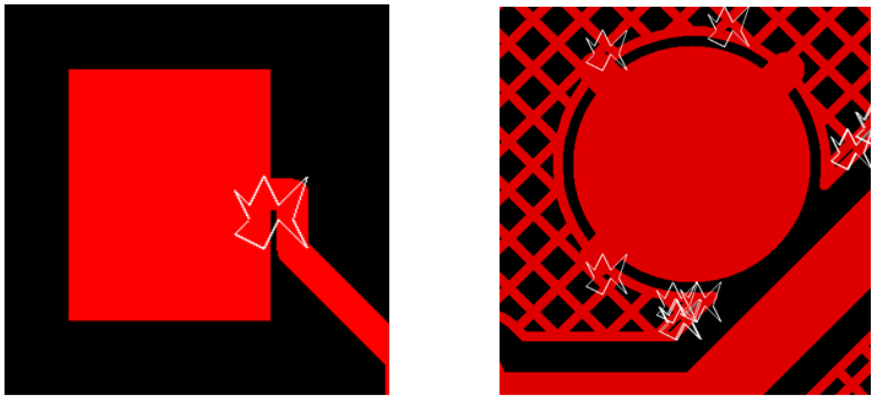


Figure 7-6: Example of peelable (left) and sliver (right)

7.8 PCB surface finish

7.8.1 Metallization

ECSS-Q-ST-70-12_1200073

a. Plating of metallic layers and finishes shall be done in conformance with the requirements from the clause 6.6 and requirements 10.2l and 10.2m of the ECSS-Q-ST-70-60.

ECSS-Q-ST-70-12_1200074

b. Except cases specified in the requirement 7.8.1d, each finish shall be on separate outer layer nets when a single PCB uses a mixed surface finish of electrolytic gold and fused tin-lead.

ECSS-Q-ST-70-12_1200075

c. Separate outer layer nets with mixed surface finishes shall have insulation distance of > 500 µm.

ECSS-Q-ST-70-12_1200413

d. Mixed surface finish may be used on the same outer layer net in case the following conditions are met:

1. a tin-lead overlap on electrolytic gold of ≥ 200 µm is used, and
2. the distance of gold plating to a solder pad is ≥ 200 µm.

NOTE 1 Condition specified in the requirement 7.8.1d.1 is to ensure coverage of the plated copper.

NOTE 2 Condition specified in the requirement 7.8.1d.2 is to avoid gold-tin embrittlement in the solder joints.

ECSS-Q-ST-70-12_1200076

e. A PCB with mixed surface finishes shall be recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200414

f. Other surface finishes than the ones specified in the requirements from 7.8.1a to 7.8.1d may be used for non-soldering purpose.

g. Surface finish types for soldering and for solderless assembly should be as per the recommendations from the component supplier.

NOTE Hot oil reflowed SnPb, galvanic (Ni)Au, ENIG, ENEPIG and ENIPIG are finishes in use and hold various levels of qualification (generic qualification, project qualification) for the bare PCB technology and for the assembly verification.

7.8.2 Solder mask

7.8.2.1 Overview

Solder mask can be used to prevent solder flowing away from AAD in a dog-bone footprint, possibly with through-hole vias. However, it is good practice to design with via-in-pad (blind, micro or filled via), which can avoid the need of solder mask. Solder mask can help to prevent solder bridging in fine pitch areas.

Problems seen with solder mask include poor adhesion to tin-lead, poor outgassing performance, high risk associated with selective stripping of tin-lead, the implementation of a minimum width to ensure adhesion and a transition zone of solder mask overlapping on tin-lead to prevent exposed copper and allow for registration tolerance.

7.8.2.2 Use of solder mask

ECSS-Q-ST-70-12_1200077

a. In case solder mask is used, the following conditions shall be met:

   1. solder mask is applied on bare copper and before surface finish,

   2. the minimum width of solder mask between openings is ≥ 100 µm,

   3. via holes are non-tented with a clearance diameter of ≥ 150 µm larger than the drilled hole size,

      NOTE A clearance diameter of ≥ 150 µm larger than the drilled hole size results in a nominal annular ring of ≥ 75 µm. This is affected by manufacturing tolerances for registration, plated hole wall copper thickness, solder mask dimensional definition. The as-manufactured minimum annular ring (MAR) of a via can be zero, i.e. tangency. For a PTH, the normal annular ring requirement for external pads is used.

b. The design of pads should be non-solder mask defined (NSMD).

c. In case of NSMD pads, the clearance distance between solder mask and pad shall be ≥ 75 µm.

d. In case of solder mask defined pads (SMD) for component holes, the clearance diameter in the solder mask exposing the external pad shall be ≥ 150 µm larger than the minimum pads specified in in 7.5.3d, 7.5.3e, 7.5.3f and 7.5.3g.

   NOTE The additional 150 µm clearance diameter is specified to allow for additional tolerance on solder mask dimensional definition and registration. This ensures that the as-manufactured minimum-annular ring on component holes is achieved.

e. The clearance distance between solder mask and the edge of the PCB, or the edge of a non-plated hole shall be ≥ 350 µm.

   NOTE This is specified to prevent lifted solder mask.

f. The colour of solder mask should be green.

NOTE Green colour for solder mask is specified because it is the most common type and easiest for processing and AOI.

g. Solder mask shall not be used as insulating layer, unless minimum coverage and dielectric withstanding voltage are specified in the PCB definition dossier and subject of a specific project qualification.

NOTE 1 It is common practice that conformal coating is applied on PCBs with solder mask, similarly to PCBs without solder mask as per 13.8.4.

NOTE 2 It is good practice to verify the compatibility of solder mask with subsequent assembly processes, as described in 13.2.1c of ECSS-Q-ST-70-61. This can include wettability, adhesion and chemical compatibility of conformal coating, as well as cleaning processes, and soldering methods.

8
Flex PCBs

8.1 Overview

This clause specifies requirements for flex PCBs with the purpose to maintain flexibility and achieve mechanical strength.

8.2 Dynamic applications

ECSS-Q-ST-70-12_1200078

a. Dynamic applications with flex PCBs shall be project qualified.

NOTE The testing of flex PCBs only covers static applications and the integration of the PCB.

8.3 PCB build-up

8.3.1 General

ECSS-Q-ST-70-12_1200079

a. The maximum number of copper layers on a flex PCB shall be 2.

ECSS-Q-ST-70-12_1200080

b. Thickness of a flexible PCB shall be ≤ 0,6 mm over the cover layers as-designed and as-manufactured.

NOTE This assumes maximum thickness of laminate, copper, adhesive and cover layer.

8.3.2 Dielectric materials

ECSS-Q-ST-70-12_1200081

a. Flex PCBs shall be manufactured with copper clad flexible polyimide laminate without adhesive between copper and laminate.

NOTE 1 This laminate type is named “adhesiveless”.

NOTE 2 The laminate typically used is of type Pyralux AP from DuPont.

ECSS-Q-ST-70-12_1200082

b. The as-designed thickness of the flex laminate shall be 25 µm , 50 µm, 75 µm, 100 µm or 150 µm.

NOTE 50 µm thickness is preferred.

ECSS-Q-ST-70-12_1200083

c. The tolerance for the as-manufactured thickness of the flex laminate shall be:

1. for ≤ 50 µm flex laminate: ≤ ±12,5 %, and
2. for ≥ 75 µm flex laminate: ≤ ±10 %.

NOTE This implies that for the as-manufactured PCB, the minimum insulation between two layers of flexible laminate in Z direction is 22 µm.

ECSS-Q-ST-70-12_1200084

d. The thickness of the polyimide cover layer shall be 25 µm or 50 µm.

ECSS-Q-ST-70-12_1200085

e. The thickness of the acrylic adhesive on the cover layer shall be 25 µm or 50 µm.

NOTE A typical cover layer is of type Pyralux LF from DuPont.

8.3.3 Copper cladding

ECSS-Q-ST-70-12_1200086

a. The thickness of copper cladding shall be 17 µm, 35 µm or 70 µm.

ECSS-Q-ST-70-12_1200415

b. Thickness of copper cladding 70 µm should not be used.

NOTE This is recommended to avoid risk in the bonding cycle of the cover layer.

ECSS-Q-ST-70-12_1200087

c. In case copper cladding of 70 µm is used, this shall be recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200088

d. Copper cladding on flex laminate of >17 µm shall be the type “rolled and annealed”.

ECSS-Q-ST-70-12_1200089

e. Copper cladding on flex laminate of 17 µm shall be the type “rolled and annealed” or “electrodeposited”.

8.3.4 Copper planes in flex PCB

ECSS-Q-ST-70-12_1200416

a. Full copper planes should not be used except the case specified in the requirement 8.3.4b.

ECSS-Q-ST-70-12_1200090

b. In case full copper planes are used, this shall be recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200417

c. In case a copper plane is used in a flex PCB, a grid with openings should be implemented as specified in the Figure 7-5.

NOTE The purpose of the openings is to improve adhesion of the cover layer, desorption of humidity and flexibility of the PCB. A grid can be 0,4 mm lines at a pitch of 0,6 mm and at 45° angle. It is preferable to have the grid offset between layers. In this case, the electrical and thermal resistance increases by a factor of approximately x2,5 compared to a solid plane.

8.4 Track design

ECSS-Q-ST-70-12_1200091

a. Tolerances on track width and spacing shall be as specified in the Table 7-3.

ECSS-Q-ST-70-12_1200092

b. Track width and spacing shall be as specified in the Table 8-1.

ECSS-Q-ST-70-12_1200093

c. <<deleted>>

ECSS-Q-ST-70-12_1200094

d. <<deleted>>

ECSS-Q-ST-70-12_1200418

e. Tracks should be evenly distributed over the entire width of the PCB.

ECSS-Q-ST-70-12_1200419

f. Non-functional tracks may be used to achieve an even distribution of tracks over the entire width of the PCB.

ECSS-Q-ST-70-12_1200420

g. Tracks on double-sided boards should not be superimposed and a clearance distance in X,Y direction should be implemented.

NOTE This is done to reduce the local thickness. An example of off-set tracks is shown in Figure 8-1.

ECSS-Q-ST-70-12_1200421

h. Edges of tracks should not be superimposed.

NOTE This is done to prevent localised high pressure during lamination.

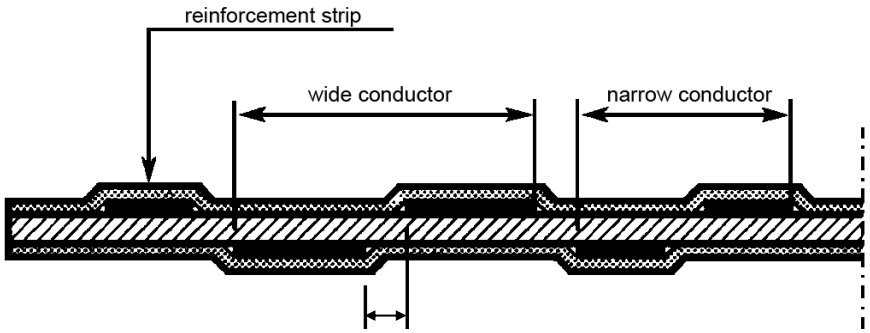


Figure 8-1: Clearance of tracks on flex PCBs.

ECSS-Q-ST-70-12_1200095

i. Tracks shall not change direction within the bending zone, as specified in Figure 8-2.

ECSS-Q-ST-70-12_1200422

j. The edge of the PCB should include on one side of the laminate a non-functional track as mechanical reinforcement with a width of ≥ 0,3 mm.

NOTE 1 This is indicated as "Ir" in Figure 8-2.

NOTE 2 The non-functional track for mechanical reinforcement is named reinforcement strip.

ECSS-Q-ST-70-12_1200423

k. The reinforcement strip should be implemented on the following areas:

1. Termination zone when no other mechanical fixing is designed apart from the termination leads,
2. Zone where a change of direction of tracks or copper plane occurs,
3. Bending zone.

ECSS-Q-ST-70-12_1200096

l. The distance of tracks or reinforcement strip to the edge of the board shall be ≥ 0,5 mm.

NOTE This is indicated as “b4” in Figure 8-2.

ECSS-Q-ST-70-12_1200424

m. The distance of tracks or reinforcement strip to the edge of the board should be ≥ 1,0 mm.

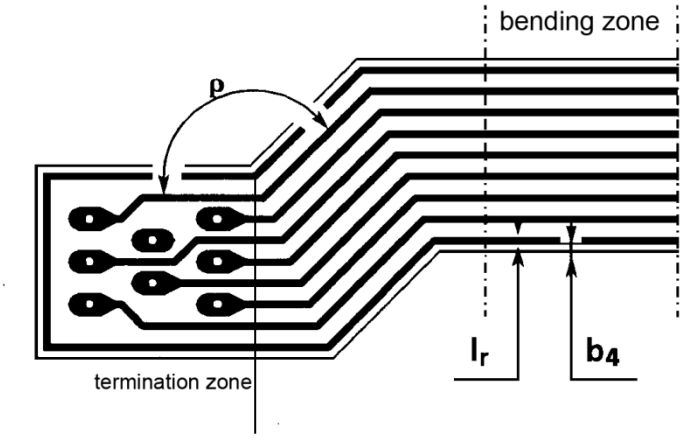
ECSS-Q-ST-70-12_1200097

n. Track width and spacing shall be in conformance with the values specified in the Table 13-4.

ECSS-Q-ST-70-12_1200098

o. When tracks change direction, the angle (p) shall be ≥ 135° as specified in the Figure 8-2.

NOTE It is recommended to design tracks as straight as possible.



ECSS-Q-ST-70-12_1200099

Figure 8-2: Tracks on flex, defining termination and bending zones.

Table 8-1: Minimum as-manufactured track width and spacing for flex layers as a function of copper thickness

Thickness category [µm]	Pitch	As-manufactured	
		width [µm]	spacing [µm]
Th≤17	normal	120	150
17<Th≤60			
60<Th≤70	normal	160	160
70<Th≤95	Not permitted as per 8.3.3a		

8.5 Through holes

8.5.1 Annular ring

ECSS-Q-ST-70-12_1200100

a. Annular ring on a flex PCB shall be the distance of the surface copper from the hole wall to the clearance opening in the cover layer.

ECSS-Q-ST-70-12_1200101

b. Adhesive protruding from underneath the cover layer onto the surface copper shall be subtracted from the annular ring measurement.

ECSS-Q-ST-70-12_1200102

c. Annular ring as-manufactured on a component hole shall be ≥ 0,25 mm.

ECSS-Q-ST-70-12_1200103

d. Annular ring as-manufactured on non-soldering hole shall be ≥ 0,1 mm.

8.5.2 Vias and pads

ECSS-Q-ST-70-12_1200104

a. PTH shall be located only in termination zones, not in the bending zone, as specified in Figure 8-2.

ECSS-Q-ST-70-12_1200105

b. Terminal pads shall include PTH.

NOTE Terminal pads on single sided board have risk to be damaged during assembly. Terminal pads need to be reinforced by plating.

ECSS-Q-ST-70-12_1200106

c. The cover layer shall include a clearance for assembly of a PTH in conformance with the clause 8.5.1.

8.5.3 Tear drop pad for flex PCB

ECSS-Q-ST-70-12_1200107

a. The diameter of a circular pad with or without teardrop reinforcement shall be D_1 as specified in Figure 8-3.

ECSS-Q-ST-70-12_1200108

b. The diameter of an oblong pad shall be equal to D_2 as specified in Figure 8-3.

ECSS-Q-ST-70-12_1200425

c. The track width should be at least half the diameter of the pad except the case specified in the requirement 8.5.3d.

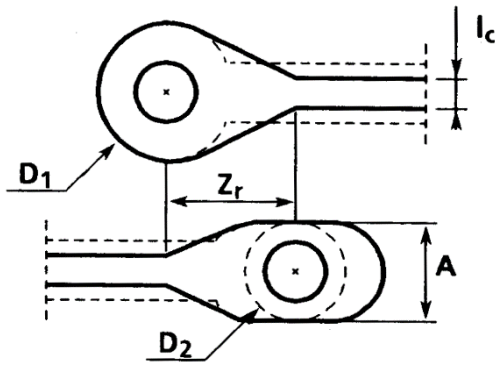
NOTE In the Figure 8-3 I_C is track width and D_1, D_2 are diameters of the pad.

ECSS-Q-ST-70-12_1200426

d. The track width may be less than half of the diameter of the pad in case the following conditions are met:

1. a teardrop reinforcement is added to the connection of the track to the pad, and
2. the reinforced zone has a length ≥ 0,8x the diameter of the pad.

NOTE In Figure 8-3 Z_r is the length of the reinforced zone.



ECSS-Q-ST-70-12_1200109

Figure 8-3: Teardrop reinforcement of terminal pads in flex PCB.

8.6 Bending radius

8.6.1 Overview

The PCB is designed to bend in L, U or S shapes with a radius of flexion that enables the PCB to be mounted and dismounted without damage. These radii depend on the type of board, the thickness of laminate and copper layers and a static or dynamic bending application, see Figure 8-4.

8.6.2 General

ECSS-Q-ST-70-12_1200110

a. The radius on a flex PCB having 50 µm laminate thickness and 35 µm double sided copper thickness and including cover layer shall be ≥ 12x total thickness of the flex for a static application.

NOTE In the Figure 8-4 R is the bending radius of a flex PCB

ECSS-Q-ST-70-12_1200111

b. Other PCB build-ups or dynamic applications shall be qualified by the supplier.

NOTE Other PCB build-ups include thicker laminate, thicker copper, or multilayers

ECSS-Q-ST-70-12_1200112

c. The termination zone shall include all termination pads.

ECSS-Q-ST-70-12_1200113

d. Bending of the flex PCB shall be designed not to occur on the termination zone and on an additional distance of 2 mm.

NOTE 1 In the Figure 8-4 the additional distance is indicated as X.

NOTE 2 Even though no bending is designed to occur on the termination zone, some bending can still occur on the assembled PCB due to the stress on the flex section. A stiffening of the termination zone by implementing double cover layer or adhesive can decrease the bending locally.

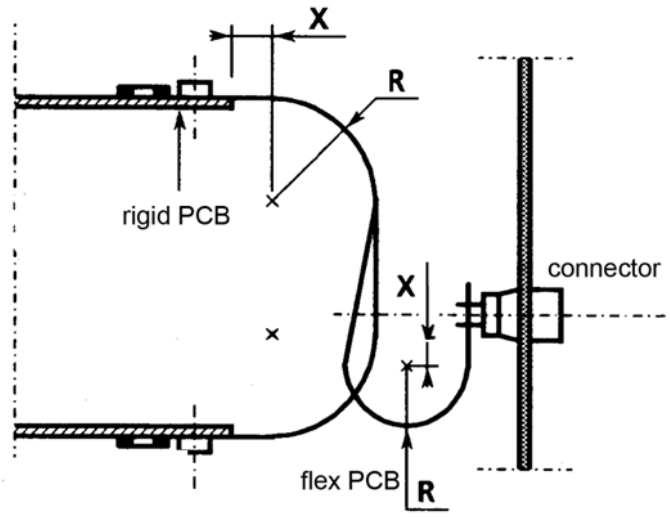


Figure 8-4: Bending radius of assembled flex

8.7 Sculptured flex PCB

8.7.1 Overview

Sculptured flex PCBs can be used as a connection between 2 PCBs or connectors. Sculptured flex circuits comprise of a copper circuit with different thickness sandwiched between two cover layers, as illustrated in Figure 8-5 and Figure 8-6.

8.7.2 General

ECSS-Q-ST-70-12_1200114

a. The thickness of the cover layer, excluding adhesive, shall be 25 µm.

ECSS-Q-ST-70-12_1200115

b. The thickness of the acrylic adhesive of the cover layer shall be 50 µm or 75 µm.

NOTE A typical cover layer is type Pyralux LF 0210 from DuPont.

ECSS-Q-ST-70-12_1200116

c. The surface finish shall be in conformance with the requirement 7.8.1b.

NOTE 1 This requirement specifies the use of hot oil reflowed tin-lead.

NOTE 2 The connector pins are cut after reflow and exposed copper is permitted.

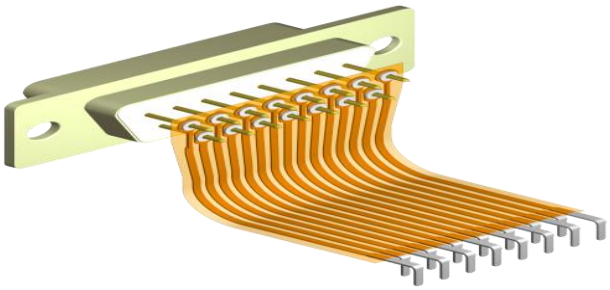


Figure 8-5: Sculptured flex circuit

8.7.3 Copper foil dimensions for build-up

ECSS-Q-ST-70-12_1200117

a. A single foil of copper shall be used in the build-up.

NOTE Copper clad laminate is not used.

ECSS-Q-ST-70-12_1200118

b. The initial thickness of the copper foil shall be 250 μm or 300 μm.

NOTE Copper type CW004 grade R240 (½ hard)

ECSS-Q-ST-70-12_1200119

c. The sculptured shape of the copper shall be manufactured by selective etching of the copper foil.

ECSS-Q-ST-70-12_1200120

d. The build-up, initial and etched copper thickness, track width and insulation distance shall be in conformance with the minimum dimensions specified in Table 8-2.

ECSS-Q-ST-70-12_1200121

Table 8-2: Minimum as-manufactured dimensions of sculptured flex conductor

	Thick initial copper		Thin initial copper	
	initial copper	etched copper	initial copper	etched copper
Initial copper thickness	300 µm		250 µm	
Track width for initial copper	400 µm		300 µm	
Insulation distance for initial copper	500 µm		400 µm	
Connection finger width	500 µm		350 µm	
Etched thickness		150 µm		100 µm
Track width for etched copper		300 µm		200 µm
Insulation distance for etched copper		350 µm		250 µm

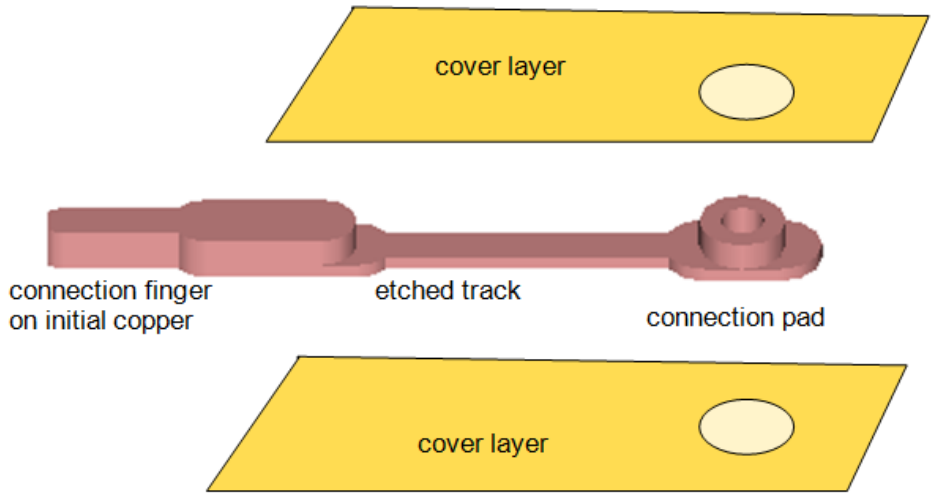


Figure 8-6: Build-up of sculptured flex circuit

8.7.4 Connection finger

ECSS-Q-ST-70-12_1200427

a. The connection fingers may be bend in a staggered pattern to fit the footprint of the connecting PCB

NOTE An example of staggered bend connection fingers is shown in Figure 8-7.

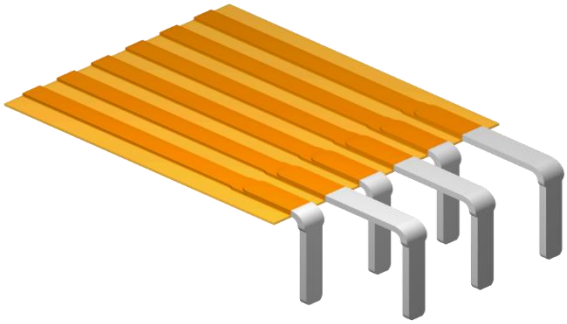


Figure 8-7: Connection finger of sculptured flex circuit

8.7.5 Through-holes

ECSS-Q-ST-70-12_1200122

a. Through-holes shall be manufactured by drilling into the initial copper thickness.

ECSS-Q-ST-70-12_1200428

b. Oblong pads should be used only in case circular pads cannot be used due to insufficient spacing in one direction.

ECSS-Q-ST-70-12_1200123

c. The drill diameter of the hole shall be ≥ 0,5 mm.

ECSS-Q-ST-70-12_1200429

d. Component holes with circular pads should have a pad diameter as-designed of ≥ 0,4 mm larger than the drilled diameter.

NOTE This results in an as-designed annular ring of 200 µm.

ECSS-Q-ST-70-12_1200430

e. The minimum as-manufactured annular ring on the component side may be 0.

NOTE The as-manufactured annular ring is indicated with the red arrow in Figure 8-8.

ECSS-Q-ST-70-12_1200124

f. There shall be no adhesive inside the hole.

NOTE Adhesive can be squeezed from underneath the cover layer and misregistration of the cover layer on component side can risk to have adhesive inside the hole.

ECSS-Q-ST-70-12_1200431

g. The minimum as-designed pad diameter on the solder side should be ≥ 0,7 mm larger than the drilled diameter.

ECSS-Q-ST-70-12_1200125

h. The annular ring on solder side shall be in compliance with Table 10-59 of ECSS-Q_ST-70-60.

NOTE The pad diameter on solder side is indicated with the blue arrow in Figure 8-8.

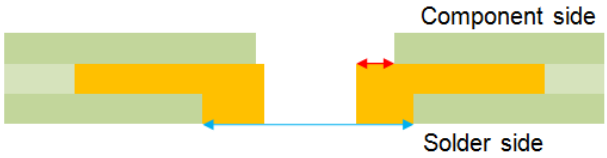


Figure 8-8 Side view of a component hole for sculptured flex

8.7.6 Bending radius

ECSS-Q-ST-70-12_1200126

a. The bending radius of sculptured flex circuit shall be ≥ 12x thickness and ≥ 3,2 mm.

ECSS-Q-ST-70-12_1200127

b. Bending shall only occur on the etched track.

ECSS-Q-ST-70-12_1200128

c. Bending shall not occur on the full thickness copper.

NOTE The etched track is shown in Figure 8-6 and copper thickness is specified in Table 8-2.

9 Rigid-flex PCBs

9.1 Overview

Multiple flex laminates with cover layers can be incorporated within a PCB. Figure 9-1 shows an example of 1 flex laminate incorporated in the rigid-flex PCB.

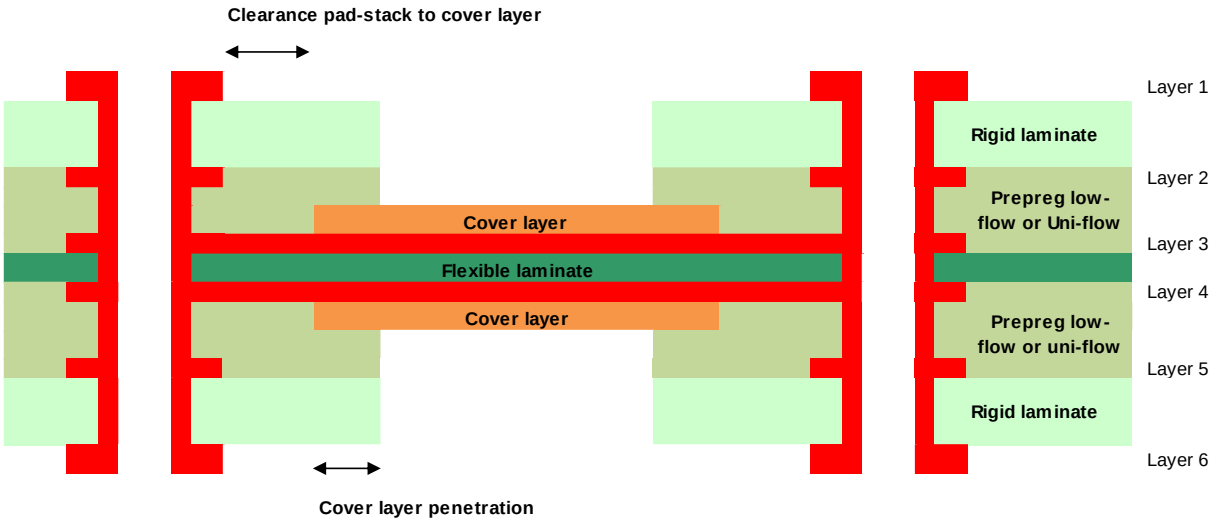


Figure 9-1 Example of a build-up of a 6 layer symmetric rigid-flex

9.2 General

ECSS-Q-ST-70-12_1200129

a. The design of rigid parts of a rigid-flex PCBs shall be performed in conformance with the requirements from the clause 7.

ECSS-Q-ST-70-12_1200130

b. The design of flex parts of a rigid-flex PCBs shall be performed in conformance with the requirements from the clause 8.

NOTE Design of rigid and flex parts include track width and spacing.

ECSS-Q-ST-70-12_1200131

c. No termination zone shall be defined for the flex section of a rigid-flex PCB.

9.3 Build-up

ECSS-Q-ST-70-12_1200132

a. The symmetry of the build-up shall be in conformance with the requirement 7.1.1a and 7.1.1b.

ECSS-Q-ST-70-12_1200133

b. In the rigid part of the PCB the flex layers shall be bonded by using prepreg.

ECSS-Q-ST-70-12_1200134

c. In the rigid part of the PCB adhesive shall not be used for bonding of the flex layers.

NOTE There are different manufacturing principles that either use standard flow prepreg as used in rigid boards, or modified no-flow type prepregs. No-flow prepreg cannot be used for resin filling of blind vias, and thereby a mix of prepreg styles can be necessary, when a sequential rigid-flex board is designed.

ECSS-Q-ST-70-12_1200135

d. Copper foil thickness of 70 µm shall not be used on flex or rigid layers bonded with no-flow prepreg unless it is recorded as a Review Item in the PCB definition dossier.

NOTE This can add risk for bonding in cover layer bond cycles or the bond cycle with no-flow prepreg.

ECSS-Q-ST-70-12_1200136

e. The number of flex laminates shall be ≤ 6, which can result in 12 copper layers when double sided flex laminates are used.

NOTE Flex layers can be bonded together by using a bondply cover layer with adhesive on both sides. The advantage of this is improved cleanliness between layers and improved control of impedance. The disadvantage is the flexibility and bending radius of the flex stack.

ECSS-Q-ST-70-12_1200137

f. Three flex laminates or more in the build-up shall be recorded as Review Item in the PCB definition dossier.

NOTE Three flex laminates can include 6 copper layers.

ECSS-Q-ST-70-12_1200138

g. Except the cases specified in the requirement 9.3h the rigid-flex PCB shall be designed and delivered with a support frame.

ECSS-Q-ST-70-12_1200432

h. The rigid-flex PCB may be delivered without a support frame in case the following conditions are met:

1. the PCB manufacturer delivers the rigid-flex PCB with a support that prevents damage to the PCB during shipment, and
2. the customer implements a support structure that prevents damage to the rigid-flex PCB during assembly and handling.

9.4 Cover layer

ECSS-Q-ST-70-12_1200139

a. The cover layer shall be placed in the flexible section of the PCB.

ECSS-Q-ST-70-12_1200140

b. The cover layer shall not be placed in the rigid section of the PCB, except for the interface to the flex section as specified in the requirement 9.4c.

ECSS-Q-ST-70-12_1200141

c. The cover layer shall extend into the rigid section of the PCB by ≥ 1,5 mm.

ECSS-Q-ST-70-12_1200433

d. In a multilayer rigid-flex PCB where flex laminates are bonded together with bondply, the ends of the cover layers and bondply should be off-set in the rigid section by 1 mm to prevent a line of weakness.

ECSS-Q-ST-70-12_1200142

e. The cover layer shall not overlap the internal pad of a via in the rigid section.

NOTE This is done to reduce stress on the hole wall due to high Z-expansion of cover layer adhesive and to maintain a good hole quality by not using dissimilar materials.

9.5 Interface of rigid part and flexible part

ECSS-Q-ST-70-12_1200143

a. The hole wall shall be ≥ 2 mm separated from the edge of the rigid part of the PCB.

NOTE A larger separation between hole wall and edge of the rigid part is recommended in case it fits within the PCB lay-out.

ECSS-Q-ST-70-12_1200144

b. Tracks on flex layers shall not change direction within 1 mm on both sides of the interface between flex and rigid sections.

NOTE Tracks extend 1 mm out of the rigid part of the PCB before they change direction. Tracks extend 1 mm into the rigid part of the PCB before they change direction.

ECSS-Q-ST-70-12_1200145

c. Bending of the flex section shall be performed in conformance with the requirements from the clause 8.6.

ECSS-Q-ST-70-12_1200146

d. Bending of the flex PCB shall not occur within 1,5 mm from the rigid section of the PCB.

9.6 Pads

ECSS-Q-ST-70-12_1200147

a. The diameter of the pads on flex layers in the rigid section of the PCB shall be ≥ 0,6 mm larger than the diameter of the drilled hole except the case specified in the requirements 9.6b.

ECSS-Q-ST-70-12_1200434

b. The diameter of pads on flex layers in the rigid section of the PCB may be < 0,6 mm larger than the diameter of the drilled hole in case the following conditions are met:

1. the annular ring as-manufactured is achieved in conformance with requirement 10.2a of ECSS-Q-ST-70-60, and
2. it is recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200148

c. Non-functional pads on flex laminate shall be in conformance with requirement 7.5.2c.2.

10
Thermal rules and heat sinks

10.1 Overview

Heat sinks have the purpose of improving the thermal management of the PCB especially in the vicinity of components with a high thermal dissipation or current carrying tracks. Heat sinks also have an effect on in-plane thermal expansion.

Metal inserts, such as invar or molybdenum, can also be used to restrict in plane thermal expansion under large leadless components, such as LCC and AAD. Metal inserts are considered as heat sinks and are covered by this clause.

Heat sinks can affect the solderability of the PCB as they increase the thermal mass.

10.2 General requirements

ECSS-Q-ST-70-12_1200149

a. Design with heat sink shall be recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200150

b. Heat sinks shall be electrically connected in conformance with the requirement 13.5a.

10.3 Specific requirements for external heat sink

10.3.1 Overview

Heat sinks can be smaller, larger or the same size as the PCB.

10.3.2 Construction of the interface between PCB and heat sink

ECSS-Q-ST-70-12_1200151

a. Heat sink shall be made of copper or aluminium core bonded to the outer layer of PCB.

NOTE Bonding can be done by no-flow prepreg, cover layer or adhesive.

ECSS-Q-ST-70-12_1200152

b. The copper or aluminium core shall have a protective layer to prevent corrosion.

NOTE The type of protective layer is specified in the PCB definition dossier. Examples of protective layers to prevent corrosion are anodization, alodine, nickel plating, gold plating. These corrosion protections can have specific drawbacks for further PCB processing.

ECSS-Q-ST-70-12_1200153

c. The heat sink shall be manufactured by milling or etching.

NOTE Milling is preferred because it can provide better edge definition. Etching of thick layers result in a wider edge profile.

ECSS-Q-ST-70-12_1200154

d. The PCB manufacturer shall inform the supplier of the method of bonding the heat sink.

NOTE This is done to verify the thermal properties of the assembly.

ECSS-Q-ST-70-12_1200155

e. Minimum two non-plated through-holes shall be diagonally placed on the PCB for registration of the heat sink.

ECSS-Q-ST-70-12_1200156

f. No conductive surface pattern shall be present beneath the heat sink, except the case specified in the requirement 10.3.2g.

ECSS-Q-ST-70-12_1200435

g. A conductive surface pattern may be present beneath the heat sink in case:

1. the adhesion of the heat sink to the external layer is ensured,
2. the insulation of tracks of different potential is ensured,
3. the surface area of tin-lead under the heat sink is minimised, and
4. it is recorded as a Review Item in the PCB definition dossier.

NOTE 1 For conditions specified in the requirements 10.3.2g.1 and 10.3.2g.3 to ensure adhesion on conductive surface pattern and tin-lead, it is an option to bond a cover layer on tin-lead or to perform selective stripping of tin-lead and bond with prepreg.

NOTE 2 For condition specified in the requirement 10.3.2g.2 to ensure insulation, it is an option to

bond a cover layer on conductive surface pattern.

NOTE 3 The behaviour of tin-lead on a PTH pad during assembly can affect the design of the bonding method of the heat sink.

10.3.3 Dimensional requirements

ECSS-Q-ST-70-12_1200157

a. The mechanical stability of individual clearances of the pattern of the heat sink shall be recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200158

b. Distance between 2 clearances shall be ≥ 1,5 mm along straight edges.

NOTE Distance along straight edges is indicated as “Iz1” in Figure 10-1.

ECSS-Q-ST-70-12_1200159

c. The length of the straight edges shall be reviewed for mechanical stability in conformance with requirement 10.2a.

ECSS-Q-ST-70-12_1200160

d. Distance between 2 clearances shall be ≥ 1,0 mm between circular edges.

NOTE Distance between circular edges is indicated as “Iz2” in Figure 10-1.

ECSS-Q-ST-70-12_1200161

e. Distance between pads on the PCB and the edge of the clearance of the heat sink shall be ≥ 0,3 mm.

NOTE Distance between pads on the PCB and the edge of the clearance of the heat sink is indicated as “i” in Figure 10-1.

ECSS-Q-ST-70-12_1200162

f. Distance between a clearance in the heat sink and the edge of the PCB laminate shall be ≥ 0,5 mm.

NOTE Distance between a clearance in the heat sink and the edge of the PCB laminate is indicated as“b6” in Figure 10-1.

ECSS-Q-ST-70-12_1200163

g. Distance between the clearance in the heat sink and the edge of the heat sink shall be ≥ 1,5 mm.

NOTE Distance between the clearance in the heat sink and the edge of the heat sink is indicated as“b7” in Figure 10-1.

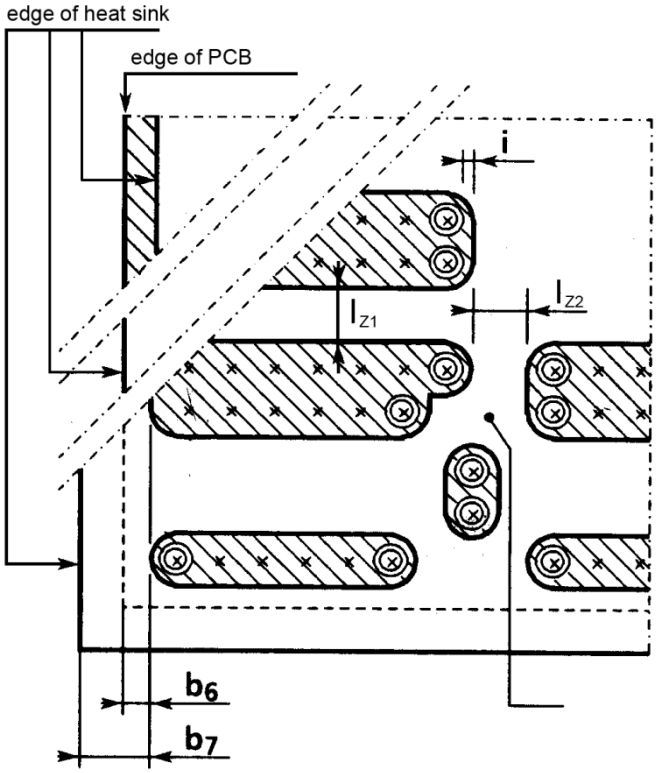


Figure 10-1: Lay out of heat sink and PCB

10.4 Specific requirements for internal heat sink

10.4.1 General

ECSS-Q-ST-70-12_1200164

a. Heat sink shall be made of copper, copper-molybdenum-copper or CIC.

NOTE 1 Heat sinks can be foils covering the entire surface of a layer or inserts placed locally under a specific component.

NOTE 2 Heat sinks that consist of a copper layer can be made by using copper foil or copper clad laminate. The advantage of a foil is the ability of prepreg to fill clearances from both sides. The advantages of copper clad laminate is better registration, ease in handling and processing and the possibility of more complex electrical routing in case of split ground planes on heat sinks.

ECSS-Q-ST-70-12_1200436

b. There should be no tracks on the same layer as a heat sink.

NOTE Local heat sink inserts can have tracks on the same layer.

10.4.2 Cu thickness and type

ECSS-Q-ST-70-12_1200165

a. Foils and laminates with as-designed copper thickness ≥ 105 µm shall be designed in conformance with the requirements from clause 10 for heat sinks.

ECSS-Q-ST-70-12_1200166

b. The number of copper heat sink layers shall be ≤ 2.

ECSS-Q-ST-70-12_1200167

c. The thickness of copper layer shall be 105 µm to 210 µm in case 2 layers of heat sinks are used.

ECSS-Q-ST-70-12_1200168

d. The thickness of copper heat sink shall be ≤ 700 µm when 1 layer of heat sink is used.

ECSS-Q-ST-70-12_1200169

e. The copper foil shall be procured in conformance with the requirements from the IPC-4562.

NOTE Types of copper foil types commonly used are: HTE grade 3, and JTC grade 1.

ECSS-Q-ST-70-12_1200170

f. Copper foil for heat sinks shall be in conformance with the requirement 7.1.2i.

NOTE High quality copper foil type HTE or JTC is necessary to ensure reliable electrical connection with vias.

10.4.3 CIC and Molybdenum inserts

ECSS-Q-ST-70-12_1200437

a. CIC may be used to reduce in plane CTE.

NOTE 1 Material designation IPC-CF-152/2 CIC W 6D as specified in IPC-CF-152B.

NOTE 2 Most common composition of CIC is 12,5% copper, 75% invar, 12,5% copper.

ECSS-Q-ST-70-12_1200171

b. The thickness of CIC shall be ≤ 150 µm.

ECSS-Q-ST-70-12_1200172

c. The number of heat sink layers with CIC shall be ≤ 2.

ECSS-Q-ST-70-12_1200173

d. The CIC layers shall have a tolerance of ≤ ± 10%.

ECSS-Q-ST-70-12_1200438

e. Molybdenum may be used to reduce in plane CTE and improve heat transfer.

NOTE Standard specification for molybdenum is according to ASTM-B386-03.

ECSS-Q-ST-70-12_1200174

f. The thickness of molybdenum inserts shall be 0,5 mm.

ECSS-Q-ST-70-12_1200175

g. The number of layers containing molybdenum inserts shall be ≤ 1.

ECSS-Q-ST-70-12_1200176

h. The molybdenum inserts shall have a tolerance of ≤ ± 0,035 mm.

10.4.4 Dimensional requirements

ECSS-Q-ST-70-12_1200177

a. The mechanical stability of individual clearances of the pattern of the heat sink shall be recorded as a Review Item in the PCB definition dossier.

NOTE Clearances that are separated by a long straight edge known as ‘thin web’ are a concern for mechanical stability.

ECSS-Q-ST-70-12_1200178

b. For heat sinks that are designed to be within the edge of the PCB, the distance between the edge of the heat sink and the edge of the PCB shall be ≥ 1,5 mm.

NOTE Sufficient resin from the edge of the heat sink to the edge of the PCB ensures adequate insulation and mechanical stiffness needed for subsequent milling of the PCB.

ECSS-Q-ST-70-12_1200179

c. Heat sinks that are aligned with the edge of the PCB or exposed on one side by depth controlled milling shall have a protective coating for corrosion protection.

NOTE Example of protective coating is nickel plating.

ECSS-Q-ST-70-12_1200180

d. The distance between a plated hole and the heat sink shall be in conformance with the requirement 13.8.2k and values specified in the Table 13-3.

ECSS-Q-ST-70-12_1200181

e. The distance between two circular clearances shall be ≥ 2x the copper thickness of the heat sink.

ECSS-Q-ST-70-12_1200182

f. In case the distance between the two clearances is less than two times the copper thickness, the remaining metal shall be removed.

NOTE This remaining metal is named “thin web”. This is illustrated in Figure 10-2.

ECSS-Q-ST-70-12_1200183

g. In case holes are overlapping, the angle of intersection, as specified in Figure 10-3, shall be minimum 110°.

NOTE This applies to etching as well as drilling and milling.

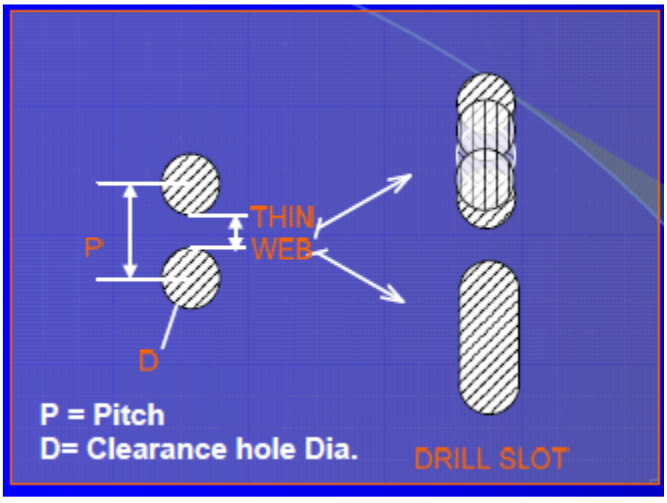
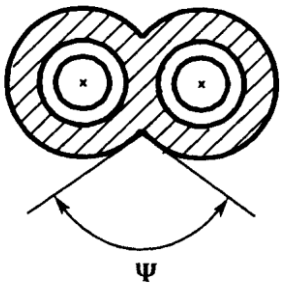


Figure 10-2: drilling holes and slots in internal heat sink



ECSS-Q-ST-70-12_1200184

Figure 10-3: Angle of intersection of overlapping holes

11
HDI PCBs

11.1 Overview

This clause defines additional technology for HDI PCBs, such as microvias. In addition, this clause specifies deviations for the following features:

a. For dielectric thickness of microvia layers on HDI PCBs, a deviation to requirement 7.1.3e is specified in requirement 11.4.1h.

b. For copper foil thickness on microvia layers on HDI PCBS, a deviation to requirement 7.1.2c is specified in requirement 11.4.1e.

c. For fine pitch track width and spacing of impedance controlled routing to 1 mm pitch AAD on HDI PCBs, a deviation to requirement 7.4.5a is specified in requirement 11.5.5a.

d. <<deleted>>

e. For aspect ratio on High Speed HDI PCBs, a deviation to requirement 7.3.5a is specified in recommendation 11.6b.

11.2 <<deleted>>

ECSS-Q-ST-70-12_1200439

a. <<deleted>>

ECSS-Q-ST-70-12_1200185

b. <<deleted>>

ECSS-Q-ST-70-12_1200186

c. <<deleted>>

11.3 Microvia technology

ECSS-Q-ST-70-12_1200187

a. <<deleted>>

Figure 11-1: <<deleted>>.

11.4 Microvias

11.4.1 Build-up of microvia layers

ECSS-Q-ST-70-12_1200188

a. <<deleted>>

ECSS-Q-ST-70-12_1200189

b. <<deleted>>

ECSS-Q-ST-70-12_1200440

c. Dummy copper plane filling should be used on internal microvia layers.

NOTE Dummy copper is used to establish a lay-out that is as homogeneous as possible. This is done to reduce embedding of copper circuit into the resin and to maximise the dielectric thickness.

ECSS-Q-ST-70-12_1200441

d. <<deleted>>

ECSS-Q-ST-70-12_1200442

e. On microvia layers, the external and internal copper layers may be designed using basic copper thickness of ≤ 17 µm.

NOTE 1 This is a deviation from the requirement 7.1.2c.

NOTE 2 The benefit of reduced copper thickness is to improve etching accuracy of fine features. To ensure an insulation of 60 µm between layers it can be beneficial to use thin copper on the internal microvia layer to avoid planarization processes.

NOTE 3 The potential lower peel strength of thin copper foil can lead to separation from the dielectric. This can be mitigated by peel strength measurement on coupon, the qualification of bare PCB technology using thermal cycling and assembly verification.

NOTE 4 Thin copper foil is more fragile, therefore a rigid carrier is used during manufacture. When the core surface is non-planar, it is possible the rigid carrier does not conform well to the non-planar prepreg causing lack of adhesion or deformation of the copper foil. The following features can cause non-planarity of the core surface: rigid-flex constructions, high via density, high track density, high copper thickness, use of no-flow prepreg.

ECSS-Q-ST-70-12_1200443

f. Microvia layers shall be designed with copper foil and prepreg.

ECSS-Q-ST-70-12_1200190

g. Insulation of microvia layers shall be performed by using 2 sheets of prepreg in conformance with the requirement 7.1.3a, except for the case specified in 11.4.1k.

ECSS-Q-ST-70-12_1200191

h. The as-manufactured insulation in Z direction in microvia layers shall be ≥ 60 µm in conformance with Table 13-3, except for the case specified in 11.4.1k.

NOTE See also Table 10-9 of ECSS-Q-ST-70-60.

ECSS-Q-ST-70-12_1200192

i. The as-designed insulation in Z direction in microvia layers should be 100 µm.

NOTE The typical build-up to achieve ≥ 60 µm as-manufactured and a designed insulation of 100 µm, is by using 2 sheets of prepreg type 106.

ECSS-Q-ST-70-12_1200193

j. For voltages >30V microvia layers shall not have superimposed conductors.

NOTE This is done to ensure that insulation in Z direction is in conformance with the Table 13-3.

k. Insulation of microvia layers may be performed by using 1 sheet of prepreg in case the following conditions are met:

1. the as-designed dielectric thickness is ≤ 95 µm,
2. the as-manufactured dielectric thickness is ≥ 40 µm,
3. the maximum voltage is 30 V,
4. method 3 is used for double insulation of critical nets, as specified in 13.9.3.1b,
5. the prepreg is procured in conformance with Appendix A of IPC-4101, as specified in Annex I of ECSS-Q-ST-70-60,
6. the cleanliness of lay-up processes and its evaluation by THB testing are in conformance with clause 6.7.2 of ECSS-Q-ST-70-60,
7. copper distribution and thickness after plating are review items in the MRR,
8. The build-up is covered by qualification.

NOTE At the time of issuing the revision 1 of this standard, no qualification was performed on single ply prepreg. The permission is described to future proof the technology.

l. In case of landing a microvia on a non-plated layer, the following conditions shall be met:

1. the copper foil thickness is ≥ 17 µm,

2. the microvia lands on the side of the copper foil that is treated by the PCB manufacturer.

NOTE 1 To achieve condition 2 of requirement l the build-up is with prepreg and copper foil on external core layers, and not with a laminate. In the latter case, the microvia would land on the rough side of the foil. This is also described in requirement f.

NOTE 2 See Figure 3-3 for an example of full and half microvia layers.

m. For polyimide HDI technology as specified in 11.6a, the build-up of full microvia layers shall be maximum 2 on each side of the PCB.

n. For High Speed HDI technology as specified in 11.6b, the build-up of microvia layers may be 3 full and one half microvia layer.

NOTE See Figure 3-3 for an example of full and half microvia layers.

o. For polyimide HDI technology as specified in 11.6a, microvias shall be staggered in case of ≥ 2 microvia layers.

NOTE Microvias can be stacked. This is considered higher risk for failure at the landing pad.

p. Microvias shall not be stacked on the buried via.

q. Microvias should not be superimposed above buried vias.

r. In case microvias are superimposed above buried vias, the configuration shall be covered by IST coupon design.

s. In case microvias are superimposed above buried vias, the IST coupon design should implement possible eccentricity due to misregistration.

NOTE An example of coupons design that investigates possible eccentricity of microvias that are superimposed above core vias is shown in Figure 11-2.

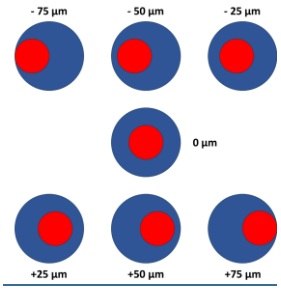


Figure 11-2: Example of an accelerated coupon test design with different levels of eccentricity of the superimposed microvia (red) to the underlying core via (blue)

11.4.2 Design of microvias

ECSS-Q-ST-70-12_1200194

a. The as-designed aspect ratio of a microvia shall meet the following conditions:

1. it is determined by the sum of the dielectric thickness calculated for the build-up (td) and copper foil thickness (tc), divided by the as-designed drilled diameter (d), in conformance with the formula: (td+tc)/d,

2. it is ≤ 0,8.

NOTE It is good practice to measure the as-manufactured aspect ratio. This can differ from the as-designed aspect ratio because of resin flow causing local thinner and thicker areas, and copper thickness and etching pattern on the landing layer.

ECSS-Q-ST-70-12_1200195

b. The microvia shall be laser drilled.

ECSS-Q-ST-70-12_1200196

c. The microvia shall be filled with copper, except for the case in requirement 11.4.2i.

ECSS-Q-ST-70-12_1200197

d. <<deleted>>

ECSS-Q-ST-70-12_1200198

e. <<deleted>>

ECSS-Q-ST-70-12_1200444

f. Microvia diameter should be ≥ 175 µm as-designed, except for the case of requirement 11.4.2h.

NOTE 1 This diameter is covered by an existing qualification at the time of issuing the revision 1 of this standard.

NOTE 2 The tolerance is small therefore the diameter as-manufactured is approximately identical.

ECSS-Q-ST-70-12_1200199

g. <<deleted>>

h. Reduced microvias may have a diameter of ≥ 150 µm as-designed.

NOTE It is good practice to manufacture reduced microvia diameters on state-of-the-art process equipment that are optimised for fluid dynamics.

i. A half-layer microvia may be non-copper filled.

NOTE See Figure 3-3 for an example of full and half microvia layers.

j. In case of a half-layer microvia it shall meet the following conditions:

1. the landing pad nominal thickness is ≥ 17 µm,
2. the copper plating thickness is ≥ 25 µm,
3. it is not stacked.

Figure 11-3: <<deleted>>

11.4.3 Pad design for microvia

ECSS-Q-ST-70-12_1200200

a. The diameter of external pads shall be the diameter of the ablated hole plus ≥ 0,15 mm.

ECSS-Q-ST-70-12_1200445

b. The diameter of external pad may be the diameter of the ablated hole plus ≥ 0,1 mm in case the following conditions are met:

1. the annular ring is 10 µm in conformance with ref F of Table 10-2 of ECSS-Q-ST-70-60, and
2. the diameter of external pad is recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200201

c. The diameter of internal pads shall be the diameter of the ablated hole plus ≥ 0,15 mm.

NOTE It is important to consider the complexity of the PCB and the PCB manufacturing tolerances for the design of the diameter of the pads.

ECSS-Q-ST-70-12_1200446

d. The internal pad of a staggered microvia and the pad of the buried via may be placed tangent to each other.

NOTE Assuming 100 µm and 10 µm for the annular ring as-manufactured of the pads of blind via and microvia, this results in a distance of about 110 µm.

11.4.4 <<deleted>>

ECSS-Q-ST-70-12_1200202

a. <<deleted>>

ECSS-Q-ST-70-12_1200203

b. <<deleted>>

ECSS-Q-ST-70-12_1200204

c. <<deleted>>

11.5 Core PCB for HDI

11.5.1 General build-up

ECSS-Q-ST-70-12_1200205

a. For HDI PCB, the core PCB shall be type non-sequential rigid.

ECSS-Q-ST-70-12_1200206

b. <<deleted>>

ECSS-Q-ST-70-12_1200207

c. The number of copper layers in the core PCB shall be in conformance with the requirements from clause 7.3.4.

ECSS-Q-ST-70-12_1200208

d. PCB thickness shall be in conformance with the requirements from the clause 7.3.

ECSS-Q-ST-70-12_1200209

e. Copper thickness of internal layers that do not include microvias may be ≥ 12 µm.

NOTE This allows for the use of 12 µm copper foil for fine pitch, in addition to the thicknesses from requirement 7.1.2c.

11.5.2 Annular ring on vias for fine pitch footprint

ECSS-Q-ST-70-12_1200447

a. <<deleted>>

Figure 11-4: <<deleted and moved to clause 7.5.3 as Figure 7-3>>

11.5.3 Track width and spacing on external layers

ECSS-Q-ST-70-12_1200448

a. <<deleted>>

ECSS-Q-ST-70-12_1200449

b. <<deleted>>

ECSS-Q-ST-70-12_1200210

c. <<deleted>>

11.5.4 Track width and spacing on internal layers for impedance control and routing to AAD

ECSS-Q-ST-70-12_1200450

a. <<deleted>>

ECSS-Q-ST-70-12_1200211

b. <<deleted>>

Figure 11-5: <<deleted>>

11.5.5 Track width and spacing on internal layers for differential pair routing within the footprint of 1,0 mm pitch AAD

ECSS-Q-ST-70-12_1200451

a. On internal layers the width and spacing of tracks may be reduced to 70 µm, in case the following conditions are met:

   1. the tracks route an edge-coupled differential pair between via pads for a 1 mm pitch AAD,
   2. the current is ≤ 50 mA and voltage is ≤ 10 V,
   3. the spacing and track width are increased outside the footprint of the AAD to normal values in conformance with the requirements from clause 7.4.6,
   4. the manufacturing tolerance for <90 µm spacing is within -10% / +20%,
   5. the manufacture of the tracks is inspected prior to lamination for conformance with designed track width and spacing within the required tolerance, and
   6. it is recorded as a Review Item in the PCB definition dossier.

      NOTE 1 NOTE to 11.5.5a.4: This reduces the tolerances from the standard ±20% as specified in the Table

7-3. This provides a minimum as-manufactured insulation distance of 63 µm as specified in the Table 13-3.

NOTE 2 NOTE to 11.5.5a.5: The inspection can be performed by AOI and by dimensional measurement under microscope on the foot of the track for spacing and track width.

NOTE 3 The reduced feature sizes increase the risk of errors during etching resulting in open or short circuits.

11.5.6 Aspect ratio of core vias

ECSS-Q-ST-70-12_1200452

a. <<deleted>>

b. The drill diameter of core vias shall be ≥ 350 µm, except for the case in requirement 11.5.6c.

c. In case of reduced drill diameter of core vias, the following conditions shall be met:

1. The drill diameter is ≥ 250 µm

2. The aspect ratio is ≤ 7

NOTE It is important to verify conformance with the PID of the PCB manufacturer at an early stage of the design process, as specified in 5.2e. At the time of issuing the revision of this standard, the qualified domain covered for a core via diameter of 350 µm.

Figure 11-6: <<deleted>>

11.6 HDI design features

a. Polyimide HDI PCB design shall implement the dimensional features from the Table 11-1.

NOTE At the time of issuing the revision 1 of this standard, the Polyimide HDI technology is qualified.

b. Standard PCB design features for polyimide HDI PCBs should implement the dimensions from Table 11-2.

c. High speed HDI PCB design should implement the dimensional features from the Table 11-1 and Table 11-2.

NOTE At the time of issuing the revision 1 of this standard, the High Speed HDI technology is under evaluation.

d. In case backdrilling of vias is performed on high speed HDI PCBs, it shall be in confromance with clause 12.9.

NOTE At the time of issuing the revision 1 of this standard, backdrilling has not been evaluated on polyimide technology.

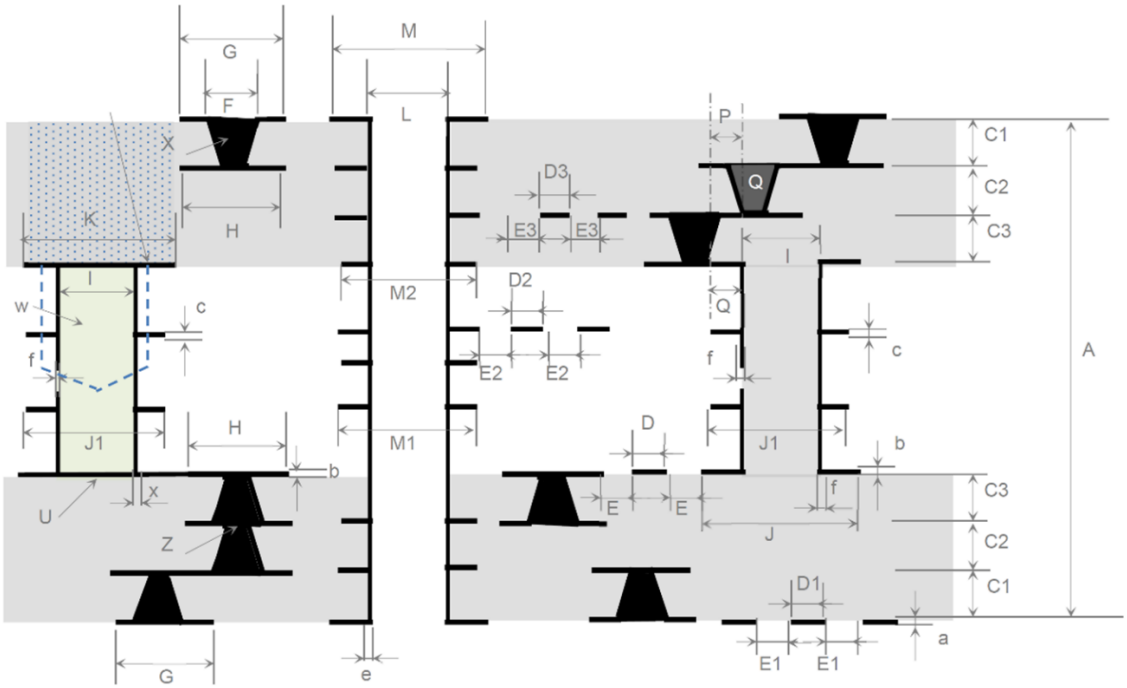


Figure 11-7: Build-up with design features for HDI

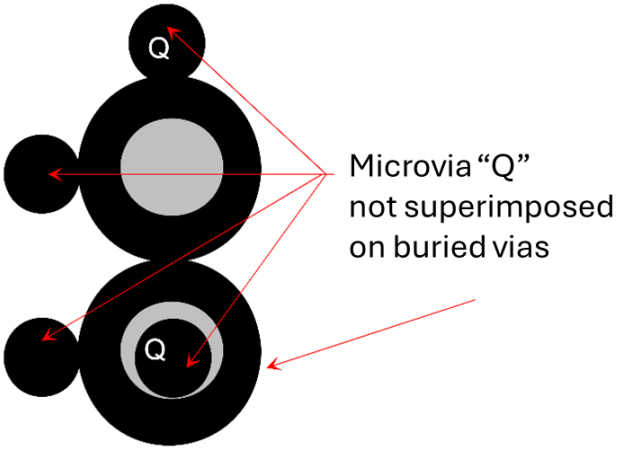


Figure 11-8: Top down view of microvias and buried via configurations

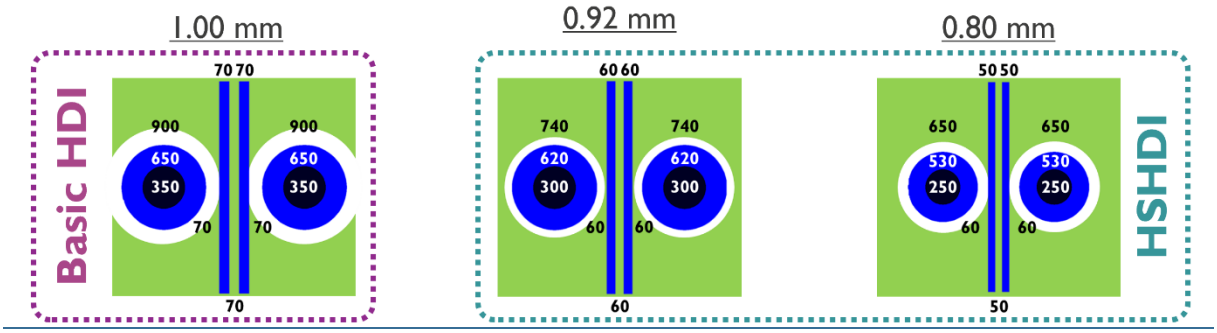


Figure 11-9: Top down view buried vias and tracks

Table 11-1: HDI design features

Design feature	Legend	Polyimide HDI	High Speed HDI
Dielectric material		polyimide	high speed
Number of microvia layers		Max 2 (2+n+2)	Max 3,5 (3,5+n+3,5)
Microvia stacked or staggered	Z	staggered	3 stacked possible; 0,5 level uvia is staggered
Microvia on core via		Staggered	Staggered
Microvia superimposed on core via	Q	not superimposed	possible, as per 11.4.1r + r
Microvias plating (inside and outside)	X	Copper filled	Copper filled for sequential laminated uvias; Resin-filled for 0,5 level uvia
Differential pair routing		For ≥1 mm pitch AAD diff pair routing possible For <1 mm pitch AAD only single track routing possible	For ≥0,8 mm pitch AAD diff pair routing possible For <0,8 mm pitch AAD only single track routing possible
Microvia drilling diameter (top opening)	F	175 µm	150 µm
Microvia external pad diameter	H	≥350 µm	≥300 µm
Microvia landing pad diameter (int)	G	≥350 µm	≥300 µm
Track width core external plated layers	D	≥120 µm	≥100 µm
Spacing on plated core layers	E	≥100 µm For core via pad to plane: ≥150 µm	≥100 µm For core via pad to plane: ≥150 µm
Track width external layers	D1	≥150 µm	≥100 µm
Spacing external layers	E1	≥150 µm	≥100 µm
Track width core internal layers	D2	≥70 µm	≥50 µm
Spacing track to track on core internal layers	E2	≥70 µm	≥50 µm
Spacing pad to track on core internal layers		≥70 µm	≥60 µm
Track width internal plated microvia layer	D3	≥120 µm	≥100 µm
Spacing on microvia layers	E3	≥100 µm For microvia pad to plane: ≥150 µm	≥100 µm For microvia pad to plane: ≥150 µm
Copper thickness core via	x	≥30 µm	≥25 µm
Maximum aspect ratio microvias	(C*+a)/F	≤0,8	≤0,8
Dielectric thickness µvia (min) - as manufactured	C1/C2/C3	≥60 µm	≥60 µm
Base copper thickness inner layer core	c	≥17,5 µm	≥17,5 µm

Design feature	Legend	Polyimide HDI	High Speed HDI
Backdrilling on vias		none	Possible on core and through-going vias
Pre filling material for core via	W	Plugging paste	Plugging paste
Cap plating for core via	U	≥5 µm	≥5 µm, if implemented
Buried via drilling diameter (*)	I	≥350 µm	≥250 µm
Max aspect ratio in buried and through-going vias		≤7	≤9
Buried via pad diameter outer core layer	J	≥650 µm	≥530 µm
Buried via pad diameter inner layer	J1	≥650 µm	≥530 µm
Minimum staggered microvia distance (on same net)	P	≥175 µm	≥150 µm
Minimum microvia to core via distance – to avoid superimposed microvias on core via	Q	≥237,5 µm	≥215 µm
Maximum total board thickness	A	≤2,8 mm	≤3 mm
NOTE: Figure 11-7, Figure 11-8 and Figure 11-9 provide the legend.			

Table 11-2: Standard design features for HDI technology

Design feature	Legend	Polyimide HDI	High Speed HDI
Plated through hole external pad diameter (*)	M	≥1050 µm	≥800 µm
Plated through hole internal pad diameter (*)	M1	≥800 µm	≥600 µm
Plated through hole internal pad diameter plated layer (*)	M2	≥800 µm	≥600 µm
Plated through hole drilling diameter (*)	L	≥500 µm	≥300 µm
Copper thickness plated through hole	e	≥25 µm	≥25 µm
Base copper thickness external layer	a	≥12 µm	≥12 µm
Base copper thickness outer layer core	b	≥12 µm	≥12 µm
(*) The drilling and pad diameter sizes are minimum values and have to be combined in order to meet the annular ring requirements.			

12
PCBs for high frequency applications

12.1 Material selection

Table 6-1 presents examples of some materials used for manufacture of RF PCBs. For the selection of materials it is important to consider that materials with good RF performance typically have poorer processing characteristics (e.g. adhesion and resin flow during lamination). High performance RF materials can exhibit lower peel strength of copper. This can affect the assembly. Some RF materials based on PTFE or mixed build-ups can exhibit smear in the drilling process. For material selection it is important to consider the RF properties and the processability of the material. The possibility to mix for instance RF laminate with standard prepreg can provide good processability while maintaining acceptable RF performance.

12.2 Build-up of RF PCB

ECSS-Q-ST-70-12_1200212

a. The build-up of RF PCBs shall be in conformance with requirements from clause 7.1, except the cases specified in the requirements from 12.2b to 12.2e.

ECSS-Q-ST-70-12_1200213

b. For copper cladding and copper foils the requirements 7.1.2h, 7.1.2i shall not apply.

ECSS-Q-ST-70-12_1200453

c. Copper type “electrodeposited - ED” or “rolled and annealed - RA” may be used for copper cladding and copper foils.

ECSS-Q-ST-70-12_1200214

d. For Molybdenum and CIC layers the requirement 7.1.1c shall not apply.

ECSS-Q-ST-70-12_1200215

e. Molybdenum and CIC layers shall not be used in RF PCBs.

12.3 Embedded film resistors

ECSS-Q-ST-70-12_1200216

a. The use of embedded film resistors in internal layers shall be recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200217

b. The tolerance on the as-manufactured resistance value shall be ≤ ±20%.

NOTE Due to the relatively high tolerance, the application of embedded film resistors is limited to line termination.

ECSS-Q-ST-70-12_1200218

c. Embedded film resistors shall be of type NiP or NiCr.

NOTE Type NiP is available from OhmegaPly. Type NiCr is available from Ticer.

ECSS-Q-ST-70-12_1200454

d. A surface resistance of 25 Ω/sq should be used.

ECSS-Q-ST-70-12_1200455

e. A surface resistance of 50 Ω/sq may be used.

NOTE A surface resistance of 25 Ω/sq is achieved on a thicker resistive layer which is beneficial for thermal reliability.

ECSS-Q-ST-70-12_1200456

f. Layers that include embedded film resistors should not be plated.

NOTE This is done to achieve the best accuracy of etching and resistor value as-manufactured.

ECSS-Q-ST-70-12_1200219

g. No more than one plating sequence shall be performed on layers that include embedded film resistors.

ECSS-Q-ST-70-12_1200457

h. All embedded film resistors on a layer should be oriented in a single direction.

ECSS-Q-ST-70-12_1200220

i. The orientation of embedded film resistors shall be recorded as a Review Item in the PCB definition dossier.

NOTE The best etching accuracy is obtained when embedded film resistors are oriented in the direction of the conveyor of the etching process.

ECSS-Q-ST-70-12_1200221

j. The width of an embedded film resistor shall be ≥ 250 µm.

ECSS-Q-ST-70-12_1200222

k. The aspect ratio of length and width of an embedded film resistor shall be ≥ 1.

NOTE A higher aspect ratio achieves better accuracy of the resistive value.

ECSS-Q-ST-70-12_1200223

l. The ratio of length to width of an embedded film resistor shall be ≤ 5.

NOTE 1 A lower ratio achieves better thermal endurance.

NOTE 2 The configurations specified in requirements 12.3d, 12.3e, 12.3k and 12.3l provide embedded film resistor values between 25 Ω and 250 Ω.

ECSS-Q-ST-70-12_1200224

m. Dedicated representative coupons shall be designed to allow verification of the embedded film resistor values on the etched layer before further lamination.

ECSS-Q-ST-70-12_1200225

n. Dedicated representative coupons shall be designed to allow verification of the embedded film resistor values on the as-manufactured PCB as specified in the requirement 15.2d.13.

12.4 Thickness of RF PCB

ECSS-Q-ST-70-12_1200458

a. The thickness of RF PCB as-designed should be ≤ 3 mm.

ECSS-Q-ST-70-12_1200459

b. The thickness of RF PCB as-designed may be > 3 mm in case the following conditions are met:

1. the thickness as-designed is ≤ 5,5 mm,
2. the materials used are not based on PTFE, and
3. it is recorded as a Review Item in the PCB definition dossier.

NOTE High PCB thickness involve a more difficult drilling process, lamination and handling in automated equipment. It is important that the PCB manufacturer confirms the good processability of the materials.

ECSS-Q-ST-70-12_1200460

c. The number of layers for RF PCBs should be ≤ 8.

ECSS-Q-ST-70-12_1200461

d. The number of layers for RF PCBs may be > 8 in case the following conditions are met:

1. the number of layers is ≤ 14, and
2. it is recorded as a Review Item in the PCB definition dossier.

12.5 Track width and spacing

12.5.1 External layers

ECSS-Q-ST-70-12_1200226

a. The spacing and width for external layers of RF PCBs shall be in conformance with the values from Table 7-4.

ECSS-Q-ST-70-12_1200462

b. For RF elements the spacing may be reduced to the values in conformance with Table 12-1 in case:

1. the voltage between nets is ≤ 1 V,
2. no assembly is performed on the RF elements,
3. no critical tracks are included in the RF element,
4. a specific visual inspection and functional measurement of the RF element is performed, and.
5. it is recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200463

Table 12-1: Minimum spacing and width as-designed for RF elements on external layers

Total copper thickness (base + plated) [µm]	17,5≤Th≤50	Th>50
width [µm]	125	200
spacing [µm]	125	200

12.5.2 Internal Layers

ECSS-Q-ST-70-12_1200227

a. The spacing and width for internal layers of RF PCBs shall be in conformance with the values from Table 7-5.

12.6 Pad design

12.6.1 Pad dimensions

ECSS-Q-ST-70-12_1200228

a. Dimensions of the via hole pads shall be in conformance with the requirements from clause 7.5.3.

12.6.2 Non-functional pads

ECSS-Q-ST-70-12_1200229

a. Removal of non-functional pads shall be performed in conformance with the requirements from clause 7.5.1.

12.7 Surface finish

ECSS-Q-ST-70-12_1200230

a. The surface finish for RF PCBs shall be in conformance with the requirements from clause 7.8.1.

12.8 Profiled layers

ECSS-Q-ST-70-12_1200464

a. (deleted)

ECSS-Q-ST-70-12_1200231

b. The use of profiled top layers shall be recorded as a Review Item in the PCB definition dossier.

NOTE Profiled layers can be manufactured by Z-controlled milling or by laminating layers with openings. Profiled top layers can be used to expose a signal circuit on layer 2 in case the top layer is used as ground plane.

ECSS-Q-ST-70-12_1200232

c. The use of profiled aluminium backing used for cooling shall be recorded as a Review Item in the PCB definition dossier.

12.9 Backdrilled vias

a. Z-controlled backdrilling of vias may be used in case:

1. the Z-controlled backdrilling on vias is included on the coupon, and
2. it is recorded as Review Item in the PCB definition dossier.

NOTE Backdrilling is done to avoid antenna effect of the via wall of high speed and high frequency applications.

b. IST coupon design and testing on backdrilled vias should evaluate the interconnect of the functional pad, in conformance with clause 9.5.5.5 of ECSS-Q-ST-70-60.

c. In case backdrilling is performed on core vias of high speed HDI PCBs, it shall be filled with plugging paste.

d. In case backdrilling is performed on through-going vias, it may be non-filled.

e. Backdrilling shall not be performed on PTH for soldering.

f. Backdrilled vias filled with plugging paste should be cap plated.

NOTE This is specified to mitigate the risk of lack of adhesion between plugging paste and prepreg resin that can evolve into dielectric cracks. Cap plating can be done on either side of the backdrilled via.

g. The minimum backdrilled diameter is equal to the via diameter + 250 µm.

h. The minimum diameter of the clearance hole in planes is equal to the via diameter + 750 µm.

i. Adjacent conductors shall not be placed closer to a backdrilled hole than the clearance specified in the requirement 12.9h.

j. On backdrilled vias, the remaining external pad and the functional pad shall not be removed.

k. The stub that is backdrilled shall not include pads in its design.

NOTE The part of the via that is not backdrilled can have pads removed, except for the external and functional pad in conformance with the requirement 12.9j.

l. Shallow backdrilling by removal of 10% of the via stub should not be performed.

NOTE Backdrilling increases stress on the first (functional) interconnect. A long via with an interconnect near the ends creates most stress on that interconnect. The combination of long vias with backdrilling is, therefore, not good practice.

m. The layers superimposed to a backdrilled via shall not include microvias.

NOTE However, these layers can include tracks and planes.

n. The as-manufactured backdrilled stub shall be ≥ 50 µm.

o. The as-designed backdrilled stub shall be as follows:

1. ≥ 150 µm for standard depth tolerance of +/- 100 µm,

2. ≥ 100 µm for reduced depth tolerance of +/- 50 µm.

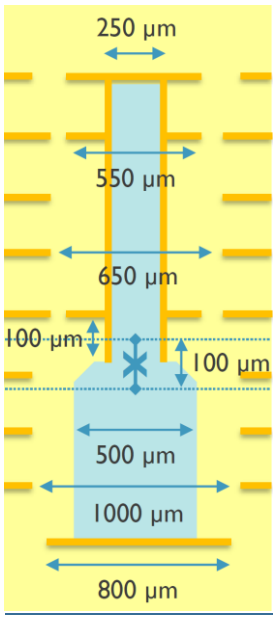


Figure 12-1: Backdrilled hole

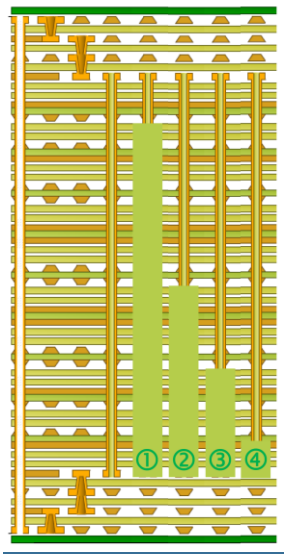


Figure 12-2: Core vias in HDI PCB with four levels of backdrill depth (1 is deep and 4 is shallow)

13
Electrical requirements for PCB design

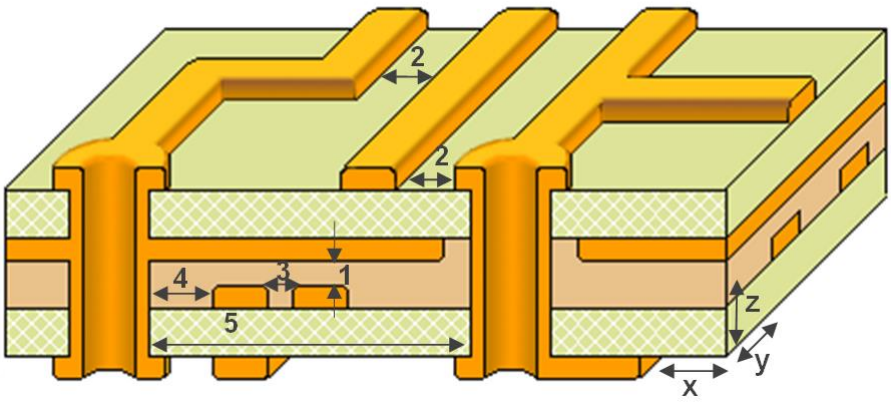
13.1 Overview

Table 13-1 explains the terms “AND”, “OR” and “FOR” as well as the used cross referencing to requirements or notes in Table 13-3, Table 13-4, Table 13-5, Table 13-6, Table 13-7, Table 13-8.

Table 13-1: Legend of terms

Terms	Meaning
AND	The term "AND" indicates that the largest value of the two are used for the relevant voltage. For example: At 50 V in Table 13-3 the X,Y internal spacing is (50x1 µm/V = 50 µm AND 150 µm). In this case 150 µm is the largest value to be used. At 200V the X,Y internal spacing is (200x1 µm/V = 200 µm AND 150 µm). In this case 200 µm is the largest value to be used.
OR	The term "OR" indicates that various options are listed and any of the options can be selected.
FOR	The term "FOR" indicates the perimeter of a technology (for example HDI, fine pitch, uncoated connectors) for which an exemption has been specified to a requirement for standard insulation distance.
Cross-reference to requirement	Cross-referencing to requirements is used to trace back the short descriptions given in the tables to the normative references.
Cross-reference to Note	Cross-referencing to notes is used to trace back the short descriptions given in the tables to informative references.

Figure 13-1 illustrates the insulation distances, numbered 1 to 5, specified in the Table 13-3, Table 13-4, Table 13-5, Table 13-6, Table 13-7 and Table 13-8.



- 1: spacing in Z direction
- 2: spacing in X,Y direction on external layer
- 3: spacing in X,Y direction on internal layer between conductors
- 4: spacing in X,Y direction on internal layer between a conductor and a hole wall
- 5: spacing in X,Y direction on internal layer between hole walls

Figure 13-1: Cross section of PCB with insulation distances.

13.2 General

ECSS-Q-ST-70-12_1200233

a. The term "AND" indicates that the largest value of the two shall be used.

NOTE This is explained in Table 13-1.

13.3 PCB drying

ECSS-Q-ST-70-12_1200234

a. Precautions shall be taken to reduce the moisture level inside the PCB for electrical testing and for measuring electrical characteristics.

NOTE Baking of PCBs is specified in clause 9.2.2 of ECSS-Q-ST-70-60. Polyimide is more hygroscopic than epoxy.

13.4 Electrical characteristics

ECSS-Q-ST-70-12_1200235

a. Insulation resistance between tracks shall be:

1. intralayer: > 10^{10} Ω,
2. interlayer: > 10^{11} Ω.

ECSS-Q-ST-70-12_1200236

b. DWV between tracks shall be 1000 Vrms/mm for intralayer and interlayer.

ECSS-Q-ST-70-12_1200237

c. <<deleted>>

ECSS-Q-ST-70-12_1200238

d. <<deleted>>

Table 13-2: <<deleted>>

ECSS-Q-ST-70-12_1200465

e. For power distribution a copper thickness of 35 µm or more should be used.

NOTE Thin copper tracks of below 35 µm are not suitable for power distribution. Therefore no requirement is specified for thin copper.

ECSS-Q-ST-70-12_1200466

f. In case sequential lamination increases the copper thickness, the current limits may be interpolated or extrapolated.

13.5 Floating metal

ECSS-Q-ST-70-12_1200239

a. Floating or connected conductive patterns shall be in conformance with clauses 6.3.1, 9.2.1 and 9.2.2 of ECSS-E-ST-20-06.

NOTE ECSS-E-ST-20-06 describes the good practice of not having floating metal to prevent surface or internal charging (and discharge effects). It also describes that this risk is limited for a surface of ≤ 1 cm^2, for a capacitance of ≤ 50 pF, for internal conductors embedded in resin and for shielded equipment that receive ≤ 0,02 pA/cm^2.

13.6 Current rating

13.6.1 Overview

Current rating in PCB tracks is based on the temperature increment of tracks compared to the initial PCB temperature when not powered. The method to compute the maximum allowed current is based on families of isothermal curves. These curves cover a range from 1°C up to 100°C and allow to compute the current starting from the copper cross section of the track or vice versa, for the required temperature increment.

The current rating model used in this standard is specified in the document IPC-2152 and the model is presented in graphical form. This standard is an evolution of and supersedes the previous model from IPC-2221A. Another model is presented in CNES/QFT/IN.0113, which is a more conservative model compared to IPC-2152. The mathematical fitting of the three models is presented as a guideline in Annex D. A comparison of the models is shown in Figure D-1.

13.6.2 Requirements for temperature increment

ECSS-Q-ST-70-12_1200240

a. The temperature increment of tracks with respect to the dielectric substrate shall be ≤ 10 °C.

ECSS-Q-ST-70-12_1200467

b. The temperature increment of tracks with respect to the dielectric substrate should be ≤ 5 °C.

ECSS-Q-ST-70-12_1200241

c. The temperature of tracks shall be ≤ 95 °C.

ECSS-Q-ST-70-12_1200468

d. The temperature of tracks should be ≤ 85 °C.

NOTE 1 The increment of 10 °C is based on a temperature of the PCB substrate of 85 °C, in which case the tracks can heat to 95 °C due to self-heating. The self-heating of tracks up to 10°C compared to the substrate, regardless of overall substrate temperature, is based on heritage.

NOTE 2 The temperature of tracks is limited by the evaluation on solder joints as specified in 13.2.1a of ECSS-Q-ST-70-61. However, bare PCBs are tested during qualification to higher temperatures as specified in clauses 9.6 and 9.8 of ECSS-Q-ST-70-60. In addition, thermomechanical properties of PCB materials indicate their robustness to higher temperatures.

13.6.3 Requirements for the model IPC-2152 for current rating

ECSS-Q-ST-70-12_1200242

a. Except for the cases specified in the clause 13.6.4, the model used to calculate temperature increment shall be in conformance with the model for conductor sizing in space environment in conformance with requirements specified in chapters 1 to 5 and appendix A of IPC-2152.

NOTE The mathematical fitting of Figure 5-14 of chapter 5.2.2. of IPC-2152 and the other models is presented as a guideline in Annex D.

ECSS-Q-ST-70-12_1200243

b. Current rating shall apply to the conductive circuit of the as-manufactured PCB including manufacturing tolerances.

NOTE 1 Minimum as-manufactured track width and minimum as-manufactured copper thickness include tolerances specified in Table 7-1 and Table 7-3.

NOTE 2 The graphical representation of the model in IPC-2152 uses nominal dimensions for track width and copper thickness. Chapter A.4.3. of IPC-2152 specifies that the final cross sectional area can be significantly different from the nominal value and needs to be considered.

ECSS-Q-ST-70-12_1200244

c. The PCB configuration for which IPC-2152 is used to calculate current rating, shall be as follows:

1. PCB thickness is more than 1,5 mm.
2. PCB dielectric material has a thermal conductivity as for polyimide or epoxy.
3. PCB total surface area is more than 75x75 mm.

ECSS-Q-ST-70-12_1200245

d. In case the PCB configuration is not in conformance with requirement 13.6.3c, the supplier shall demonstrate the validity of the model used for the current rating.

NOTE In this case the model of IPC-2152 is not considered to be valid.

ECSS-Q-ST-70-12_1200469

e. The temperature rise of a track may be reduced when it is superimposed by a copper plane, in conformance with requirements specified in chapter A.4.6.2. of IPC-2152.

NOTE This chapter specifies that the presence of copper planes is recommended to be used to calculate temperature and to be considered as design margin.

ECSS-Q-ST-70-12_1200246

f. Current rating of a via shall use the same temperature rise as a track with equivalent cross section, in conformance with requirements specified in chapter A.3.4 of IPC-2152.

NOTE This chapter specifies that multiple vias can be used to reach the same cross sectional area of the connecting track.

ECSS-Q-ST-70-12_1200247

g. Multiple tracks in parallel with a spacing of less than 25 mm shall be assessed as parallel conductors, in conformance with requirements specified in chapter A.3.3 of IPC-2152.

NOTE Temperature rise of parallel conductors is determined by calculating the equivalent cross-sectional area and the equivalent current. A summary is also given in paragraph "e" of chapter 4 of IPC-2152.

ECSS-Q-ST-70-12_1200248

h. The current rating of polyimide and epoxy PCBs shall be in conformance with requirements specified in chapter A.4.4 of IPC-2152.

NOTE The chapter A.4.4 in IPC-2152 specifies that there is less than 2% difference.

13.6.4 Amendments to the model from IPC-2152

13.6.4.1 Overview

The requirements of the clause 13.6.4.2 specify amendments with respect to the model for conductor sizing in space environment defined in the clause 13.6.3. These amendments are specified for the current rating and for the temperature rise in the specified configurations.

13.6.4.2 List of amendments

ECSS-Q-ST-70-12_1200249

a. The current rating of external conductors shall be reduced by 10%.

NOTE This is an amendment to chapter A.6 of IPC-2152, which specifies that the current rating of external layers is the same as for internal layers. The justification for the 10% margin is specified in chapter 4.5 of CNES/QFT/IN.0113.

ECSS-Q-ST-70-12_1200250

b. For PCBs with a thickness between 1,5 mm and 1,8 mm, the temperature rise of tracks shall be increased by 20%.

NOTE The mathematical fitting of Figure 5-14 of chapter 5.2.2. of IPC-2152 presented as a guideline in Annex D is valid for PCBs of 1,8 mm. The justification for 20% margin for thinner PCBs is given in chapter A.4.2 of IPC-2152.

ECSS-Q-ST-70-12_1200470

c. Current rating of a via connecting to a copper plane may be 5 times higher.

NOTE This amendment to IPC-2152 is based on chapter 5.3 of CNES/QFT/IN.0113.

ECSS-Q-ST-70-12_1200471

d. Current rating of a track may be 5 times higher in case it is less than 2mm long and connecting a via to a copper plane.

NOTE This amendment to IPC-2152 is based on chapter 5.3 of CNES/QFT/IN.0113.

ECSS-Q-ST-70-12_1200472

e. In case a track leads to a PTH of a connector footprint and the track is reduced in width to pass between pads within the footprint, the current rating may be 2 times higher.

NOTE This is specified to avoid reducing annular ring to allow a wider track to pass in between pads. The increased current rating is justified by the presence of PTHs with copper pads used for assembly of connectors.

13.7 Provisions to prevent open circuit failure on critical tracks

13.7.1 Overview

The open circuit failure of a track in a PCB can lead to loss of function, a random behaviour, or worse, to the propagation of failure. As example, the open circuit failure of a connection in the DC/DC converter feedback loop can cause the loss of the DC/DC function and the failure propagation to the supplied downstream circuits.

13.7.2 Routing

ECSS-Q-ST-70-12_1200251

a. Criticality of tracks shall be as specified in requirement 13.9.2a.

ECSS-Q-ST-70-12_1200473

b. Critical tracks should be routed on a single layer.

ECSS-Q-ST-70-12_1200252

c. A verification shall be performed to reduce the use of vias on critical tracks.

NOTE Some automated routing software can cause unnecessary use of vias.

ECSS-Q-ST-70-12_1200253

d. For a critical track a second redundant via shall be used for the interconnection.

NOTE This is done to prevent open circuit failure of a single interconnection between track, via pad and via barrel.

13.8 Voltage rating

13.8.1 Overview

The insulation distance is determined by the following parameters:

- Voltage rating, as specified in requirements of clause 13.8 for single insulation and in clause 13.9 for double insulation.
- Manufacturing tolerances associated with the copper thickness and track width, as specified in requirements of clause 7.4.1.
- Manufacturing capability as function of copper thickness, as specified in requirements of clause 7.4.3 for external layers and requirements of clause 7.4.4 for internal layers.
- Exemptions made to accommodate HDI designs, as specified in requirements 11.4.1h, 11.4.1i, 11.4.1j, 11.5.2a, 11.5.5a and 11.5.6a.
- Exemptions made to accommodate the use of uncoated connectors, as specified in requirements of clause 13.8.4.
- Tolerances on laminate or prepreg, as specified in requirements of clause 7.1.3.
- Tolerances on hole wall to hole wall registration depending on number of bond sequences, as specified in requirement 13.8.2i and its Note.

All parameters listed are included in Table 13-7 and Table 13-8.

Voltage rating and its associated insulation distances do not include a mitigation for CAF. Designing with minimum distances as specified in this chapter is considered good practice to avoid voltage breakdown in general. However, the specific failure mode of CAF can occur at low distances, in specific environmental conditions and are dependent on the properties of the materials and processes. This CAF failure mode is, therefore, not excluded when designing with minimum insulation distances as specified in this chapter. To analyse and mitigate the risk of CAF, a CAF risk assessment is performed as specified in 7.7.2.q of ECSS-Q-ST-70-60, as well as CAF testing for qualification as specified in 9.7.3 of ECSS-Q-ST-70-60.

13.8.2 General requirements

ECSS-Q-ST-70-12_1200254

a. Voltage rating shall apply to the as-manufactured PCB.

ECSS-Q-ST-70-12_1200255

b. Voltage rating shall apply to the worst-case peak transient voltage.

ECSS-Q-ST-70-12_1200256

c. The supplier shall design the PCB with the insulation distances as specified in the requirements from the clause 13.8.

ECSS-Q-ST-70-12_1200257

d. The insulation distance as function of voltage of the as-manufactured PCB shall be in compliance with values specified in Table 13-3 and Table 13-4.

NOTE 1 The insulation distances also depends on manufacturing capability and tolerances as specified in clause 13.8.1 and specified in Table 7-4 and Table 7-5.

NOTE 2 The Table 13-3 and Table 13-4 cover any elevation. Withstanding voltage between two tracks in air at 87% relative humidity is 1600 V/mm. It is considered that breakdown or arcing cannot occur below this field strength as indicated in the paper by D. P Cullen and G O'Brien (see bibliography).

NOTE 3 The following calculations explain how dimension from the Table 13-3 are derived:

- Spacing track to track – 20 %: 130 µm - 26 µm = 104 µm
- Spacing track to track – 20 %: 120 µm - 24 µm = 96 µm
- Spacing track to track – 10 %: 70 µm - 7 µm = 63 µm
- Minimum as-manufactured Annular Ring + X,Y conductor to conductor: 50 µm + 104 µm = 154 µm
- Minimum as-manufactured Annular Ring with teardops + X,Y conductor to conductor for fine pitch: 25 µm + 96 µm = 121 µm
- Minimum as-manufactured Annular Ring with teardops + X,Y conductor to conductor for polyimide HDI (equivalent to 1,0 mm pitch HDI): 25 µm + 63 µm = 88 µm

ECSS-Q-ST-70-12_1200258

e. Insulation distance in Z direction for superimposed conductors shall be in conformance with values specified in Table 13-3 and Table 13-4.

NOTE The requirements 7.1.3e and 10.3.1 also specify insulation distance of superimposed conductors, as explained in the clause 13.8.1.

ECSS-Q-ST-70-12_1200259

f. Conductors that are not superimposed in Z direction shall be offset in X,Y direction by the distance for X,Y internal conductor-to-conductor spacing as specified in Table 13-3 and Table 13-4.

ECSS-Q-ST-70-12_1200260

g. Insulation distance from conductors to plated or non-plated hole wall shall be in conformance with the values specified in the Table 13-3.

NOTE These insulation distances include an additional spacing of 50 µm to allow for wicking. The requirement does not need to be considered in addition to the requirement for X,Y internal conductor-to-conductor spacing in case the minimum annular ring as-manufactured is 50 µm and the wicking is ≤ 50 µm.

ECSS-Q-ST-70-12_1200261

h. Insulation distance of conductors to PCB edge shall be as for X,Y internal conductor to hole wall, as specified in Table 13-3.

ECSS-Q-ST-70-12_1200262

i. The insulation distance between hole wall of vias on different nets shall be in conformance with the values specified in the Table 13-3.

NOTE The as-manufactured distance is not affected by the number of bond sequences. However, the tolerance on the as-designed distance increases with the number of bond sequences, as specified in the Table 13-7.

ECSS-Q-ST-70-12_1200474

j. The insulation distance between hole wall of vias on the same net may be less than the distances specified in the Table 13-3.

NOTE Vias on the same net can be used for redundancy. This can apply in particular for microvias.

ECSS-Q-ST-70-12_1200263

k. The insulation distance between the heat sink and a hole wall shall be in conformance with values from Table 13-3.

ECSS-Q-ST-70-12_1200264

l. Voltages above 500 V shall be subject to specific qualifications of the design.

ECSS-Q-ST-70-12_1200265

Table 13-3: Minimum insulation distance as function of voltage on as-manufactured PCB for rigid laminate.

V	Z	X,Y external with conformal coating	X,Y external without conformal coating	X,Y internal conductor to conductor	X,Y internal conductor to hole wall	X,Y internal Hole wall to hole wall, Hole wall to heat sink
0-10V	70 µm FOR µvia layer 11.4.1h: 60 µm	120 µm	200 µm	104 um FOR fine pitch 7.4.5a: 96 µm FOR 1 mm pitch HDI 11.5.5a and 11.6a: 63 µm	154 µm FOR reduced pad diameter 7.5.3l and FOR fine pitch 7.4.5a: 121 µm	350 µm
11-30V			300 µm	104 um FOR fine pitch 7.4.5a: 96 µm	FOR 1 mm pitch HDI 11.5.5a and 11.6a: 88 µm	
31-500V	1 µm/V AND 100 µm	2 µm/V AND 160 µm	5 µm/V AND 500 µm	1 µm/V AND 150 µm	(1µm/V+50 um) AND 200 µm	2 µm/V AND 350 µm
Note: The legend to this table is provided in Table 13-1.						

13.8.3 Spacing on flex and rigid-flex laminate

ECSS-Q-ST-70-12_1200266

a. The spacing of conductors on flex laminate in the rigid section shall be in conformance with values for X,Y internal specified in the Table 13-3.

NOTE Conductors on flex laminate in rigid section are covered by prepreg.

ECSS-Q-ST-70-12_1200267

b. The spacing of conductors on flex laminate in the flex section shall be in conformance with values for X,Y internal specified in the Table 13-4.

NOTE Conductors on flex laminate in flex section are covered by cover layer.

ECSS-Q-ST-70-12_1200268

c. The spacing of conductors on flex laminate in the flex section for soldering a flex termination shall be in conformance with values for X,Y external specified in the Table 13-3.

NOTE 1 Conductors in flex section for soldering a flex termination are not covered by cover layer.

NOTE 2 Insulation distance in Z direction does not apply for sculptured flex, since it contains only a single layer of copper.

ECSS-Q-ST-70-12_1200269

Table 13-4: Minimum insulation distance as function of voltage on as-manufactured PCB for flex laminate.

V	Z	X,Y internal	X,Y external
0-150 V	1 µm/V AND 25 µm	1,5 µm/V AND 150 µm	as specified in Table 13-3
Note: The legend to this table is provided in Table 13-1.			

13.8.4 Conformal coating

ECSS-Q-ST-70-12_1200475

a. Conductors on external layers should be covered with conformal coating.

ECSS-Q-ST-70-12_1200270

b. Fine pitch conductors on external layers shall be covered with conformal coating.

ECSS-Q-ST-70-12_1200271

c. Uncoated conductors on a PCB shall not be used for voltages > 30 V, except the case specified in the requirement 13.8.4d.

NOTE This is to avoid Paschen discharge when switched on during launch.

ECSS-Q-ST-70-12_1200476

d. Uncoated conductors may be used above 30 V for connector pads where coating or potting cannot penetrate locally between the connector pins.

ECSS-Q-ST-70-12_1200272

e. For the footprint of components and connectors that cannot be conformally coated, the insulation distance shall be in compliance with the requirements specified in Table 13-3 for X,Y external without conformal coating.

ECSS-Q-ST-70-12_1200273

f. The requirement 13.8.4e shall apply in case the conformal coating is used but cannot penetrate the footprint and cannot completely encapsulate the pads.

ECSS-Q-ST-70-12_1200274

g. Coating types that provide encapsulation of the PCB shall be included as conformal coating.

NOTE Higher voltage (> 30 V) PCBs designed without conformal coating are commonly encapsulated by other means, such as potting. Connectors can be potted or coated in similar way.

h. In case of overhang of Au or Ni/Au, the assembled PCB shall be conformal coated in conformance with requirement 10.6.3j of ECSS-Q-ST-70-60.

13.9 Double insulation design rules for critical tracks

13.9.1 Overview

The design of PCBs can have an impact on the reliability of a system. Any credible single failure into a PCB can lead to loss of a critical function of a system.

13.9.2 Critical nets

ECSS-Q-ST-70-12_1200275

a. Nets shall be identified as “critical” when they include the following functionalities:

1. non-protected sections of a main bus power distribution system up to and including the first protection device,
2. nets that are a single point failure SPF for the system,
3. nets on which a loss of insulation can result in electrical failure propagation to a critical net,
4. cross-strapped functions and associated common links from source to load.

NOTE 1 Details for requirement 13.9.2a.1 are specified in requirement 5.8.1.c. of the ECSS-E-ST-20.

NOTE 2 Example for the requirement 13.9.2a.3 is primary and redundant nets on a single PCB.

NOTE 3 Examples of cross-strapped functions from the requirement 13.9.2a.4 are hot redundant power links, majority voters "reliable" links, specific telecommand or telemetry matrices.

ECSS-Q-ST-70-12_1200276

b. Critical nets shall be subject to double insulation in conformance with requirements from the Clause 13.9.

ECSS-Q-ST-70-12_1200477

c. PA requirements of projects may specify requirements to implement double insulation on specific nets.

ECSS-Q-ST-70-12_1200277

d. FAI shall be performed in case double insulation applies.

13.9.3 Prevention of short circuit

13.9.3.1 Increase insulation in the PCB

ECSS-Q-ST-70-12_1200278

a. The insulation in Z direction between adjacent layers as specified in the requirement 13.8.2e and Table 13-3 shall be increased by one of the three methods:

   1. Method 1: Increase the insulation distance in Z direction by implementing the distance specified in Table 13-5 and Table 13-6.

   2. Method 2: Maintain insulation distance in Z direction as specified in Table 13-3 and Table 13-4 and use a combination of two different individually cured insulators as specified in the following options:

      (a) Prepreg with laminate and copper on one side only,

      (b) Prepreg with flex laminate and copper on one side only

   3. Method 3: Maintain insulation distance in Z direction as specified in Table 13-3 and Table 13-4 and have conductors on adjacent layers not superimposed and off-set by an insulation distance in X,Y direction as specified in requirement 13.9.3.1c.

ECSS-Q-ST-70-12_1200279

b. Method 3 of requirement 13.9.3.1a shall be used on microvia layers.

ECSS-Q-ST-70-12_1200280

c. The insulation distance in X,Y direction shall be increased in conformance with values specified in Table 13-5 and Table 13-6.

NOTE 1 Increasing insulation distance as specified in the requirement 13.9.3.1a.1 results in a lower field strength.

NOTE 2 Figure 13-2 and Figure 13-3 show examples of double insulation methods. The letters A, B, C, D, E, F, G, H, I, L indicate insulation distance.

NOTE 3 An example of insulation by prepreg and rigid laminate as specified in the requirement 13.9.3.1a.2(a) is shown in Figure 13-2 between copper tracks 2 and 5. The copper on the bottom side of the laminate (between track 4 and 6) has been etched away such that double insulation is achieved between track 2 and 5.

NOTE 4 An example of insulation of prepreg and flex laminate as specified in the requirement 13.9.3.1a.2(b) is shown in Figure 13-3 between copper tracks 2 and 5.

NOTE 5 An example of off-set conductors as specified in requirement 13.9.3.1a.3 is shown in Figure 13-2 between copper tracks 2 and 4.

NOTE 6 An example of insulation in X,Y direction as specified in the requirement 13.9.3.1c, is shown in Figure 13-2 between copper tracks 2 and 1.

NOTE 7 For insulation in Z direction as specified in requirement 13.9.3.1a, method number 3 is considered more reliable for electrical insulation than method 2 and method 1. Method 2 is again more reliable than method 1.

NOTE 8 For insulation in Z direction as specified in requirement 13.9.3.1a, method number 2 is subject to qualification of the PCB manufacturing processes as specified in the PID.

NOTE 9 Fine pitch tracks are not compliant with double insulation because of the increased distance specified in the Table 13-5.

ECSS-Q-ST-70-12_1200281

Table 13-5: Minimum double insulation distance as function of voltage on as-manufactured PCB for rigid laminate.

V	Z	X,Y external with conformal coating	X,Y external without conformal coating	X,Y internal conductor to conductor	X,Y internal conductor to hole wall	X,Y internal Hole wall to hole wall Hole wall to heat sink
0-10V	100 µm	240 µm	Not permitted	240 µm	290 µm	700 µm
11-30V						
31-500	1,5 µm/V AND 130 µm	4 µm/V AND 320 µm		2 µm/V AND 300 µm	(2 µm/V+50) AND 350 µm	4 µm/V AND 700 µm
Note: The legend to this table is provided in Table 13-1.						

ECSS-Q-ST-70-12_1200282

Table 13-6: Minimum double insulation distance as function of voltage on as-manufactured PCB for flex laminate.

V	Z	X,Y internal	X,Y external
0-150 V	2 µm/V AND 50 µm	3 µm/V AND 300 µm	as specified in Table 13-5
Note: The legend to this table is provided in Table 13-1.			

13.9.3.2 Increase insulation of PCB assembly

ECSS-Q-ST-70-12_1200283

a. Conformal coating shall be applied on external conductors in case of double insulation.

ECSS-Q-ST-70-12_1200284

b. The insulation of conductive elements on external layers for a PCB assembly for which double insulation applies, shall be increased as follows:

1. The insulation distance of the surface pattern to adjacent surroundings is ≥ 2x the distance as specified in Table 14-1 up to a distance of 1 mm.
2. The insulation distance of components to adjacent surroundings equals the recommended data as specified in Table 14-2.
3. The insulation distance to component pads is ≥ 2x the distance specified in Table 14-3.

NOTE This is done to mitigate the risk of loss of insulation due to foreign particles, voids, or cracks in laminate or prepreg.

ECSS-Q-ST-70-12_1200285

c. The insulation distance from a conductor to the PCB edge in conformance with the requirement 13.8.2h shall be doubled in case the PCB edge faces an external conductive element within a distance of less than 1 mm.

ECSS-Q-ST-70-12_1200286

d. Flexible PCB sections that include critical tracks and that face other conductive elements with an insulation distance of < 1 mm shall include an additional insulation layer of ≥ 25 µm on the conductive element.

NOTE Additional insulation can be provided by 25 µm Kapton tape.

ECSS-Q-ST-70-12_1200287

e. Overhang of chip components shall not reduce the insulation distance below the values specified in the requirement 13.9.3.2b.3.

13.9.3.3 Routing

ECSS-Q-ST-70-12_1200478

a. Critical tracks as specified in the requirement 13.9.2a should not be routed on external layers.

NOTE This is also recommended for non-critical track in conformance with requirements from the clause 7.4.3a.

ECSS-Q-ST-70-12_1200288

b. In case critical tracks are routed on external layers, they shall not be routed under components.

NOTE This is done to allow inspection of critical tracks.

ECSS-Q-ST-70-12_1200289

c. A critical net shall be covered with conformal coating including the track, pads and component leads.

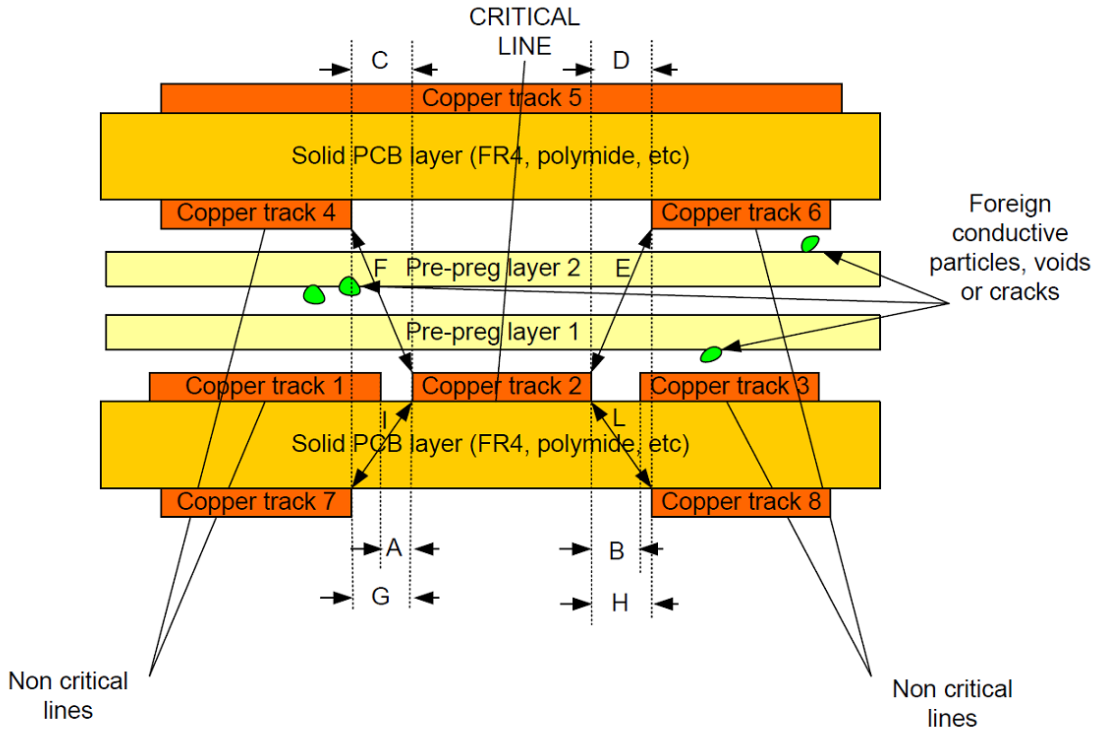


Figure 13-2: Example of double insulation by increasing distance in X,Y and by not superimposing copper on adjacent layers

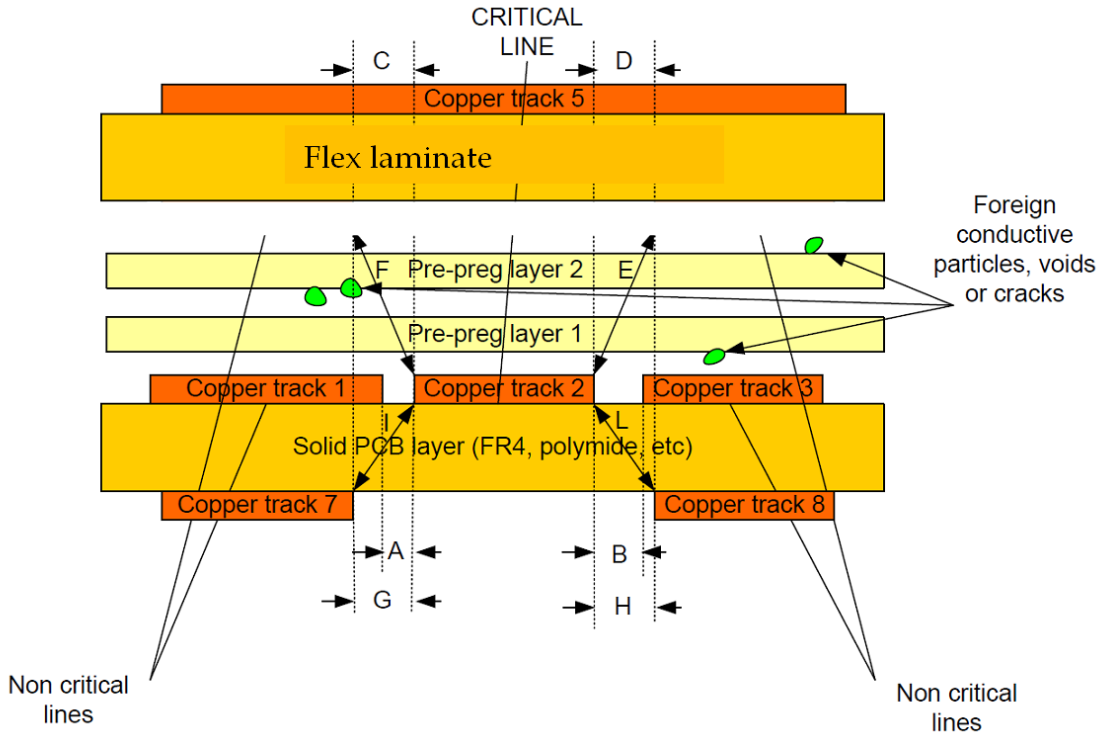


Figure 13-3: Example of double insulation by increasing distances in X,Y and by using two insulators in Z direction.

13.10 Insulation distance of combined requirements on rigid PCB

ECSS-Q-ST-70-12_1200290

a. As-manufactured insulation distance shall be in conformance with the values specified in Table 13-7 and Table 13-8.

ECSS-Q-ST-70-12_1200479

b. As-designed insulation distance should be in conformance with the values specified in Table 13-7 and Table 13-8.

ECSS-Q-ST-70-12_1200480

c. As-designed insulation distance may be less than the values specified in the Table 13-7 and Table 13-8 in case the following conditions are met:

1. a dedicated inspection is performed to verify that the as-manufactured insulation distance is in compliance with the values from the Table 13-7 and Table 13-8, and
2. the insulation distance is recorded as a Review Item in the PCB definition dossier.

NOTE 1 See the overview specified in clause 13.8.1 for a list of parameters that affect the insulation

distance and that are included in the Table 13-7 and Table 13-8.

NOTE 2 For legend to Table 13-7 and Table 13-8 see the overview in clause 13.1.

d. The single or sequential 'bond sequence' specified in the Table 13-7 for 'X,Y internal hole wall to hole wall' shall be determined at the time of drilling.

Table 13-7: Minimum insulation distances on rigid PCB as function of all combined requirements (*part 1 of 4*)

		Z laminate				Z prepreg	
	Insulation →	**standard**		**Double 13.9**		**standard**	**Double 13.9**
V (peak 13.8.2b)	Cu Th →	≤ 35 µm	70 µm	≤ 35 µm	70 µm	-	-
0<V≤10	As manufactured	70 µm		100 µm		70 µm FOR µvia layer 11.4.1h: 60 µm	100 µm FOR µvia layer offset 13.9.3.1b: 60 µm
	As-designed	≥ 4mil 7.1.3f	≥ 5mil 7.1.3g	5mil screened 7.1.3g OR 5mil class D 7.1.3j OR 6mil		-	-
10<V≤30	As-manufactured	70 µm		100 µm		70 µm FOR µvia layer 11.4.1h: 60 µm	100 µm FOR µvia layer offset 13.9.3.1b: 60 µm
	As-designed	≥ 4mil 7.1.3f	≥ 5mil 7.1.3g	5mil screened 7.1.3g OR 5mil class D 7.1.3j OR 6mil		-	-
30<V≤50	As-manufactured	100 µm		130 µm OR 100 µm with two insulators 13.9.3.1a.2.		100 µm FOR µvia layer offset 11.4.1j: 60 µm	130 µm OR 100 µm with two insulators 13.9.3.1a.2 FOR µvia layer offset 13.9.3.1b: 60 µm
	As-designed	5mil screened 7.1.3g OR 5mil class D 7.1.3j OR 6mil		See Table 7-2		-	-
50<V≤100	As-manufactured	100 µm		(1,5 µm/V AND 130 µm) OR 100 µm with two insulators 13.9.3.1a.2.		100 µm FOR µvia layer offset 11.4.1j: 60 µm	(1,5 µm/V AND 130 µm) OR 100 µm with two insulators 13.9.3.1a.2 FOR µvia layer offset 13.9.3.1b: 60 µm
	As-designed	5mil screened 7.1.3g OR 5mil class D 7.1.3j OR 6mil		See Table 7-2		-	-
100<V≤500	As-manufactured	1 µm/V		1,5 µm/V OR 1 µm/V with two insulators 13.9.3.1a.2.		1 µm/V FOR µvia layer offset 11.4.1j: 60 µm	1,5 µm/V OR 1 µm/V with two insulators 13.9.3.1a.2 FOR µvia layer offset 13.9.3.1b: 60 µm
	As-designed	See Table 7-2		See Table 7-2		-	-

Table 13-7: Minimum insulation distances on rigid PCB as function of all combined requirements (*continued 2 of 4*)

Insulation →		X,Y external without conformal coating				X,Y external with conformal coating					
		standard			Double 13.9	standard			Double 13.9		
max tolerance in X,Y 7.4.2b →		50 µm	50 µm	70 µm		50 µm	50 µm	70 µm	50 µm	50 µm	70 µm
V (peak 13.8.2b)	Cu Th →	fine pitch Th ≤ 70 µm	normal pitch Th ≤ 70 µm	normal pitch Th > 70 µm		fine pitch Th ≤ 70 µm	normal pitch Th ≤ 70 µm	normal pitch Th > 70 µm	fine pitch Th ≤ 70 µm	normal pitch Th ≤ 70 µm	normal pitch Th > 70 µm
0<V≤10	As-manufactured	not permitted	200 µm	280 µm	not permitted	120 µm	160 µm	240 µm	not permitted	320 µm	480 µm
	As-designed		250 µm	350 µm		150 µm	200 µm	300 µm		370 µm	550 µm
10<V≤30	As-manufactured		300 µm	380 µm		120 µm	160 µm	240 µm		320 µm	480 µm
	As-designed		350 µm	450 µm		150 µm	200 µm	300 µm		370 µm	550 µm
30<V≤50	As-manufactured		not permitted, except FOR connector pads 13.8.4d: 500 µm			not permitted	160 µm	240 µm		320 µm	480 µm
	As-designed		FOR 13.8.4d: 550 µm	FOR 13.8.4d: 570 µm			200 µm	300 µm		370 µm	550 µm
50<V≤100	As-manufactured	7.4.3g.3	not permitted, except FOR connector pads 13.8.4d: 500 µm		13.9.3.2a		2 µm/V AND 160 µm	240 µm	13.9.3.1c and its NOTE 9	4 µm/V AND 320 µm	480 µm
	As-designed		FOR 13.8.4d: 550 µm	FOR 13.8.4d: 570 µm		7.4.3g.4	2,5 µm/V AND 200 µm	300 µm		(4 µm/V + 50 µm) AND 370 µm	550 µm
100<V≤500	As-manufactured		not permitted, except FOR connector pads 13.8.4d: 5 µm/V				2 µm/V	2 µm/V AND 240 µm		4 µm/V	4 µm/V AND 480 µm
	As-designed		FOR 13.8.4d: (5 µm/V +50µm)	FOR 13.8.4d: (5 µm/V +70µm)			(2 µm/V +50µm)	(2 µm/V + 70µm) AND 300 µm		(4 µm/V +50µm)	(4 µm/V +70µm) AND 550 µm

Table 13-7: Minimum insulation distances on rigid PCB as function of all combined requirements (*continued 3 of 4*)

Insulation →		X,Y internal conductor to conductor									
		standard					Double 13.9				
max tolerance in X,Y 7.4.2b →		30 µm	30 µm	50 µm	50 µm	70 µm	30 µm	30 µm	50 µm	50 µm	70 µm
V (peak 13.8.2b)	Cu Th →	fine pitch Th ≤ 17 µm	normal pitch Th ≤ 17 µm	17<Th≤60 µm	60<Th≤70 µm	70<Th≤95 µm	fine pitch Th ≤ 17 µm	normal pitch Th ≤ 17 µm	17<Th≤60 µm	60<Th≤70 µm	70<Th≤95 µm
0<V≤10	As-manufactured	FOR fine pitch 7.4.5a: 96 µm FOR 1mm pitch HDI 11.5.5a and 11.6a: 63 µm	104 µm	120 µm	160 µm	240 µm	not permitted 13.9.3.1c and its NOTE 9	240 µm	240 µm	280 µm	360 µm
	As-designed	FOR fine pitch 7.4.5a: 120 µm FOR 1mm pitch HDI 11.5.5a and 11.6a: 70 µm	130 µm	150 µm	200 µm	300 µm		270 µm	290 µm	330 µm	430 µm
10<V≤30	As-manufactured	FOR fine pitch 7.4.5a: 96 µm	104 µm	120 µm	160 µm	240 µm		240 µm	240 µm	280 µm	360 µm
	As-designed	FOR fine pitch 7.4.5a: 120 µm	130 µm	150 µm	200 µm	300 µm		270 µm	290 µm	330 µm	430 µm
30<V≤50	As-manufactured	not permitted 7.4.5d	150 µm	150 µm	160 µm	240 µm		300 µm	300 µm	310 µm	390 µm
	As-designed		180 µm	188 µm	200 µm	300 µm		330 µm	350 µm	360 µm	460 µm
50<V≤100	As-manufactured		150 µm	150 µm	160 µm	240 µm		300 µm	300 µm	310 µm	390 µm
	As-designed		180 µm	188 µm	200 µm	300 µm		330 µm	350 µm	360 µm	460 µm
100<V≤500	As-manufactured		1 µm/V AND 150 µm	1 µm/V AND 150 µm	1 µm/V AND 160 µm	1 µm/V AND 240 µm		2 µm/V AND 300 µm	2 µm/V AND 300 µm	2 µm/V AND 310 µm	2 µm/V AND 390 µm
	As-designed		(1 µm/V +30µm) AND 180 µm	(1 µm/V +50µm) AND 188 µm	(1 µm/V +50µm) AND 200 µm	(1 µm/V +70µm) AND 290 µm		(2 µm/V +30µm) AND 330 µm	(2 µm/V +50µm) AND 350 µm	(2 µm/V +50µm) AND 360 µm	(2 µm/V +70µm) AND 460 µm

Table 13-7: Minimum insulation distances on rigid PCB as function of all combined requirements (*continued 4 of 4*)

		X,Y internal conductor to hole wall		X,Y internal hole wall to hole wall			
Insulation →		standard	Double 13.9	standard		Double 13.9	
max tolerance in X,Y 13.8.2iNOTE →		-	-	100 µm	300 µm	100 µm	300 µm
V (peak 13.8.2b)	bond sequence →	-	-	single bond sequence	sequential bonding and rigid flex	single bond sequence	sequential bonding and rigid flex
0<V≤10	As-manufactured	FOR reduced pad diameter 7.5.3l, fine pitch 7.4.5a, 1 mm pitch HDI 11.5.5a and 11.6a: X,Y internal + annular ring of 25 µm		350 µm	350 µm	700 µm	700 µm
	As-designed			450 µm	650 µm	800 µm	1000 µm
10<V≤30	As-manufactured			350 µm	350 µm	700 µm	700 µm
	As-designed			450 µm	650 µm	800 µm	1000 µm
30<V≤50	As-manufactured	X,Y internal + annular ring of 50 µm 13.8.2g and its NOTE		350 µm	350 µm	700 µm	700 µm
	As-designed			450 µm	650 µm	800 µm	1000 µm
50<V≤100	As-manufactured			350 µm	350 µm	700 µm	700 µm
	As-designed			450 µm	650 µm	800 µm	1000 µm
100<V≤500	As-manufactured			2 µm/V AND 350 µm	2 µm/V AND 350 µm	4 µm/V AND 700 µm	4 µm/V AND 700 µm
	As-designed			(2 µm/V + 100 µm) AND 450 µm	(2 µm/V + 300 µm) AND 650 µm	(4 µm/V + 100 µm) AND 800 µm	(4 µm/V + 300 µm) AND 1000 µm

Note: The legend to this table is provided in Table 13-1.

Table 13-8: Minimum insulation distances on flex PCB, as well as flex section of rigid-flex PCB, as function of all combined requirements

- Insulation →		X,Y internal				X,Y external without conformal coating				Z	
		standard		Double 13.9		standard			Double 13.9	standard	Double
max tolerance in X,Y 7.4.2b →		30 µm	50 µm	**30 µm**	50 µm	50 µm	50 µm	70 µm		-	-
V (peak 13.8.2b)	Cu Th →	normal pitch Th ≤ 17 µm	normal pitch 17 < Th ≤ 60 60 < Th ≤ 70	normal pitch **Th ≤ 17 µm**	normal pitch 17 < Th ≤ 60 60 < Th ≤ 70	fine pitch Th ≤ 70 µm	normal pitch Th ≤ 70 µm	normal pitch Th > 70 µm		-	-
0<V≤100	As-manufactured	150 µm	160 µm	300 µm		not permitted 7.4.3g.3	0<V≤10: 200 µm 10<V≤30: 300 µm 30<V≤100: 500 µm	0<V≤10: 280 µm 10<V≤30: 380 µm 30<V≤100: 500 µm	not permitted 13.9.3.2a	1 µm/V AND 25µm	2 µm/V AND 50µm
	As-designed	180 µm	200 µm	330 µm	350 µm		0<V≤10: 250 µm 10<V≤30: 350 µm 30<V≤100: 550 µm	0<V≤10: 350 µm 10<V≤30: 450 µm 30<V≤100: 570 µm		Nearly the same as above due to very small tolerance	
100<V≤150	As-manufactured	1,5 µm/V	1,5 µm/V AND ≥160 µm	3 µm/V	3 µm/V		5 µm/V	5 µm/V		1 µm/V	2 µm/V
	As-designed	1,5 µm/V + 30 µm	1,5 µm/V + 50 µm	3 µm/V + 30 µm	3 µm/V + 50 µm		5 µm/V + 50µm	5 µm/V + 70µm		Nearly the same as above due to very small tolerance	

13.11 Controlled impedance tracks

13.11.1 Definitions specific to controlled impedance

Microstrip is a track coupled to one copper plane. Stripline is a track between two copper planes. Stripline provides better shielding of the signals compared to microstrip, but it requires more plane layers.

Differential microstrip are two parallel tracks on the same layer and coupled to one copper plane. Differential striplines are two parallel tracks either edge coupled or broadside coupled and coupled to two copper planes.

For end to end configuration only a single driver and receiver is present at the extremes of a track. For multidrop configuration multiple drivers and receivers are possible along a track.

13.11.2 General rules

ECSS-Q-ST-70-12_1200292

a. Controlled impedance tracks shall be recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12_1200481

b. Controlled impedance tracks should be routed on a single layer.

ECSS-Q-ST-70-12_1200482

c. Vias should not be used in controlled impedance tracks except for the connection of component pads.

ECSS-Q-ST-70-12_1200483

d. The controlled impedance tracks should be designed with end-to-end configuration.

ECSS-Q-ST-70-12_1200484

e. The controlled impedance tracks may be designed with multidrop configuration.

ECSS-Q-ST-70-12_1200293

f. When using multidrop configuration the impedance calculation shall include the additional discrete loads.

13.11.3 Microstrip and stripline

ECSS-Q-ST-70-12_1200294

a. Microstrip or stripline shall be used for single ended controlled impedance tracks.

ECSS-Q-ST-70-12_1200295

b. Differential microstrip and differential stripline shall be used for differential controlled impedance tracks.

NOTE An example of edge coupled differential striplines is given in Figure 13-4. This figure shows the following characteristic dimensions used to calculate impedance:

- H: distance between planes as-manufactured
- H1: laminate thickness between tracks and plane.
- W: width of the top of the tracks
- W1: width of the foot of the tracks
- S: spacing between foot of tracks.

ECSS-Q-ST-70-12_1200296

c. Differential tracks shall be routed in parallel without change of the distance between the tracks except the case specified in the requirement 13.11.3d.

ECSS-Q-ST-70-12_1200485

d. Differential tracks may be routed non-parallel at the end of the track.

NOTE This is permitted to route to pads.

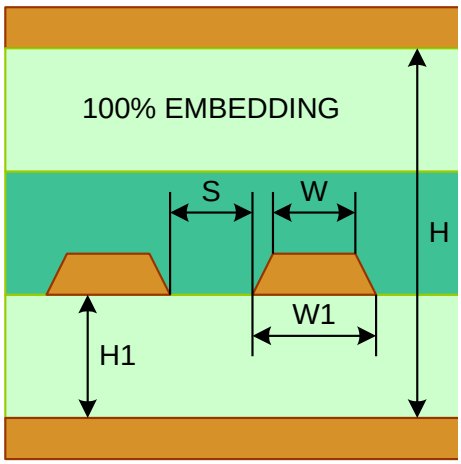


Figure 13-4: Edge coupled differential striplines

13.11.4 Line impedance termination for end-to-end configuration

ECSS-Q-ST-70-12_1200297

a. Series termination shall be used for end-to-end configuration.

ECSS-Q-ST-70-12_1200298

b. The resistor for series termination shall be placed at the driver output.

ECSS-Q-ST-70-12_1200486

c. AC parallel termination may be used in the end-to-end configuration at the input of the receiver.

13.11.5 Line impedance termination for multidrop configuration

ECSS-Q-ST-70-12_1200299

a. Parallel termination shall be used in multidrop configuration.

ECSS-Q-ST-70-12_1200487

b. DC or AC termination may be used in a multidrop configuration.

NOTE AC termination can be preferred to save power.

ECSS-Q-ST-70-12_1200300

c. In multidrop configuration with one driver and several receivers the driver shall be at one end of the line and the termination at the other end.

ECSS-Q-ST-70-12_1200301

d. In multidrop configuration with several drivers and several receivers the line termination shall be at both ends of the line.

13.12 Digital PCB

13.12.1 Overview

Digital circuitries are those in which the information on a line can assume only two values “0” or “1”. They are, in general, more robust to noise with respect to the analog ones. They can be critical during the transition of the threshold region if the input signal is not monotonic.

The criticality of digital signals is indicated as non-critical, critical and highly critical. The criteria for criticality are not the same as for critical nets subject to double insulation as specified in the clause 13.9.2.

13.12.2 Zone management and routing

ECSS-Q-ST-70-12_1200488

a. The layout of a PCB should be partitioned by using zone management where different logical blocks are physically separated from each other.

NOTE Different blocks to be separated in a board layout can be low speed (or static) links, analog links, power lines, high speed serial digital links, RF signals.

ECSS-Q-ST-70-12_1200489

b. The low speed circuit should be separated from the high speed digital circuit.

ECSS-Q-ST-70-12_1200490

c. High speed signals should not be routed through low speed zones.

NOTE This is done to prevent cross talk.

ECSS-Q-ST-70-12_1200302

d. Ground planes shall be used in high speed digital applications.

ECSS-Q-ST-70-12_1200491

e. Ground planes should be used in all digital applications.

ECSS-Q-ST-70-12_1200303

f. High speed signals shall be routed over uninterrupted planes

NOTE Examples of uninterrupted planes are Vcc or GND.

ECSS-Q-ST-70-12_1200492

g. The loop area of high speed signals should be minimised.

NOTE Loop area is minimised to reduce current noise. This can be achieved by routing the forwarded signal directly below or above a ground plane as return path. Further precautions can be found in the following references: chapter B.3.3 and B.3.4 of IPC-2251; chapter 6.4.6 of IPC-2221B.

ECSS-Q-ST-70-12_1200493

h. Circuitry and components for high speed signals should be kept close together.

ECSS-Q-ST-70-12_1200494

i. The length of routing in digital applications for high speed signals should be minimised, except when matched timing is used.

NOTE Reducing the length of signal paths is done, especially for high speed parallel links between components, to reduce crosstalk, voltage noise and adaptation of line impedance. This also achieves a more compact PCB design. The technology determines how to implement minimisation. For example, rise and fall time are more critical than frequency. Tracks length lower than "critical length" defined in Table 5-4 of IPC-2251 is an example of minimisation. When "critical length" is exceeded, the tracks are considered as transmission lines. This is described in chapter 4.4.2.d of IPC-2251 and in IPC-2141A.

13.12.3 Criticality of digital signals

13.12.3.1 Non-critical signals

ECSS-Q-ST-70-12_1200304

a. Signals that are not sensitive to the coupling between them shall be identified as "non-critical".

NOTE Examples of non-critical signals are: data bus, address bus.

ECSS-Q-ST-70-12_1200495

b. Non-critical signals specified in the requirement 13.12.3.1a may be routed together in bundles disregarding transients between them.

NOTE 1 Transients are temporary anomalies in the electrical signal, such as overshoot, undershoot, ringing, lines reflection, crosstalk.

NOTE 2 Transients are typically expired or reduced to an acceptable level before the sampling time.

ECSS-Q-ST-70-12_1200496

c. Direct coupling between bundles of non-critical signals specified in the requirement 13.12.3.1a should be avoided.

13.12.3.2 Critical signals

ECSS-Q-ST-70-12_1200305

a. Signals that require a monotonic waveform through the voltage threshold of the receivers shall be identified as "critical".

NOTE Examples of critical signals are: clocks signals, write signals.

ECSS-Q-ST-70-12_1200497

b. The routing of critical signals specified in the requirement 13.12.3.2a should maintain signal integrity at the receiver end.

NOTE Signal integrity tools can be used to simulate the behaviour of the PCB after routing.

ECSS-Q-ST-70-12_1200306

c. The integrity of critical signals specified in the requirement 13.12.3.2a shall be verified by electrical testing of the PCB.

13.12.3.3 Highly critical signals

ECSS-Q-ST-70-12_1200307

a. Signals that can affect the performance of the circuit as a result of noise, crosstalk, jitter, ringing or propagation delay, shall be identified as “highly critical”.

NOTE Examples of highly critical signals are: PLL signals, low voltage and high frequency LVDS signals.

ECSS-Q-ST-70-12_1200498

b. Highly critical signals specified in the requirement 13.12.3.3a should be routed without adjacent signals or protected by shielding.

NOTE Separation of other highly critical signals is done to prevent crosstalk and noise pickup. Separation can be achieved by planes and rows of shielding vias.

ECSS-Q-ST-70-12_1200308

c. The integrity of highly critical signals specified in the requirement 13.12.3.3a shall be verified by electrical testing of the PCB.

13.13 Analog PCB

13.13.1 Overview

PCB for analog circuitries are used to interconnect heterogeneous discrete components such as resistors, capacitors, diodes, transistors, amplifiers to implement an analog function. Analog circuitries are more susceptible to noise compared to digital circuitries. The PCB design can affect the overall performance. Analog signals include all values within a range. The criticality depends on the resolution or on the bandwidth of the signal.

The criticality of analog signals is indicated as non-critical, critical and highly critical. The criteria for criticality are not the same as for critical nets subject to double insulation as specified in the clause 13.9.2.

13.13.2 Criticality of analog signals

13.13.2.1 Non-critical signals

ECSS-Q-ST-70-12_1200309

a. Signals that have low speed, low bandwidth or low resolution shall be identified as “non-critical”.

NOTE The signal-to-noise ratio, pickup and crosstalk noise (or any combination) are non-critical for such signals. These signals do not affect the performance or the functionality of the equipment.

13.13.2.2 Critical signals

ECSS-Q-ST-70-12_1200310

a. Signals for which signal-to-noise ratio, pickup or crosstalk noise can affect performance of a circuit shall be identified as “critical”.

NOTE Examples of critical signals are: feedback signals of control loop of series and switching regulators.

13.13.2.3 Highly critical signals

ECSS-Q-ST-70-12_1200311

a. Signals with high speed or high bandwidth or low amplitude or high resolution shall be identified as “highly critical”.

NOTE The performance degradation of such signals can affect the functionality of the equipment.

NOTE The parasitic inductance of a track and the parasitic capacitance of a pad can affect high speed analog circuit performance.

ECSS-Q-ST-70-12_1200499

b. The length of a track connecting an inverted input of a high speed amplifier with a passive component should be minimised.

NOTE This reduces the noise coupling to high impedance input of the amplifier. The objective is to guarantee the noise performance of the amplifier.

ECSS-Q-ST-70-12_1200312

c. Highly critical circuitry specified in the requirement 13.13.2.3a shall have priority in the design, placement and routing.

13.13.3 Routing and shielding

ECSS-Q-ST-70-12_1200313

a. Ground planes shall be used for critical and highly critical analog circuitries specified in the requirements 13.13.2.2a and13.13.2.3a.

ECSS-Q-ST-70-12_1200500

b. Ground planes should be used for non-critical analog circuitries specified in the requirement 13.13.2.1a.

NOTE Ground planes shield signals from pickup noise.

ECSS-Q-ST-70-12_1200501

c. The track length of high impedance signals should be minimized.

NOTE This is done to reduce crosstalk and pickup noise.

ECSS-Q-ST-70-12_1200502

d. High impedance signals should be shielded or have guard rings implemented.

ECSS-Q-ST-70-12_1200503

e. “Set on test” components should be placed near to the adjusted component.

ECSS-Q-ST-70-12_1200504

f. Test point and jumpers for analog circuitry should be placed near to the circuit that requires adjustment.

NOTE Examples of circuit that can require adjustment are: series regulator, voltage reference, DC/DC converters.

13.14 Mixed analog-digital PCB

ECSS-Q-ST-70-12_1200314

a. Analog and digital circuitry on the same PCB shall be separated from each other by zone management and shielding.

ECSS-Q-ST-70-12_1200505

b. Planes of analog and digital circuitries should be separated.

NOTE Superimposed analog and digital planes can result in AC coupling and digital noise on the analog signal.

ECSS-Q-ST-70-12_1200506

c. Planes of analog and digital circuitries may be combined in case separation of the planes has an adverse effect on performance or functionality or EMC.

ECSS-Q-ST-70-12_1200315

d. In case planes of analog and digital circuitries are combined, power supply decoupling shall be implemented.

ECSS-Q-ST-70-12_1200507

e. Digital signals should not be routed through analog zones.

NOTE The accurate routing of the analog and digital signals is important for DAC, ADC and MUX applications.

14
Design for assembly

14.1 Overview

The requirements in this clause apply to the design of the PCB for PCB assembly by internal or external assembly house. The surface pattern of the PCB depends on the PCB geometry, the assembly method and the location of mechanical and external elements.

14.2 General

ECSS-Q-ST-70-12_1200316

a. When PCB design and PCB assembly are performed in different companies, the supplier shall confirm with the assembly house which assembly processes are used.

ECSS-Q-ST-70-12_1200317

b. Pad geometry and outer layers shall be reviewed and approved by the assembly house for potential assembly problems in compliance with requirements from ECSS-Q-ST-70-61.

NOTE An example of assembly problems referred to in this requirement is a stay out zone to enable access with solder iron without touching the component to be soldered as well as adjacent components. Another example is a stay out zone to enable reflow for repair of an AAD with a hot air soldering station without affecting adjacent components.

ECSS-Q-ST-70-12_1200318

c. <<deleted>>

ECSS-Q-ST-70-12_1200319

d. Assemblies using SnPb solder alloys on gold plated pads shall be in conformance with clause 6.9.2 of ECSS-Q-ST-70-61.

e. In case coverage with SnPb on the side of small SMT pads is needed, it shall be specified as a review item in the PCB definition dossier.

NOTE Exposed copper due to lack of SnPb coverage on the sides of conductors is permitted as specified in ref C of Table 10-40 of ECSS-Q-ST-70-60. It can be important to have SnPb coverage on the edges of

pads of fine pitch AAD footprint to achieve compliant assembly. In case SnPb is missing, it is a possibility to repair as specified in 6.10.2g of ECSS-Q-ST-70-60. For the smallest pitch AAD it is probable that there is a systematic lack of SnPb on the edges, which cannot be repaired within the limitations of the clause 6.10.2 of ECSS-Q-ST-70-60. In this case, another surface finish can be good practice.

f. The PCB shall be delivered with a support frame in case this is specified in the PCB definition dossier.

NOTE This is also specified for rigid-flex technology in conformance with requirement 9.3g.

g. The method of depanneling a PCB from its support frame shall be included in the PCB definition dossier.

h. Additional insulation distance should be designed by implementing a clearance zone around depanneling areas.

NOTE Depanneling methods include e.g. depanneling pips, break tabs and v-scoring. Depanneling processes are in conformance with clause 5.5.15 of ECSS-Q-ST-70-61. It is good practice to use a machine cutting process and to verify absence of defects on the PCB edge, such as haloing, crazing and delamination. In addition, it is good practice to implement a clearance zone, where possible, to mitigate impact on nearby components. Break tabs typically include mouse bites. The term 'break tabs' can suggest that the PCB is separated by breaking away its frame, which is not good practice as it leads to defects. Instead, it is good practice to handle break tabs in the same manner as depanneling pips using machine cutting.

14.3 Placement requirements

14.3.1 Conductive patterns

ECSS-Q-ST-70-12_1200320

a. The distance of the surface pattern to the adjacent surroundings shall be in conformance with values specified in Table 14-1.

NOTE An illustration is given in Figure 14-1.

ECSS-Q-ST-70-12_1200321

Table 14-1: Minimum distance as-manufactured of the surface pattern to the adjacent surroundings

Dimension	Description	Permitted	Recommended
A 1	Dimension between track and PCB edge	0,7 mm	
A 2	Dimension between track and mechanical part	1,0 mm	2,0 mm
A 3	Dimension between track and non-plated through hole	0,4 mm	
A 4	Dimension between via pad and hole for mechanical function	1,0 mm	
A 5	Dimension between track and screw	0,5 mm	
A 6	Dimension between conductive surface pattern and PCB edge	0,25 mm	
A 7	Dimension between edge of screw hole and PCB edge	1,0 mm	1,5 mm

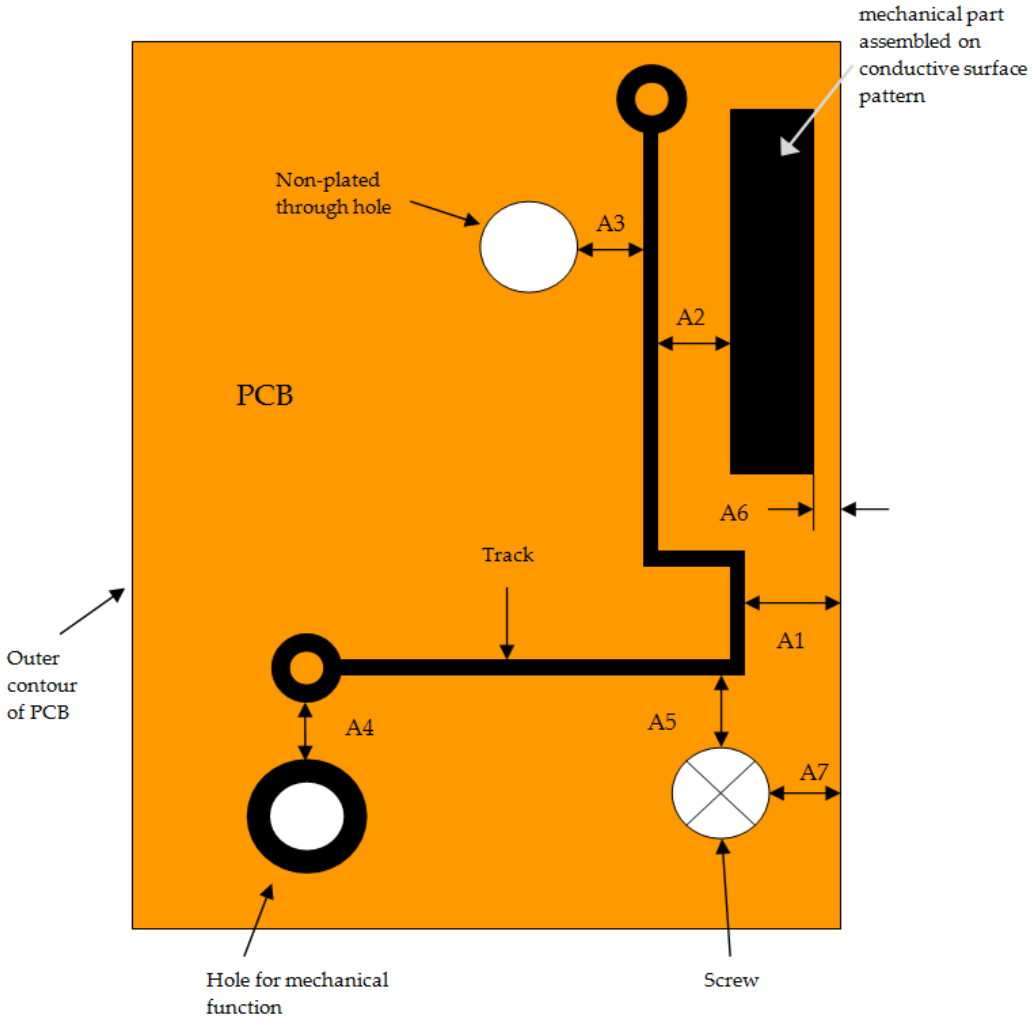


Figure 14-1: Illustration of surface pattern to adjacent surroundings

14.3.2 Components

ECSS-Q-ST-70-12_1200322

a. The conductive parts of components shall not be in contact with each other or with any metal in their adjacent surroundings.

NOTE For example screws, rack, and structure.

ECSS-Q-ST-70-12_1200323

b. The distance of components to adjacent surroundings shall be in conformance with values specified in Table 14-2.

NOTE An illustration is given in Figure 14-2.

ECSS-Q-ST-70-12_1200508

c. The width of the zone without components along the PCB edges should be ≥ 5 mm.

NOTE This is done to provide a clearance for the conveyor in the assembly equipment.

ECSS-Q-ST-70-12_1200324

d. In case the lay-out of the PCB requires the restricted zone to be less than 5 mm from the edge of the PCB, the PCB assembly house shall be consulted.

ECSS-Q-ST-70-12_1200325

Table 14-2: Minimum distance as-manufactured of components to adjacent surroundings

Minimum dimension	Description	Permitted data	Recommended data
B 1	Distance between component body to component body, one of which is non-conductive	> 0 mm, in case that precautions are taken to prevent damage during vibration.	0,6 mm
B 2	Distance between component lead and cover (of electronic box)	1,0 mm	1,0 mm
B 3	Component lead to component lead (B3-a) Component lead to component body (B3-b) Component lead to adjacent surroundings (B3-c) Component body to adjacent surroundings (B3-d) Distance between component body to component body, both of which are conductive (B3-e)	0,5 mm	1,0 mm

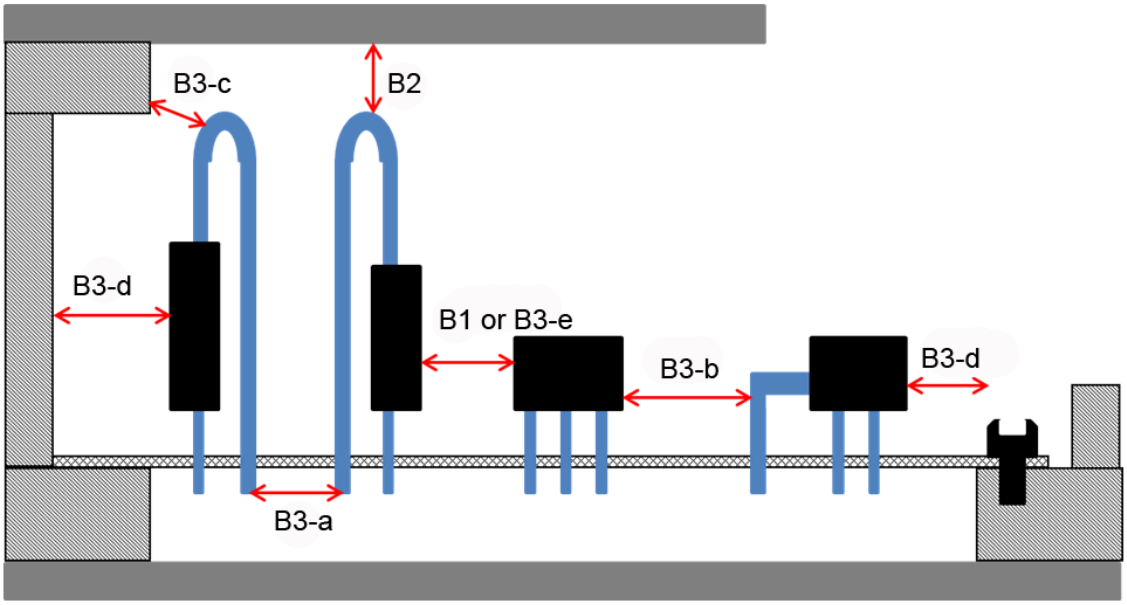


Figure 14-2: Illustration of component placing on PCB w.r.t. adjacent surrounding

14.3.3 Component pads

ECSS-Q-ST-70-12_1200326

a. Design for assembly on component pads shall be in conformance with requirements from the clause 8 and 10 of ECSS-Q-ST-70-61.

ECSS-Q-ST-70-12_1200327

b. The distance of component pads to adjacent surroundings shall be in conformance with values specified in Table 14-3.

NOTE An illustration is given in Figure 14-3

ECSS-Q-ST-70-12_1200328

c. The location of the devices shall be such that each solder connection can be visually inspected.

ECSS-Q-ST-70-12_1200509

d. High components should not be placed close together.

NOTE This is done to enable repair by manual soldering.

ECSS-Q-ST-70-12_1200510

e. Around an AAD a clearance should be implemented for repair.

NOTE Requirements for PCB repair are specified in ECSS-Q-ST-70-28.

ECSS-Q-ST-70-12_1200511

f. For PCBs submitted to conveyor wave soldering, components and tracks should be oriented in the solder direction.

ECSS-Q-ST-70-12_1200329

g. Designed test points shall be separated from the component solder pads.

ECSS-Q-ST-70-12_1200512

h. Test points may be incorporated in the solder pad by extending the pad dimensions so that test probing takes place outside the critical solder joint area in conformance with requirements 12.3.a.21 of the ECSS-Q-ST-70-61.

ECSS-Q-ST-70-12_1200330

i. The extended pad shall be included in the assembly qualification as the extra size affects the volume of solder in the joint.

ECSS-Q-ST-70-12_1200331

j. Thermal relief shall be designed between component PTH and copper planes.

ECSS-Q-ST-70-12_1200332

Table 14-3: Minimum distance as-manufactured to component pads

Minimum dimension	Description	Permitted data
A, B, C, G, J	- Dimension between pads of PTH on solder side - Pads of non-leaded SMT devices	0,3 mm
D, E, H, I	- Dimension between pads of PTH on component side - Pads of leaded SMT devices	0,5 mm
F	Dimension between component body to pad	0,5 mm

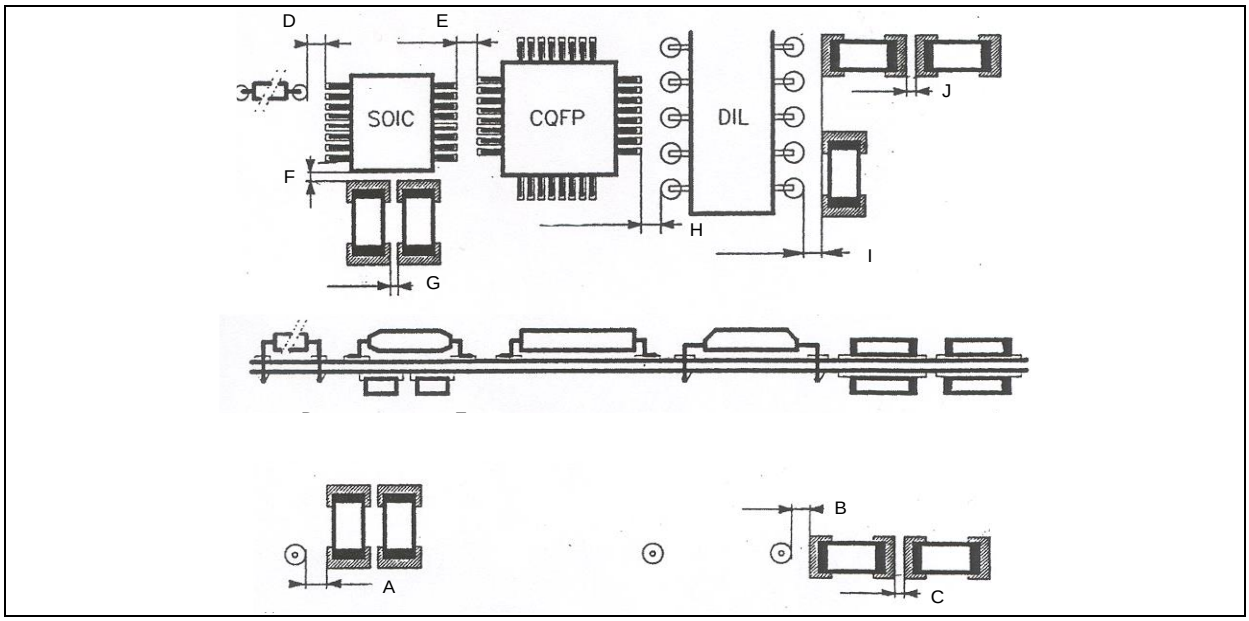


Figure 14-3: Illustration of pad placing on PCB with respect to adjacent surroundings

14.3.4 Fan out of SMT pads

ECSS-Q-ST-70-12_1200333

a. The track length between SMT pad and via shall be in conformance with values specified in Table 14-4

NOTE 1 In Figure 14-4: L_T is the track length between SMT and via.

NOTE 2 The through going via can absorb all tin-lead away from the pad during assembly.

ECSS-Q-ST-70-12_1200334

b. For other track dimensions, the supplier shall extrapolate or interpolate from the values specified in requirement 14.3.4a.

NOTE Larger distances are preferred, even though tracks are avoided on external layers.

ECSS-Q-ST-70-12_1200513

c. The fan out should be symmetric.

NOTE This is done to avoid unwanted movement of components during reflow soldering. An example of a symmetric fan out is given in Figure 14-4.

ECSS-Q-ST-70-12_1200514

d. The SMT pad of an AAD may be asymmetric.

NOTE Examples of asymmetric SMT pad are key hole, solder verification snip. The purpose of this is to verify quality of the solder joint.

ECSS-Q-ST-70-12_1200335

e. The four quadrants of the total footprint of the AAD shall be designed point symmetric such that each quadrant has the asymmetry in four directions.

NOTE This is done to prevent the component drifting away from the footprint during assembly. An example of a point symmetric AAD footprint is given in Figure 14-5.

ECSS-Q-ST-70-12_1200336

f. The width of the track connecting to an SMT pad of a chip device should be ≤ 1/3 of the width of the pad.

NOTE 1 An illustration of fan out from SMT pad is given in Figure 14-4.

NOTE 2 In Figure 14-4: W_T is the width of the track connecting to an SMT pad of a chip device, and W_P is width of the pad

NOTE 3 This is done for thermal relief to prevent the track acting as a heat sink and removing heat from the pad during assembly.

NOTE 4 This requirement is defined for chip devices not for flat packs.

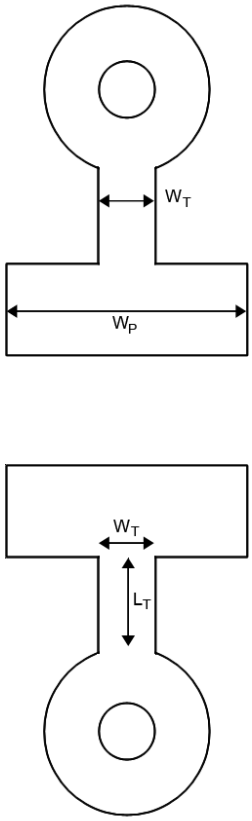


Figure 14-4: Fan out from SMT pad to via

ECSS-Q-ST-70-12_1200337

Table 14-4: Minimum track length to component pads

W_T [mm]	L_T [mm]
0,2	≥ 0,25
0,3	≥ 0,7

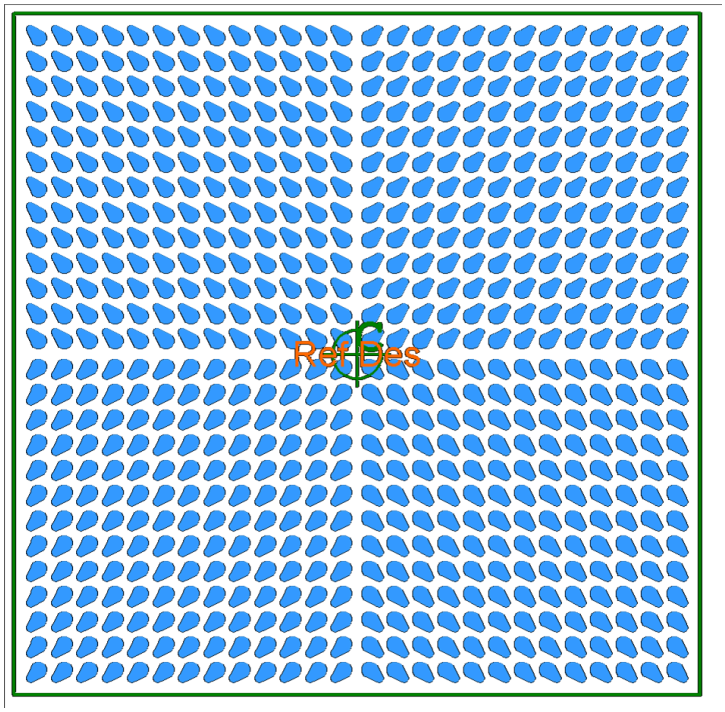


Figure 14-5: Example of point symmetric AAD footprint

14.3.5 Fan out of PTH

ECSS-Q-ST-70-12_1200338

a. The track width connecting to soldering pad of PTH should be maximum half of the diameter of the pad.

NOTE 1 An illustration of track connecting to soldering pad is shown in Figure 14-6

NOTE 2 In Figure 14-6: I_c is the track width connecting to soldering pad of PTH with diameter D.

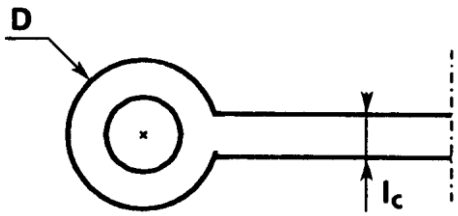


Figure 14-6: Track width (I_c) ratio to PTH pad (D) diameter.

ECSS-Q-ST-70-12_1200339

b. The track length between soldering pad of PTH and via should be at least half the diameter of the largest pad

NOTE 1 An illustration of track between soldering pad and via is shown in Figure 14-7.

NOTE 2 In Figure 14-7: L_c is the track length between soldering pad of PTH with diameter D_1 and via pad with diameter D_3.

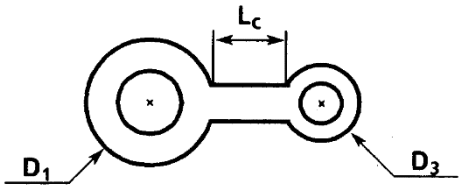


Figure 14-7: Track length (Lc) between soldering pad of PTH (D_1) and via pad (D_3)

14.4 Specific requirements for fused tin-lead finish

ECSS-Q-ST-70-12_1200515

a. Adhesive bonding should not be performed on fused tin-lead.

ECSS-Q-ST-70-12_1200340

b. Bonded devices shall have clearance for spot bonding.

14.5 Dimensional requirements for SMT foot print

14.5.1 Overview

Successful assembly verification justifies the use of pad designs provided that minimum insulation distance is achieved, as specified in requirement 14.5.2c.

The use of blind via in component pad can act as a heat sink.

This clause specifies as-manufactured pad dimensions for various component footprints. The as-designed pad dimensions depend on following:

a. the etching tolerance for the surface copper thickness,

b. etching undercut

c. tolerance of component dimensions

d. minimum width of solder fillet

e. misalignment of component on footprint

Table 14-5 Legend for dimensions of components and footprint

Minimum dimension	Description
i	insulation distance
M1	Solder fillet
M2	
M3	
X	Width of pad
AA	Distance between pads
BB	Total length of pad footprint
Y	Length of pad
L, E	Length of component
T	Length of termination
W, C	Width of termination
P	Pitch of AAD
D	Diameter of pad for AAD

14.5.2 General

ECSS-Q-ST-70-12_1200341

a. Insulation distance shall be in conformance with requirements of clauses 13.8, 13.9 and 13.10.

ECSS-Q-ST-70-12_1200342

b. The largest distance shall be used in case the distance between pads specified as AA in Table 14-6, Table 14-7, Table 14-8, Table 14-9 and Table 14-10 is smaller than the insulation distance specified in the requirement 14.5.2a.

NOTE 1 Insulation distance is indicated with the letter "i" in Figure 14-8, Figure 14-9, Figure 14-10, Figure 14-11, Figure 14-12 and Figure 14-13.

NOTE 2 The minimum insulation distance applies to all pad designs, including existing pad designs, new pad designs and pad designs not specified in this standard.

ECSS-Q-ST-70-12_1200516

c. Pad designs may deviate from the requirements of clauses 14.5.3 to 14.5.7, in case the following conditions are met:

1. the existing pad designs are verified in accordance with clause 13 of ECSS-Q-ST-70-61, and
2. insulation distance is in conformance with requirement 14.5.2a.

NOTE This requirement is defined to enable best practices as per recommendations from the EEE component manufacturer, and optimisation for assembly and PCB manufacturing.

ECSS-Q-ST-70-12_1200343

d. Pad designs of components that are not specified in requirements from clauses 14.5.3 to 14.5.8 shall be designed in compliance with the manufacturer's datasheet and requirements from clause 14.5.2a.

14.5.3 Bipolar components

ECSS-Q-ST-70-12_1200344

a. The pad design for bipolar components shall be in conformance with the as-manufactured values specified in the Table 14-6, except for the case specified in 14.5.2c

NOTE 1 Examples of bipolar components are: cylindrical, rectangular and square end-capped devices

NOTE 2 An illustration is given in Figure 14-8.

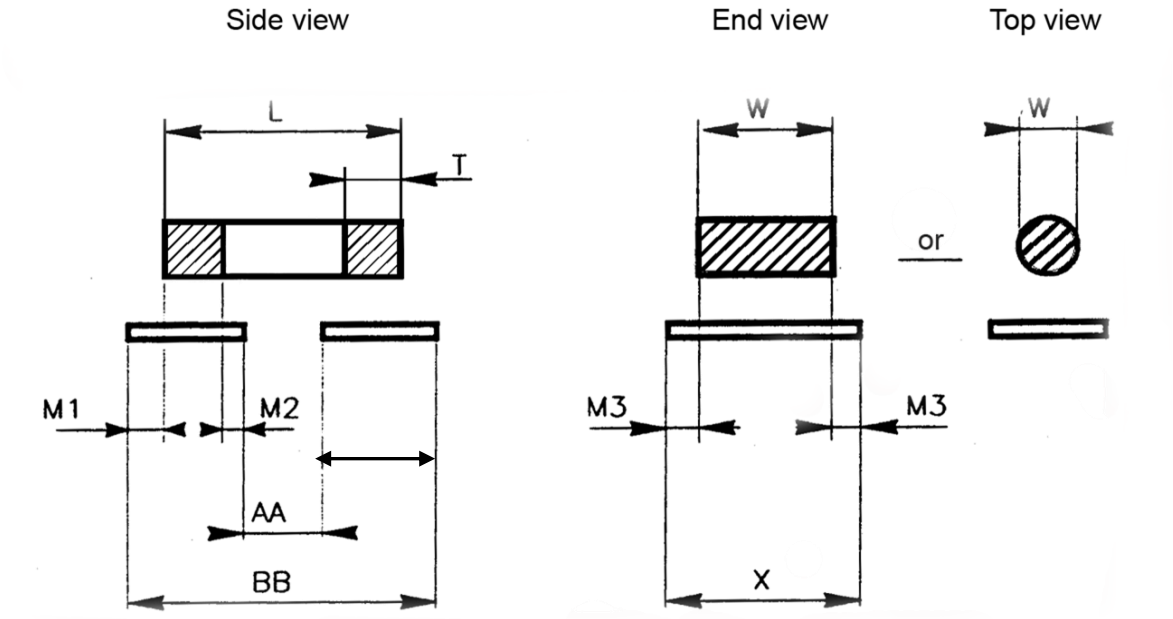


Figure 14-8:Illustration of bipolar component pads

ECSS-Q-ST-70-12_1200345

Table 14-6 As-manufactured pad sizes for bipolar components

Minimum dimension	Permitted data
M1	0,2 mm
M2	0,1 mm
M3	> 0 mm
X	W_{max}+ 2*M3
AA	L_{min}-2*(T_{max} + M2)
BB	L_{max}+2*M1
Y	$\frac{BB - AA}{2}$

14.5.4 SOIC components

ECSS-Q-ST-70-12_1200346

a. The pad design for components of type SOIC with gullwing-leads shall be in conformance with the as-manufactured values specified in Table 14-7, except for the case specified in 14.5.2c.

NOTE An illustration is given in Figure 14-9.

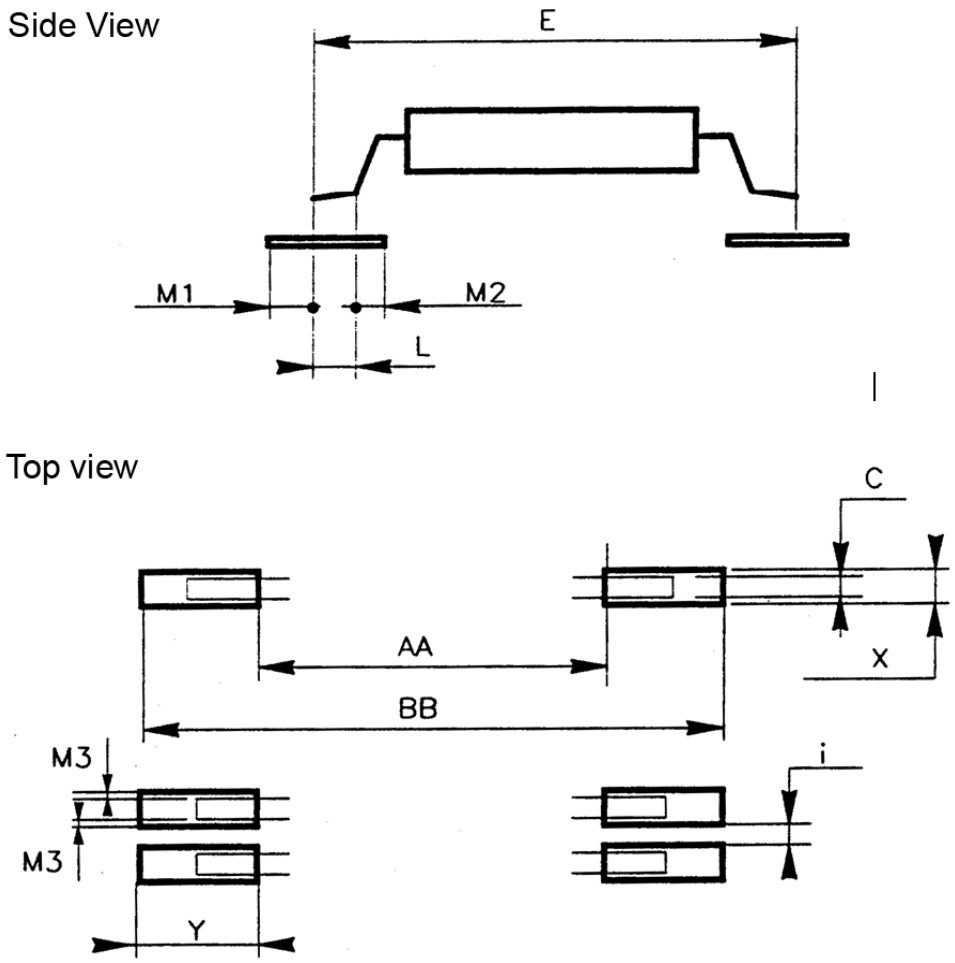


Figure 14-9: Illustration of SOIC component pads

ECSS-Q-ST-70-12_1200347

Table 14-7: As-manufactured pad sizes for SOIC components

Minimum dimension	Permitted data
M1	0,2 mm
M2	0,2 mm
M3	> 0 mm
X	C_{max}+ 2*M3
AA	E_{min}-2*(L_{max} + M2)
BB	E_{max}+2*M1
Y	$\frac{BB - AA}{2}$

14.5.5 J-leaded components

ECSS-Q-ST-70-12_1200348

a. The pad design for components with J-leads shall be in conformance with the as-manufactured values specified in Table 14-8, except for the case specified in 14.5.2c.

NOTE An illustration is given in Figure 14-10.

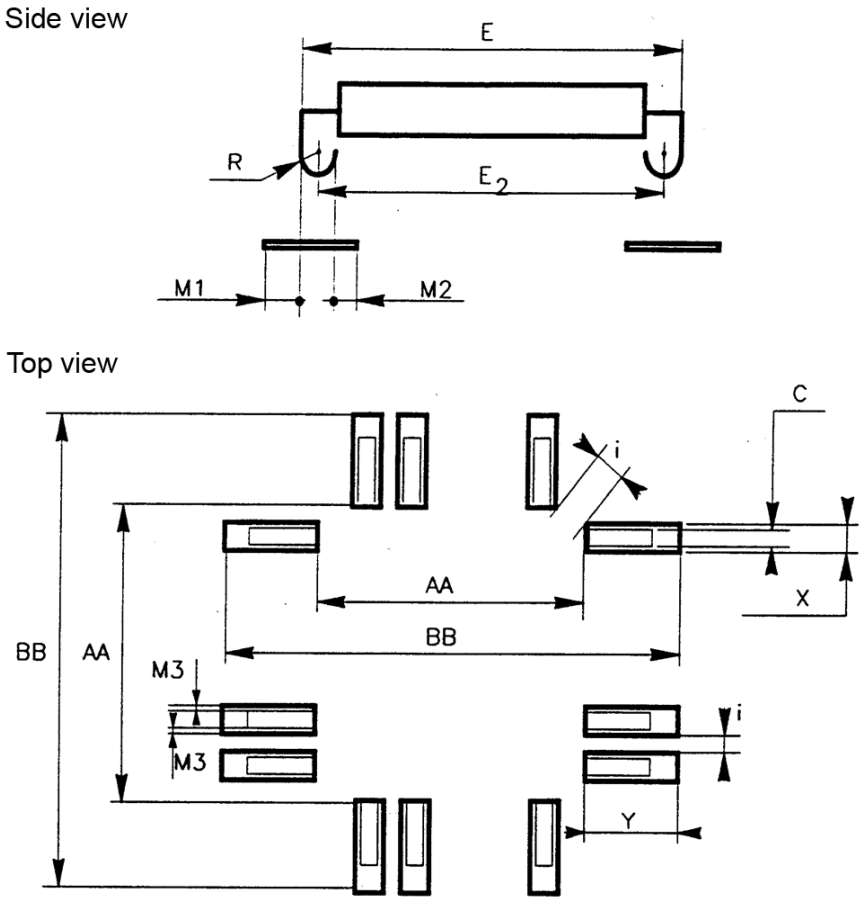


Figure 14-10: Illustration of J-leaded component pads

ECSS-Q-ST-70-12_1200349

Table 14-8: As-manufactured pad sizes for J-leaded components

Minimum dimension	Permitted data
M1	0,2 mm
M2	0,2 mm
M3	> 0 mm
X	C_{max}+ 2*M3
AA	$E_{2\,min}$-2*(R_{max} + M2)
BB	E_{max}+2*M1
Y	$\frac{BB - AA}{2}$

14.5.6 LCC components

ECSS-Q-ST-70-12_1200350

a. The pad design for components of type LCC shall be in conformance with the as-manufactured values specified in the Table 14-9, except for the case specified in 14.5.2c.

NOTE 1 An illustration is given in Figure 14-11.

NOTE 2 LCC means leadless chip carrier.

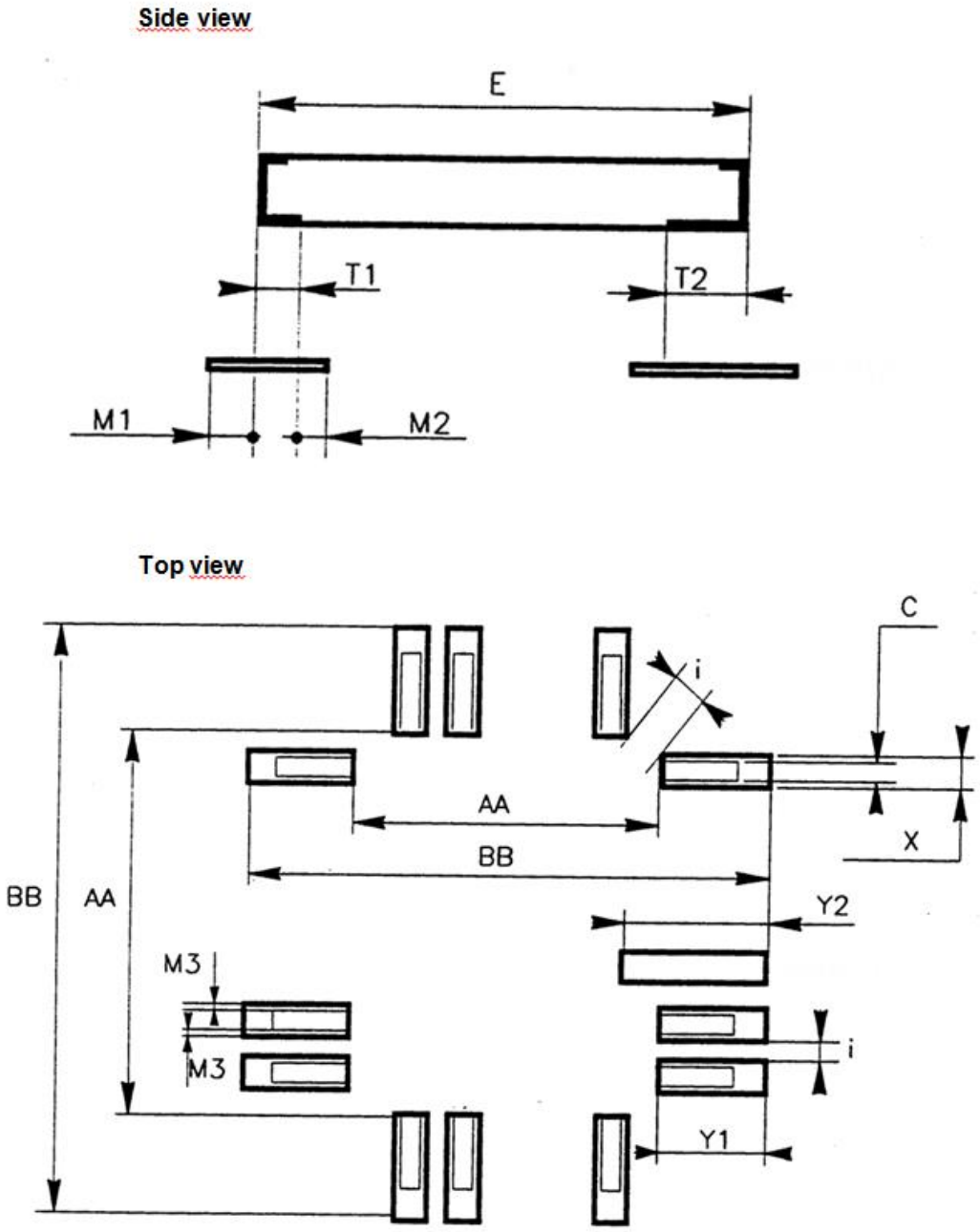


Figure 14-11: Illustration of LCC component pads

ECSS-Q-ST-70-12_1200351

Table 14-9: As-manufactured pad sizes for LCC components

Minimum dimension	Permitted data
M1	0,2 mm
M2	0,2 mm
M3	> 0 mm
X	C_{max}+ 2*M3
AA	E_{min}-2*(T1+ M2)
BB	E_{max}+2*M1
Y1	$\frac{BB - AA}{2}$
Y2	Y1+(T2- T1)

14.5.7 Flat pack components

ECSS-Q-ST-70-12_1200352

a. The pad design for components of type FP and QFP shall be in conformance with the as-manufactured values specified in the Table 14-10, except for the case specified in 14.5.2c.

NOTE 1 An illustration is given in Figure 14-12.

NOTE 2 FP means flat pack. QFP means quad flat pack.

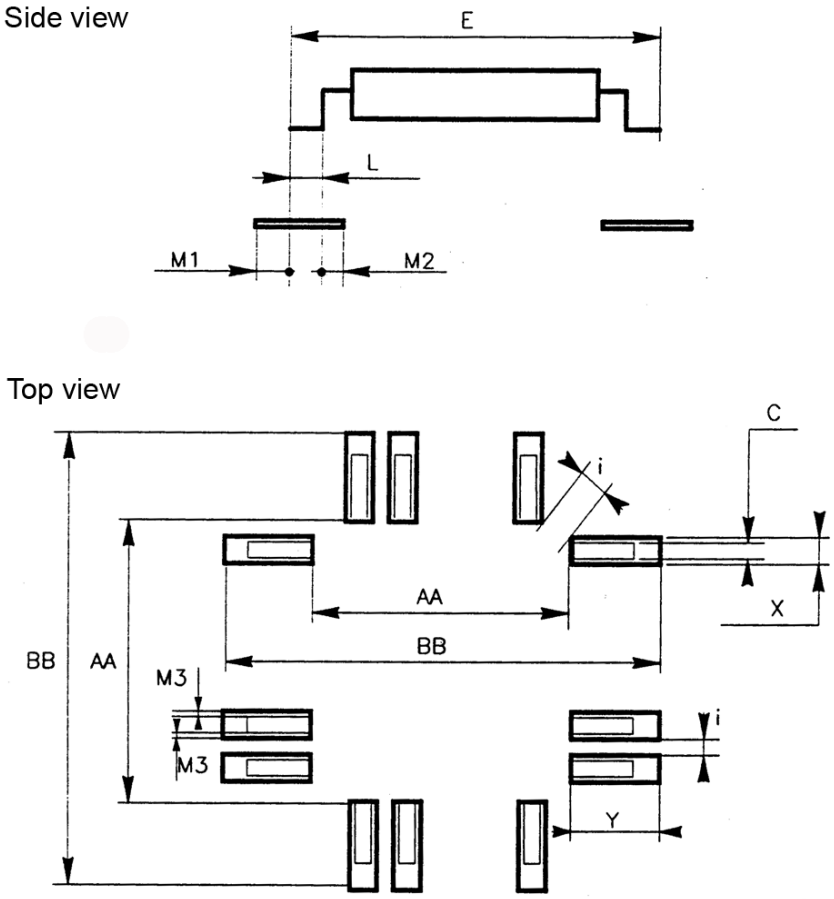


Figure 14-12: Illustration of FP and QFP component pads

ECSS-Q-ST-70-12_1200353

Table 14-10: As-manufactured pad sizes for FP and QFP components

Minimum dimension	Permitted data
M1	0,2 mm
M2	0,2 mm
M3	> 0 mm
X	C_{max}+ 2*M3
AA	E_{min}-2*(L_{max} + M2)
BB	E_{max}+2*M1
Y	$\frac{BB - AA}{2}$

14.5.8 AAD components

ECSS-Q-ST-70-12_1200517

a. The pad design for components of type AAD should be in conformance with the as-designed values specified in Table 14-11.

NOTE An illustration of circular pad design for AAD footprint is given in Figure 14-13. An illustration of teardrop pad design of AAD footprint is given in Figure 14-5.

ECSS-Q-ST-70-12_1200518

b. The pad design for components of type AAD should be circular or with teardrop.

ECSS-Q-ST-70-12_1200519

c. The pad design for components of type AAD should be with via-in-pad technology.

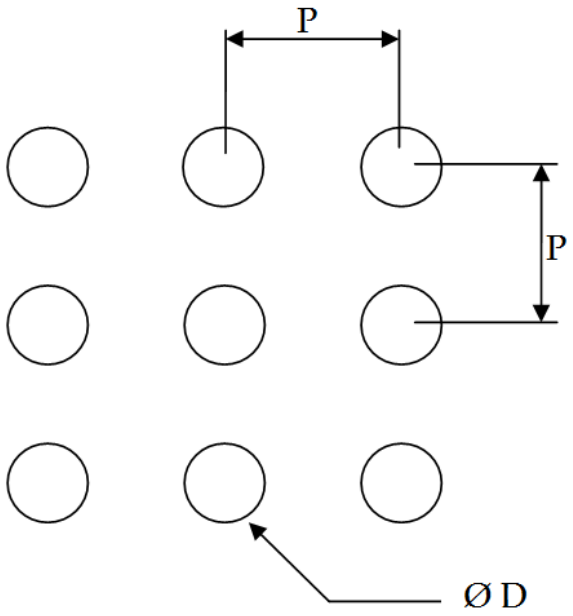


Figure 14-13: Illustration of AAD component pads

ECSS-Q-ST-70-12_1200520

Table 14-11: As-designed pad diameter for AAD components

Component pitch (P)	Minimum pad diameter (D)
1,27 mm	0,7 mm
1,0 mm	0,6 mm

15
Design of test coupon

15.1 Design rules for test coupon

ECSS-Q-ST-70-12_1200354

a. The supplier shall be accountable for the design of the test coupon in conformance with requirements from the Clause 15.

ECSS-Q-ST-70-12_1200355

b. The design of the test coupon shall be indicated as a Review Item.

NOTE It is common practice that the PCB manufacturer designs the coupon on behalf of the supplier. However, these requirements ensure that the supplier verifies the design of the coupon and has the end responsibility.

15.2 Test coupon design

ECSS-Q-ST-70-12_1200521

a. The test coupon design should be representative of the PCB.

ECSS-Q-ST-70-12_1200522

b. In case the PCB design is complex and the coupon cannot be designed with full representativity, the inspection on the coupon should be supplemented by a FAI.

NOTE The different density of a coupon compared to the rest of the PCB can limit the representativity. A higher copper density of the footprint of an AAD compared to a typical coupon design can cause a lower plating thickness. The higher via density of the footprint of an AAD can cause problems with resin flow and filling, which can remain undetected in a coupon of different density. High pressure areas local within the PCB can cause lower dielectric spacing compared to the coupon.

ECSS-Q-ST-70-12_1200523

c. Test coupon location in the manufacturing panel should be representative of the worst case.

NOTE Worst-case location for registration is typically on the corners of the panel. However, worst-case for plating is typically in the centre of the panel. In this case, it is important the PCB manufacturer compares the plating thickness in the coupon with the rest of the panel. This is typically verified during qualification.

ECSS-Q-ST-70-12_1200356

d. The following specific features shall be represented on the coupon in the same configuration as on the PCB:

1. PCB build-up,
2. Copper planes,
3. Non-functional pads,
4. Internal heat sinks,
5. Hole types as follows:
   (a) PTH for components
   (b) Through-hole vias
   (c) Blind vias
   (d) Buried vias
   (e) Microvias in the same configuration as on the PCB
6. The minimum hole size of each type.
7. The pad stack with the minimum pad diameter
8. Either the maximum component hole size or the most frequently used component hole size.
9. The minimum track width and spacing on each layer.
10. All used surface finishes and overlap zones in conformance with requirement 7.8.1d.1.
11. All plating, drilling and lamination sequences.
12. Backdrilling of vias including:
    (a) Backdrill depth
    (b) Backdrill orientation
13. Embedded film resistors of highest and lowest resistance
14. Flex layers including cut-out and cover layer placement

NOTE 1 Minimum hole size is included into requirement 15.2d.6 to verify plating in maximum aspect ratio holes.

NOTE 2 The pad stack with minimum pad diameter is included into requirement 15.2d.7 to verify worst-case annular ring as-manufactured and registration.

NOTE 3 In the requirement 15.2d.8 the supplier can decide which hole sizes to be incorporated on the coupon.

NOTE 4 Minimum track width and spacing is included into requirement 15.2d.9 to be verified as function of copper thickness on a dedicated pattern.

ECSS-Q-ST-70-12_1200357

e. In case teardrop reinforcement is used on the PCB, the following conditions shall be designed on the coupon:

1. the teardrop reinforcement is not included on the coupon, and
2. the minimum pad diameter is included on the coupon.

NOTE This is done to ensure the annular ring requirement specified in the 7.5.3l.1 (i.e. 25 µm) is achieved without teardrop reinforcement.

ECSS-Q-ST-70-12_1200358

f. The coupons shall be capable of completing the following tests:

1. Thermal tests:
   (a) Solderability,
   (b) Rework Simulation,
   (c) Thermal Stress.
2. Mechanical tests:
   (a) Peel strength,
   (b) Pull-off test,
   (c) Flex bend cycles,
   (d) Tape bond test.
3. Electrical tests:
   (a) Insulation resistance,
   (b) Interconnection resistance and continuity test,
   (c) Inter-layer dielectric withstanding voltage,
   (d) Controlled impedance,
   (e) Embedded film resistance.
4. Dimensional inspection:
   (a) Annular ring,
   (b) Track width and spacing.
5. Inspection of general aspect in microsections.

ECSS-Q-ST-70-12_1200359

g. A dedicated coupon pattern shall be implemented to verify controlled impedances, when used on the PCB.

NOTE This dedicated coupon can be designed by the PCB manufacturer.

ECSS-Q-ST-70-12_1200524

h. With multiple small PCBs on a panel, a spare PCB may be used instead of a coupon.

ECSS-Q-ST-70-12_1200360

i. Each coupon shall have a serial number that ensures traceability to the panel.

Annex A (normative)
PCB definition dossier - DRD

A.1 DRD identification

A.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-12 requirement 5.2a.

A.1.2 Purpose and objective

The PCB definition dossier specifies the design and contains all information required for the tooling. The PCB definition dossier is part of the PCB manufacturing dossier under approval in the MRR.

A.2 Expected response

A.2.1 Scope and content

<1> General

ECSS-Q-ST-70-12_1200361

a. The PCB definition dossier shall include the following data:
   1. Description, as specified in A.2.1<2>,
   2. Mechanical layout, as specified in A.2.1<3>,
   3. Artwork data , as specified in A.2.1<4>,
   4. Drawing, as specified in A.2.1<5>,
   5. Specific electrical test, as specified in A.2.1<6>,
   6. Review Items , as specified in A.2.1<7>,
   7. Check list, as specified in A.2.1<8>,

<2> Description

ECSS-Q-ST-70-12_1200362

a. The PCB definition dossier shall include a description containing at least the following data:

1. Base material,
2. Finishes,
3. Number of layers,
4. Size,
5. Thickness and tolerance,
6. Part number of PCB design: specified by supplier,
7. Revision number of PCB design,
8. Heat sink including:
   (a) Heat sink thickness,
   (b) Tolerances permitted,
   (c) Material used,
   (d) Type of protective surface coating.

NOTE Synonyms of revision number in requirement 7 are issue number and version number.

<3> Mechanical layout

ECSS-Q-ST-70-12_1200363

a. The PCB definition dossier shall include the mechanical layout containing at least the following data:

1. One or more mechanical drawings including a dimensioning system,
2. Location and form for the PCB manufacturer to place date code and serialization.

NOTE 1 It is recommended in the requirement 1 to use a reference hole as datum point. The reference hole is recommended to be drilled in the first drill cycle.

NOTE 2 The form of numbering as specified in requirement 2 can be in ink or conductive pattern.

NOTE 3 An example of mechanical layout is shown in Figure A-1.

<4> Artwork data

ECSS-Q-ST-70-12_1200364

a. The PCB definition dossier shall include the artwork data containing at least the following information:

1. Artwork data of each conductive PCB layer,
2. Artwork data for non-conductive layers,
3. Drilling and milling files.

NOTE 1 Examples of conductive layers for the requirement 1 are circuitry and selective finishes.

NOTE 2 Examples of non-conductive layers for the requirement 2 are solder mask and silk screen

NOTE 3 It is preferred in the requirement 3 to distinguish by different tool codes the plated and non-plated holes in the drill file even if they have identical diameter.

NOTE 4 For example, ODB++ is a format that describes all artwork of all layers in one file.

<5> Drawing

ECSS-Q-ST-70-12_1200365

a. The PCB definition dossier shall include the drawings containing at least the following:

1. Drilling drawing,
2. Drilling tables, including:
   (a) Symbol,
   (b) Diameter of as-manufactured holes,
   (c) Tolerance,
   (d) Plated or not plated,
   (e) Quantity.
3. Build-up data, including:
   (a) Numbered conductive layers from top to bottom,
   (b) Total copper thickness, basic + plated, for each layers with tolerances,
   (c) Presence of planes: ground and supply, mesh plane or full copper,
   (d) Presence of layers with controlled impedance,
   (e) Thickness tolerance of laminate and prepreg, including minimum as-manufactured insulation distances,

(f) Total PCB thickness and tolerance,

(g) Specification if thickness is measured over bare laminate or over conductive pattern,

(h) Specific requirements for build-up.

NOTE 1 Examples of specific requirements for build-up are:

- style of prepreg and laminate,
- use of separate copper foil or copper cladding on laminate for external layers,
- use of single or double sided laminate,
- use of two individually cured insulators to achieve double insulation.

NOTE 2 Examples of Drilling drawing, Drilling table and Build-up data are given in Figure A-2, Figure A-3, Figure A-4.

<6> Electrical test

ECSS-Q-ST-70-12_1200366

a. The PCB definition dossier shall include the electrical test description containing at least the following data:

1. Netlist,
2. Definition of any electrical tests that are specific to the PCB design and in addition to the standard set of electrical tests,
3. Identification of conductive lines that are designed to be of higher DC resistance that are at risk not to pass standard continuity testing,
4. The definition of controlled impedance tracks including:
   (a) Reference planes,
   (b) Type of coupling,
   (c) Track dimensions, including height, width, cross section,
   (d) Spacing dimensions in X,Y and in Z direction,
   (e) Impedance value, tolerance and method of measurement.
5. Identification of any deliberate errors.

NOTE 1 Example for requirement 4(b): broadside coupled, edge coupled.

NOTE 2 In the requirement 4(e) the standard method for measuring impedance and tolerance is TDR in case the method is not specified

NOTE 3 Example for the requirement 5 are differences between artwork and net list such as star points.

<7> Review Items

ECSS-Q-ST-70-12_1200367

a. The PCB definition dossier shall include all Review Items.

NOTE The following design features are required to be recorded as Review Items by the present standard:

1. Asymmetric build-up as specified in 7.1.1b,
2. Molybdenum or CIC layers as specified in 7.1.1c
3. Asymmetric copper cladding as specified in 7.1.2b,
4. Total copper thickness >700 µm as specified in 7.1.2g,
5. Single sheet of glass reinforcement in laminate as specified in 7.1.3c,
6. 4 mil laminate as specified in 7.1.3f,
7. 5 mil laminate at >30V as specified in 7.1.3g,
8. Total PCB thickness as specified 7.3.2c and 7.3.3c,
9. Reduced as-designed track width and spacing as specified in 7.4.3c and 7.4.4c,
10. Fine pitch tracks as specified in 7.4.3g, and 7.4.5b,
11. Removal of non-functional pads as specified in 7.5.2c,
12. Reduced as-designed pad dimensions on solder side and component side as specified 7.5.3e and 7.5.3g,
13. Pad diameter on rigid laminate <0,3mm larger than drilled hole as specified in 7.5.3j,
14. Non-circular pads as specified in 7.5.4b
15. Asymmetric copper planes as specified in 7.6e,
16. Mixed surface finish as specified in 7.8.1e,
17. 70 µm copper cladding in flex laminate as specified in 8.3.3c,
18. Full copper planes in flex laminate as specified in 8.3.4b,
19. 70 µm copper foil in combination with no-flow prepreg as specified in 9.3d,
20. More than 2 flex laminates as specified in 9.3f,
21. Pad diameter on flex laminates <0,6 mm larger than diameter of drilled hole as specified in 9.6b,
22. Heat sinks and their mechanical stability as specified in 10.2a, 10.3.3a and 10.4.4a.
23. Conductive surface pattern below external heat sink as specified in 10.3.2g,
24. HDI as specified in 11.2c,
25. Basic copper layer thickness <17 µm as specified in 11.4.1e,

26. Diameter of external pad of microvia <0,15 mm larger than the ablated hole as specified in 11.4.3b,
27. Reduced annular ring with teardrop reinforcement as specified in 11.5.2a,
28. Differential pair routed in 1 mm pitch AAD footprint as specified in 11.5.5a,
29. Aspect ratio of vias >7 for 1 mm pitch AAD footprint as specified in 11.5.6a,
30. Embedded film resistors as specified in the requirements 12.3a and 12.3i,
31. Thickness of RF PCB >3mm as specified in 12.4b,
32. Number of layers in RF PCB >8 as specified in 12.4d,
33. Reduced insulation distance for RF elements as specified in 12.5.1b,
34. Z-controlled backdrilling as specified in 12.9a,
35. Profiled top layers as specified in 12.8b,
36. Profiled aluminium backing as specified in 12.8c,
37. Reduced as–designed insulation distance as specified in 13.10c,
38. Controlled impedance tracks as specified in 13.11.2,
39. Design of test coupon as specified in 15.1b.
40. Copper distribution and thickness after plating of microvia layers with 1 sheet of prepreg as specified in 11.4.1k.7,
41. Possible tape testing on PCB as specified in 9.4.5g of ECSS-Q-ST-70-60.

ECSS-Q-ST-70-12_1200368

b. The PCB definition dossier shall include all specific inspections required for the Review Items.

<8> Check list

ECSS-Q-ST-70-12_1200369

a. The PCB definition dossier shall include a check list containing at least the following data:

1. all file names included in the archive,
2. last modified data of each file,
3. size of the file,
4. CRC.

NOTE The purpose of the check list is to define the content of the archive file to prevent transmission of wrong data. In Figure A-5 an example of a check list is shown. The check list

indicates the content of the archive file by the four items mentioned in A.2.1<8>.

A.2.2 Special remarks

ECSS-Q-ST-70-12_1200370

a. The format of the data of the PCB definition dossier shall be agreed between supplier and PCB manufacturer.

ECSS-Q-ST-70-12_1200525

b. One single file should be used for transferring the data between supplier and PCB manufacturer.

ECSS-Q-ST-70-12_1200526

c. The transmitted file should be an archive with lossless compression.

NOTE Examples of file extensions of archives with lossless compression are: .zip, .rar,.7z, .tar.

ECSS-Q-ST-70-12_1200371

d. The supplier shall ensure the file format enables verification of file integrity to prevent corruption.

NOTE For example verification by CRC.

A.2.3 Example figures

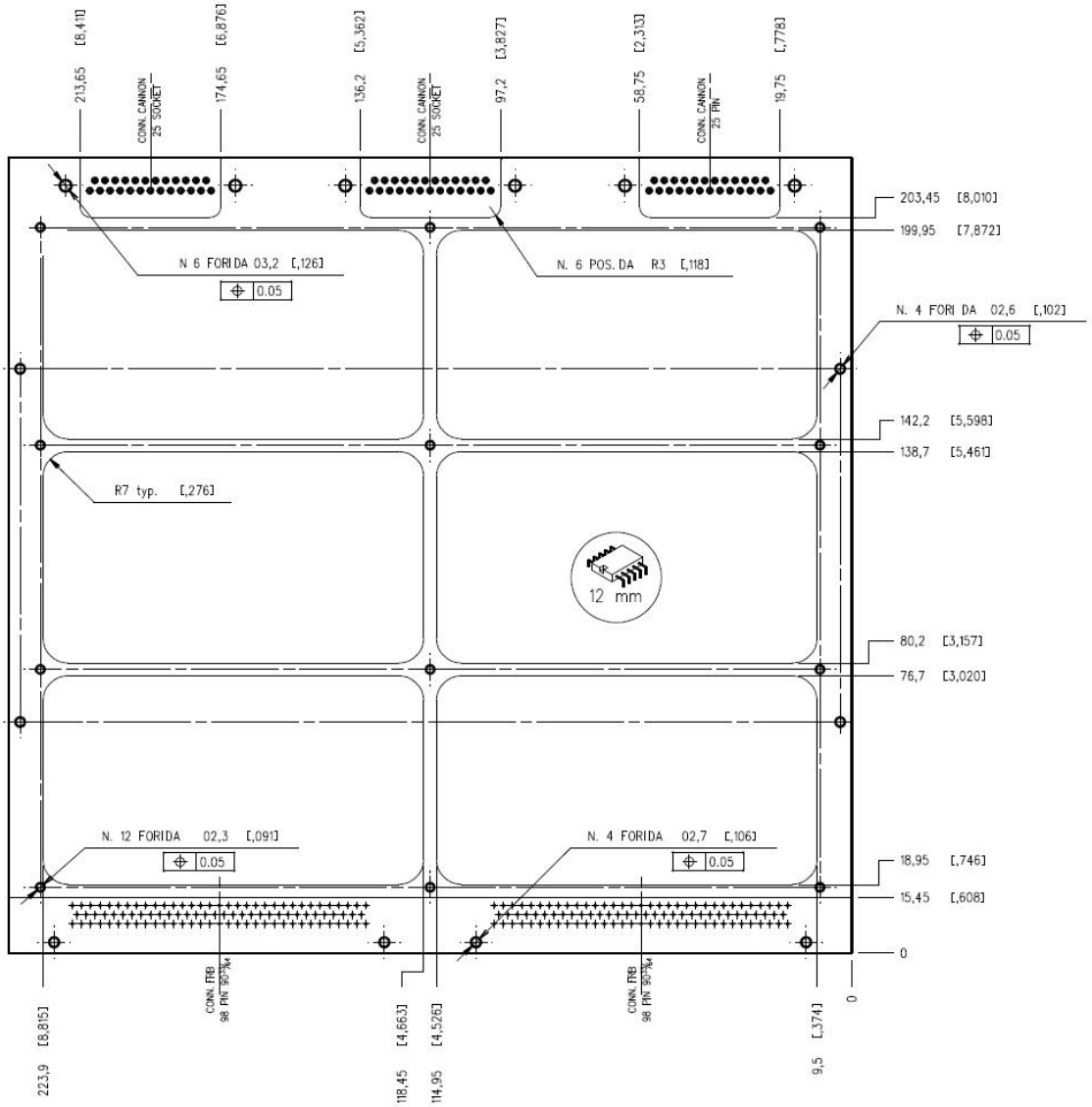


Figure A-1: Example of PCB mechanical layout

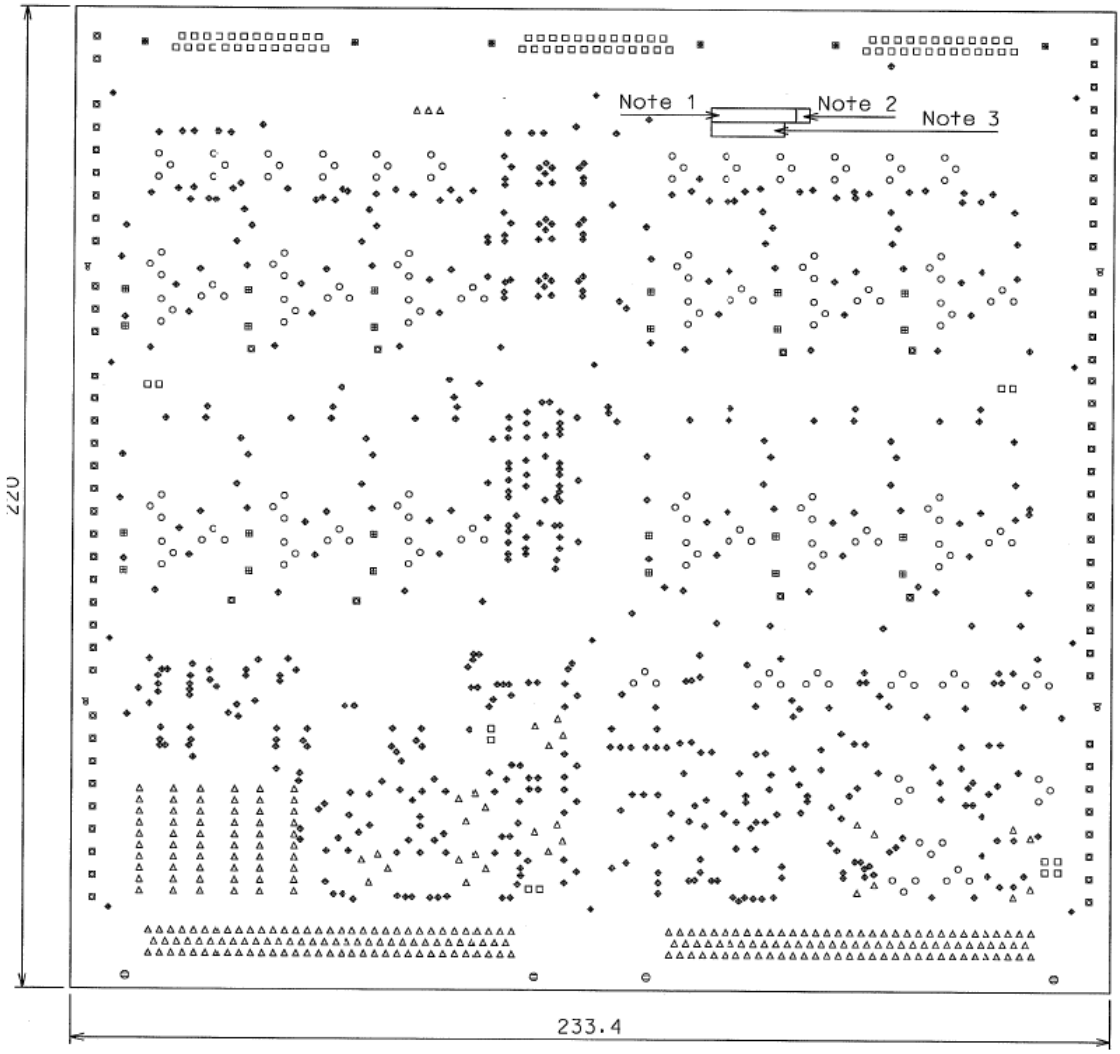
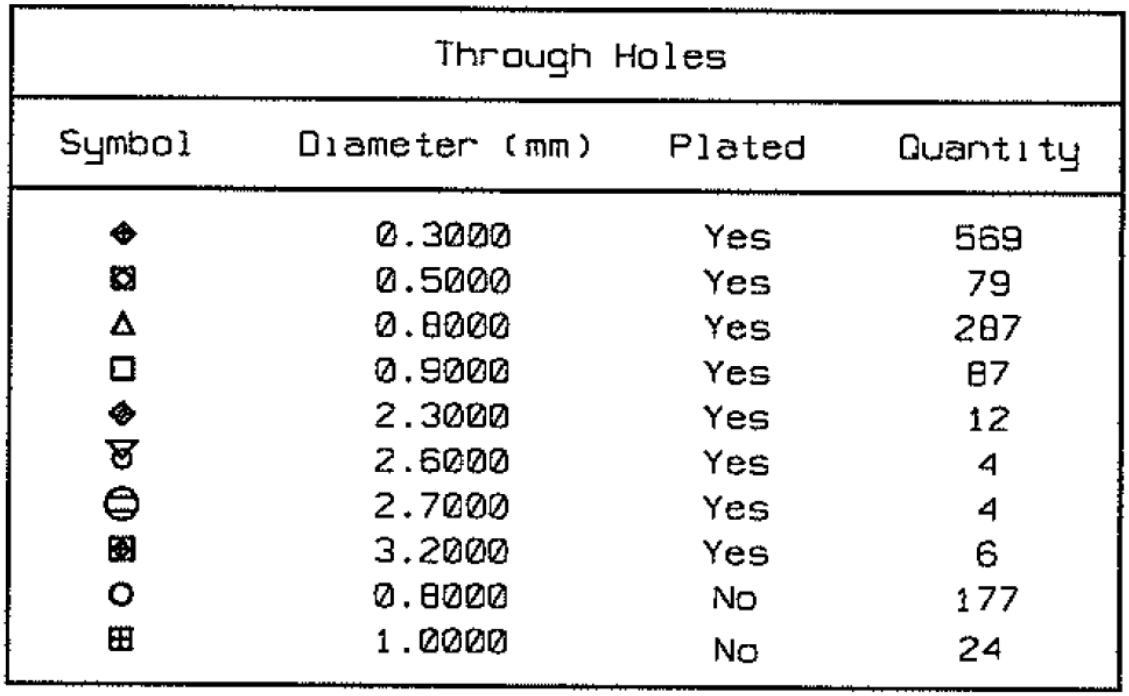


Figure A-2: Example of a drilling drawing



Through Holes			
Symbol	Diameter (mm)	Plated	Quantity
	0.3000	Yes	569
	0.5000	Yes	79
	0.8000	Yes	287
	0.9000	Yes	87
	2.3000	Yes	12
	2.6000	Yes	4
	2.7000	Yes	4
	3.2000	Yes	6
	0.8000	No	177
	1.0000	No	24

Figure A-3: Example of a table indicating as-designed plated hole diameters

	Stack	Insulation thickness (as-manufactured board) (µm)	Copper plane	Base copper thick-ness (µm)	Drilling								Total copper thickness (as-manufactured board) (µm)		Number of layers
							1		2		3		As-designed (µm)	Tolerances	
1				17									77,5	±30%	1
		100µm min													
2				35									35	±20%	2
		100µm min													
3				35									35	±20%	3
		100µm min													
4				35									35	±20%	4
		100µm min													
5				35									35	±20%	5
		100µm min													
6				35									35	±20%	6
		100µm min													
7			Yes	35									35	±20%	7
		100µm min													
8			Yes	35									60	±20%	8
		100µm min													
9			Yes	35									60	±20%	9
		100µm min													
10			Yes	35									35	±20%	10
		100µm min													
11				35									35	±20%	11
		100µm min													
12				35									35	±20%	12
		100µm min													
13				35									35	±20%	13
		100µm min													
14				35									35	±20%	14
		100µm min													
15				35									35	±20%	15
		100µm min													
16				17									77,5	±30%	16

Figure A-4: Example of build-up data

Grb700200846-01revA\

File Name	File Type	Modified	Size	Ratio	Packed	CRC
DrillDrawing.gdo	File GDO	12-11-2009 10.49.38	240,904	76%	58,980	995DD56E
driver_mpe.dsn	Nome origine dati	12-11-2009 10.49.38	1,910	75%	482	30229A0B
Layer10Bottom.gbr	File GBR	12-11-2009 10.49.38	82,433	73%	21,955	E7BC9C4F
Layer1Top.gbr	File GBR	12-11-2009 10.49.38	118,527	75%	30,156	AA09CA45
Layer2.gbr	File GBR	12-11-2009 10.49.38	159,644	72%	44,086	F615F85B
Layer3.gbr	File GBR	12-11-2009 10.49.38	22,200	68%	7,091	6DD85226
Layer4.gbr	File GBR	12-11-2009 10.49.38	41,301	70%	12,394	45F936B2
Layer5.gbr	File GBR	12-11-2009 10.49.38	157,225	74%	41,549	08D530E4
Layer6.gbr	File GBR	12-11-2009 10.49.38	155,765	73%	41,589	0E14CD46
Layer7.gbr	File GBR	12-11-2009 10.49.38	27,191	68%	8,801	081B59D0
Layer8.gbr	File GBR	12-11-2009 10.49.38	83,037	73%	22,178	58AF5FED
Layer9.gbr	File GBR	12-11-2009 10.49.38	159,429	72%	43,981	496A1F1F
pwb700200846-01revA.dxf	File DXF	01-03-2010 12.07.14	1,899,315	91%	172,721	14331470
PWB700200846-01_REV_A.pdf	Adobe Acrobat Document	01-03-2010 11.55.42	117,405	10%	105,790	BC2E384F

Figure A-5: Example of the archive file with CRC

Annex B (normative)
PCB manufacturing dossier – DRD

B.1 DRD identification

B.1.1 Requirement identification and source document

This DRD is called from the ECSS-Q-ST-70-12 requirement 5.2h

B.1.2 Purpose and objective

The PCB manufacturing dossier specifies the tooling and contains all information required for the manufacture. The PCB manufacturing dossier is under approval in the MRR.

B.2 Expected response

B.2.1 Scope and content

ECSS-Q-ST-70-12_1200372

a. The PCB manufacturing dossier shall contain following information:
   1. Reference to the purchase order including the following items:
      (a) ID number
      (b) Line item numbers for each required PCB type
      (c) Line item numbers for each required PCB tooling
      (d) Line item numbers for other required services like FAI
      (e) Required quantities for each line item
      (f) Required delivery dates for each line item
   2. Reference to the PCB definition dossier for each PCB type.
   3. Tooling files
      (a) Imaging
      (b) Drilling
      (c) Milling or routing
      (d) Plating

(e) Lamination

(f) AOI

(g) Electrical testing

(h) Process route card or traveller information

(i) Inspection drawings

4. MRR checklist

NOTE An example of an MRR checklist is provided in Annex G.

ECSS-Q-ST-70-12_1200373

b. The supplier and PCB manufacturer shall document in the MRR checklist their approval of the PCB manufacturing dossier, the PCB definition dossier and all Review Items.

B.2.2 Special remarks

None

Annex C (informative) Example of capability list of PID

Example of technical capabilities of PCB manufacturer as specified in the PID is shown in the Table C-1.

Table C-1: Example of technical capabilities of PCB manufacturer as specified in the PID

PCB		
PID		
Technology	DS	
	ML	
	Rigid-flex	
	HDI	
Number layers /sequence	Rigid	
	Flex	
	Drilling sequence	
	Lamination sequence	
Thickness/size	PCB Size (mm)	
	Maximum PCB Thickness (mm)	
	External minimum Cu thickness (µm)	
	External maximum Cu thickness (µm)	
	Internal minimum Cu thickness (µm)	
	Internal maximum Cu thickness (µm)	
Material	Epoxy	
	HTg epoxy	
	Polyimide	
	Flexible	
	PTFE	
	Mixed materials	
	Metal core	

Surface finish	Sn/Pb reflow	
	Ni/Au electroplated (Hard/soft)	
	ENIG	
	Tin diffusion layer	
	Soldermask	
Design features	External trace width (µm)	
	External space width (µm)	
	Internal trace width (µm)	
	Internal space width (µm)	
	Min Z insulation thickness (µm)	
Min hole size	PTH	
	Blind	
	Buried	
	Microvia	
Aspect ratio	PTH	
	Blind	
	Buried	
	Microvia	

Annex D (informative) Track current rating computation methodology

D.1 Introduction of the three models

D.1.1 Overview

Track current rating can be computed with the following three commonly used models:

- IPC-2221A. The original chart dated from the 1950's from National Bureau of Standards as shown in figure 6.4 IPC-2221A (also referenced in Appendix A7 of IPC-2152) This model has been superseded by IPC-2152.
- IPC-2152 using the conductor sizing chart for vacuum and space environment in chapter 5.2.2 (dated August 2009).
- CNES/QFT/IN.0113.

The three models are similar for current rating computation. The CNES model is slightly more conservative than IPC-2152. An example is shown in Figure D-1.

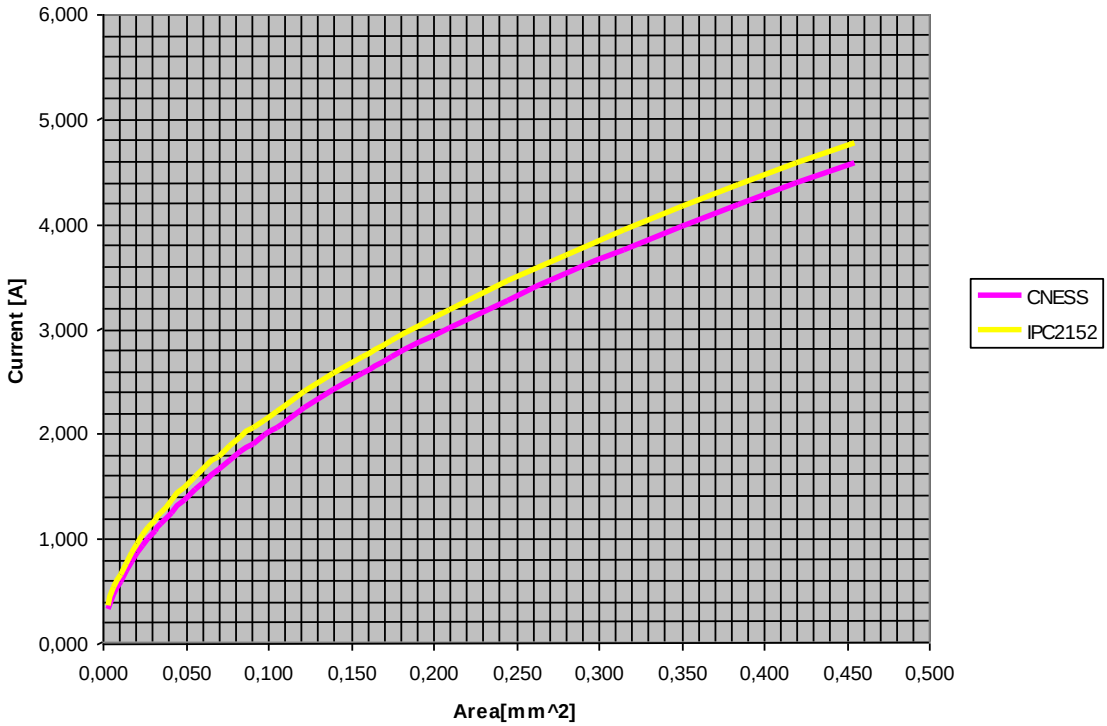


Figure D-1: Comparison between CNES and IPC-2152 current rating at 5°C increase

D.1.2 Formulae for the three models

a. In the three models the temperature increment of tracks is calculated with respect to the initial temperature of the PCB when it is not powered.

b. Current rating and cross sectional area are calculated in the three models by using the following formulae:

1. Current rating [I in Amp]
2. Cross sectional area of tracks [A in mm2]
3. Temperature increment of tracks [ΔT in °C].
4. Constants k0, k1, m0, m1. The values of the constants are specified in the paragraphs describing each model.
5. Conversion factor mm^2 to $mils^2$ c1=1550.
6. Formula for current rating:

$$I = k_0 \cdot \Delta T^{k_1} \cdot \left(c_1 \cdot A\right)^{m_0 \cdot \Delta T^{m_1}}$$

7. Formula for cross sectional area:

$$A = \frac{1}{c_1} \cdot \left(\frac{I}{k_0 \cdot \Delta T^{k_1}} \right)^{\frac{1}{m_0 \cdot \Delta T^{m_1}}}$$

D.1.3 Example of current rating

Using the mathematical model of IPC-2152 specified in clause D.2, to carry a current of 1 A and to maintain a temperature increment of 5 °C, a track of as-manufactured thickness of 25 µm (as-designed thickness of 35 µm, as per Table 7-1) should have an as-manufactured track width of 925 µm (as-designed width of 975 µm, as per Table 7-3).

D.2 Track current rating computation based on IPC-2152

The IPC-2152 is the most comprehensive standard for the computation of the track current rating. It includes track sizing charts for vacuum or space environment, for several PCB thicknesses and for several copper plane thicknesses in SI (metric) and Imperial (inch) units. This standard allows to accurately calculate the current rating of a track from cross sectional area and the temperature rising of the track. However no derating are applied to take into account the complexity of the PCB.

The model presented in this clause is based on a curve fitting performed on Figure 5-14 of chapter 5.2.2. of IPC-2152.

c. The model is valid for a range up to 30 A and up to 100°C temperature increment with respect to an initial PCB temperature of 25°C when not powered.

d. Current rating and cross sectional area are calculated as per the formula in clause D.1.2 with the following constants:

   1. k0 = 0,0756
   2. k1 = 0,4375
   3. m0 = 0,5000
   4. m1 = 0,0301

e. Example charts based on this model are shown in Figure D-2 to Figure D-7.

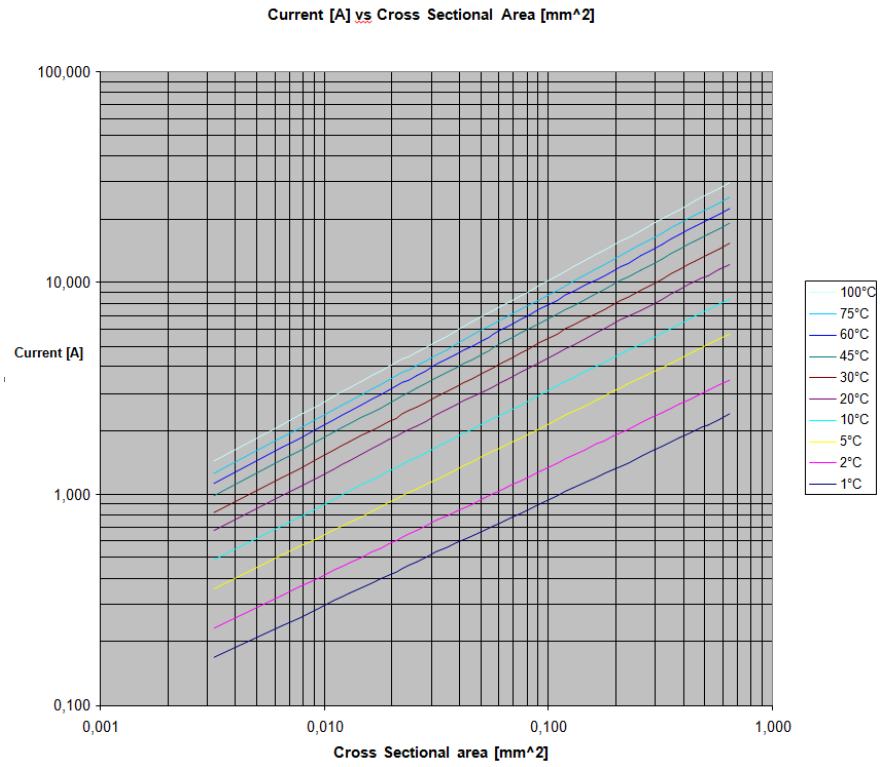


Figure D-2: IPC-2152: Current rating [A] vs cross sectional area [mm²] in double log scale

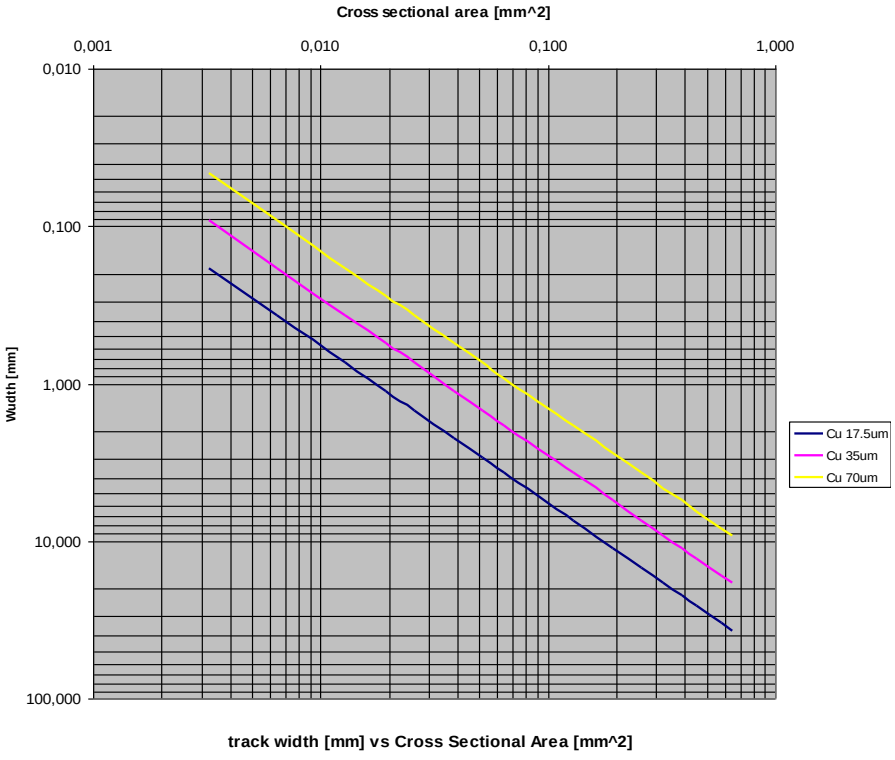


Figure D-3: IPC-2152: Track width [mm] vs cross sectional area [mm²]

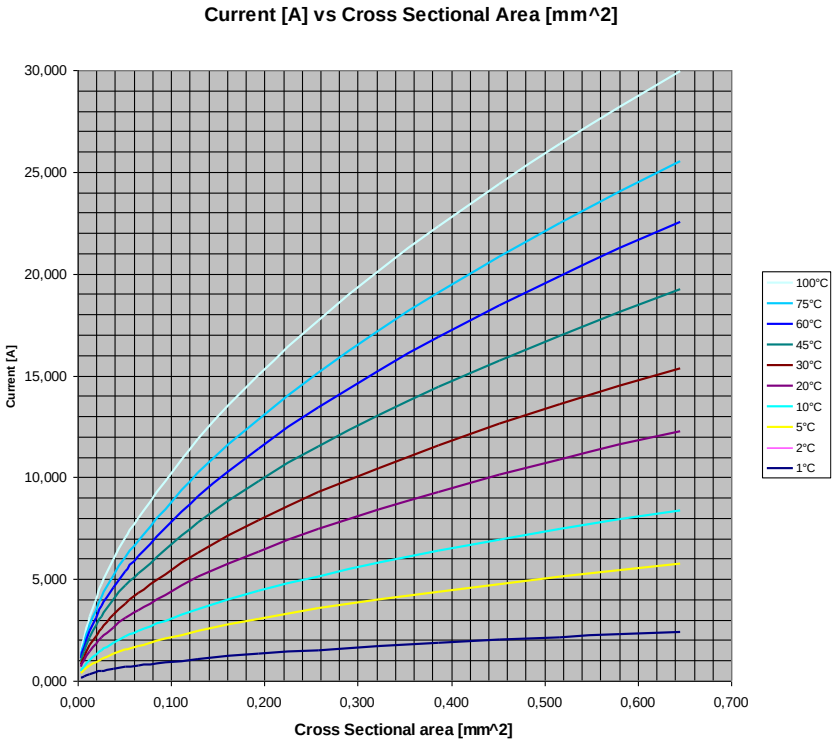


Figure D-4: IPC-2152: Current rating based on Figure D-2, range 0-25 A

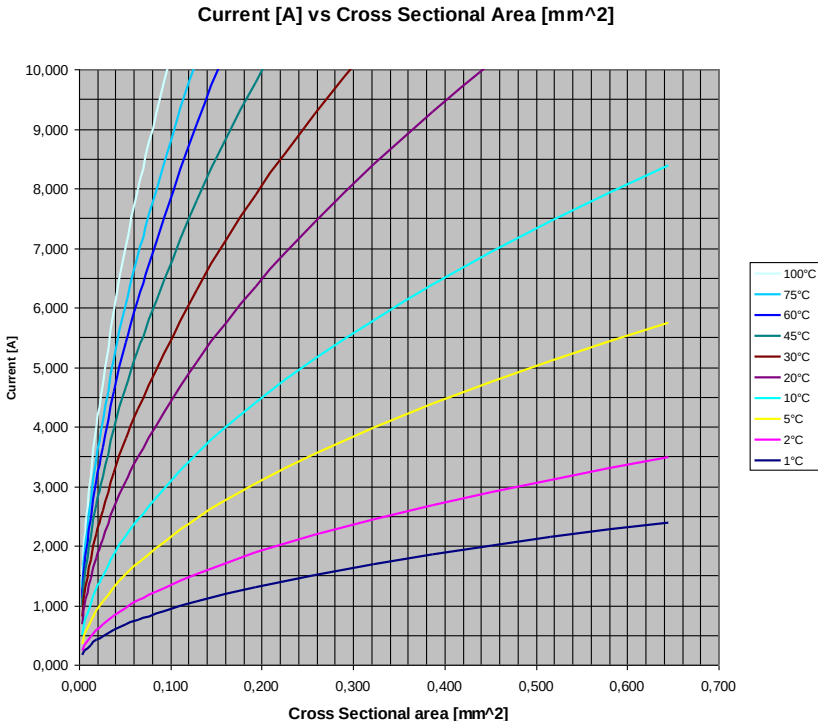


Figure D-5: IPC-2152: Current rating based on Figure D-2, range 0-10 A

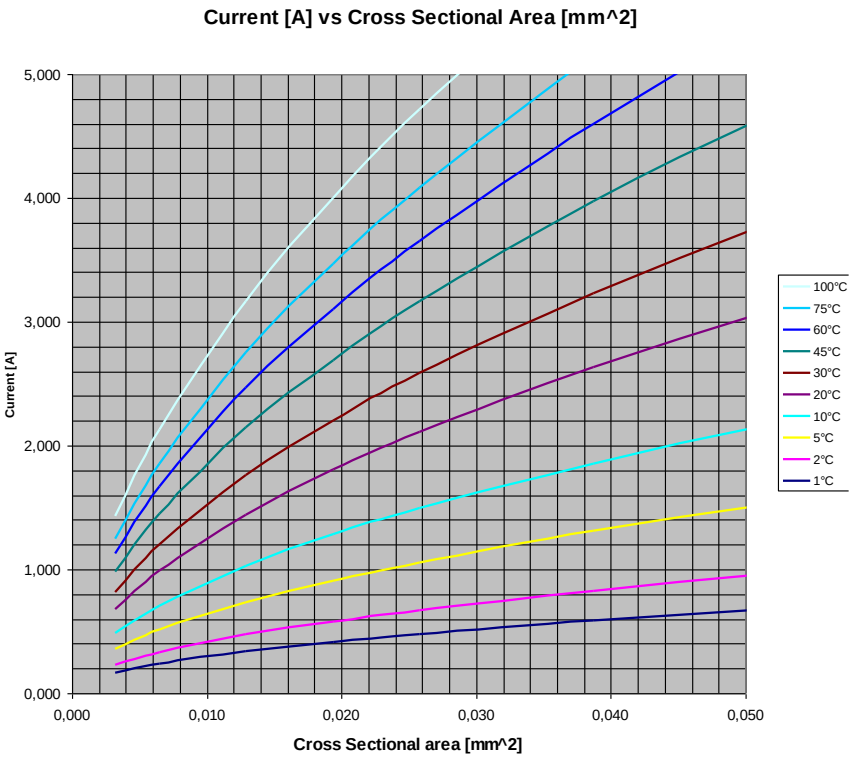


Figure D-6: IPC-2152: Current rating based on Figure D-2, range 0-5 A

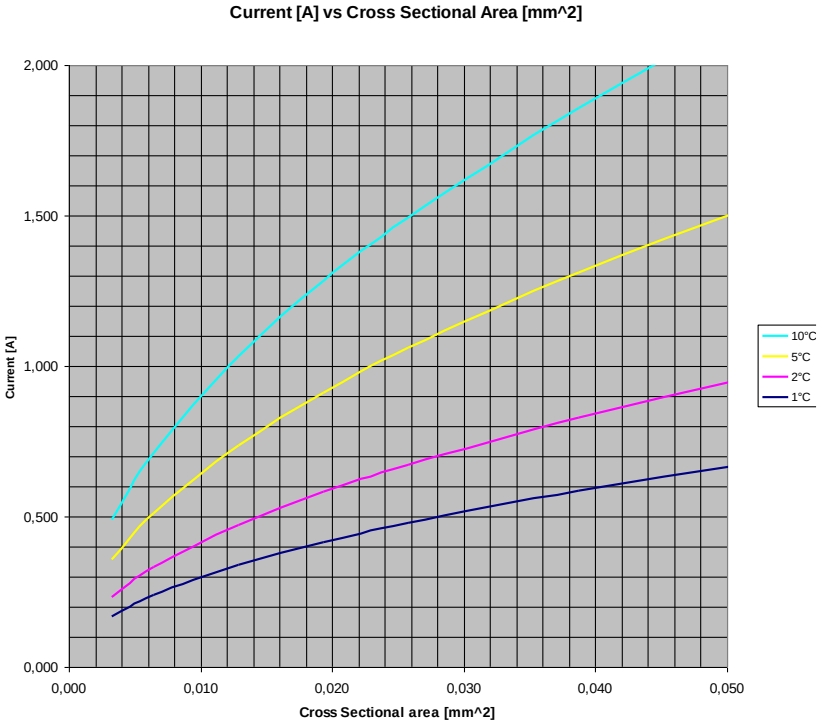


Figure D-7: IPC-2152: Current rating based on Figure D-2, range 0-2 A

D.3 Track current rating computation based on CNES/QFT/IN.0113

The CNES current rating computation is based on the thermal model correlated to experimental data. The values obtained for current carrying capacity are about 10% more conservative with reference to those of IPC-2152.

The model does not apply derating to take into account the complexity of the PCB.

The model presented in this clause is based on a curve fitting performed on the data given in the table "Tableau de quelques valeurs particulieres, Intensite=f(largeur, ΔT)" on page 10 of CNES/QFT/IN.0113".

a. The model is derived from experimental data ranging up to 8 A and up to 100°C temperature increment with respect to an initial PCB temperature of 25°C when not powered.

b. Current rating and cross sectional area are calculated as per the formula in clause D.1.2 with the following constants:

   1. k0= 0,0594
   2. k1= 0,4800
   3. m0= 0,5420
   4. m1= 0,0034

c. Example charts based on this model are shown in Figure D-8 to Figure D-13.

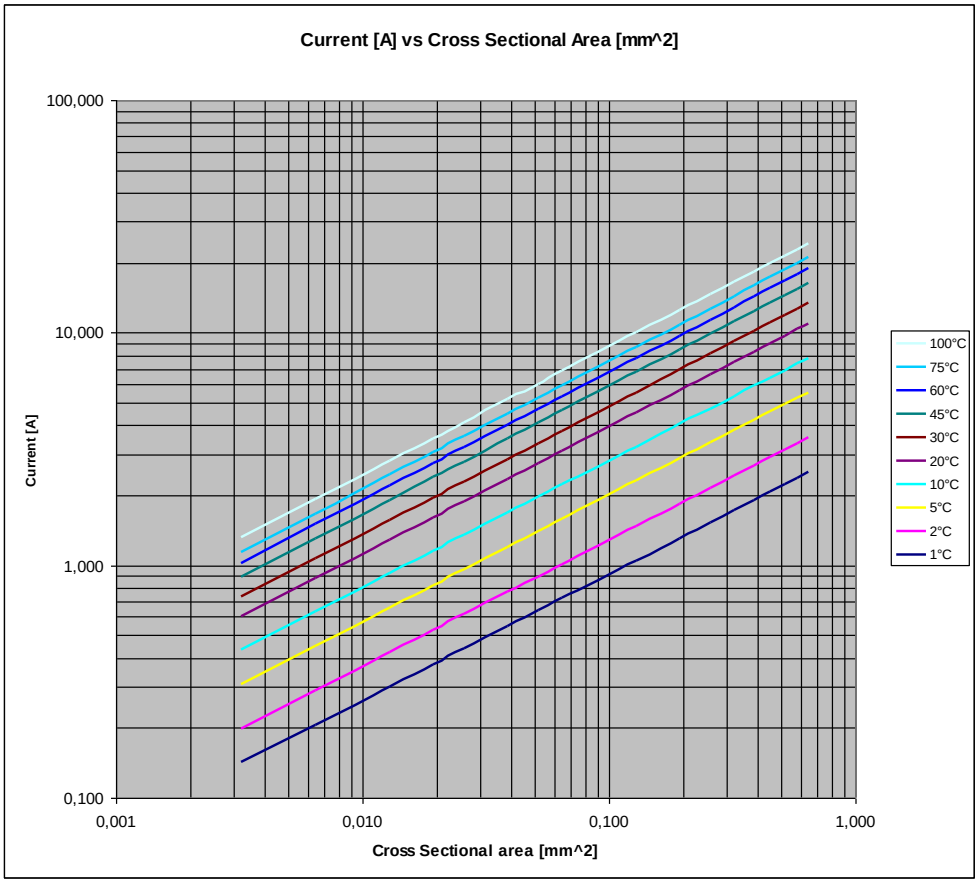


Figure D-8: CNES/QFT/IN.0113: Current rating [A] vs cross sectional area [mm²] in double log scale

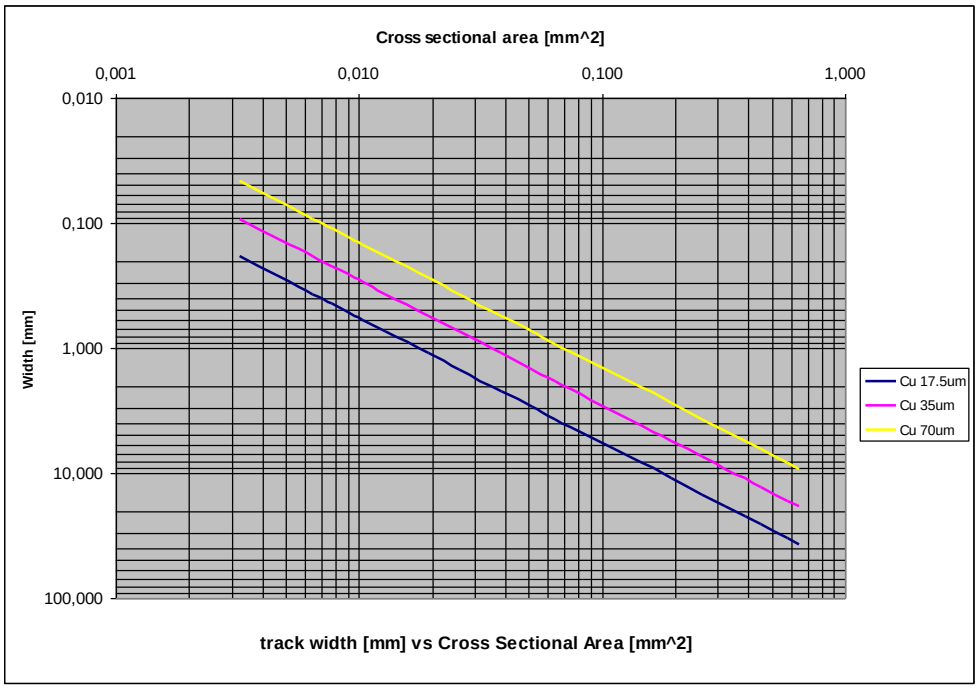


Figure D-9: CNES/QFT/IN.0113: Track width [mm] vs cross sectional area [mm²]

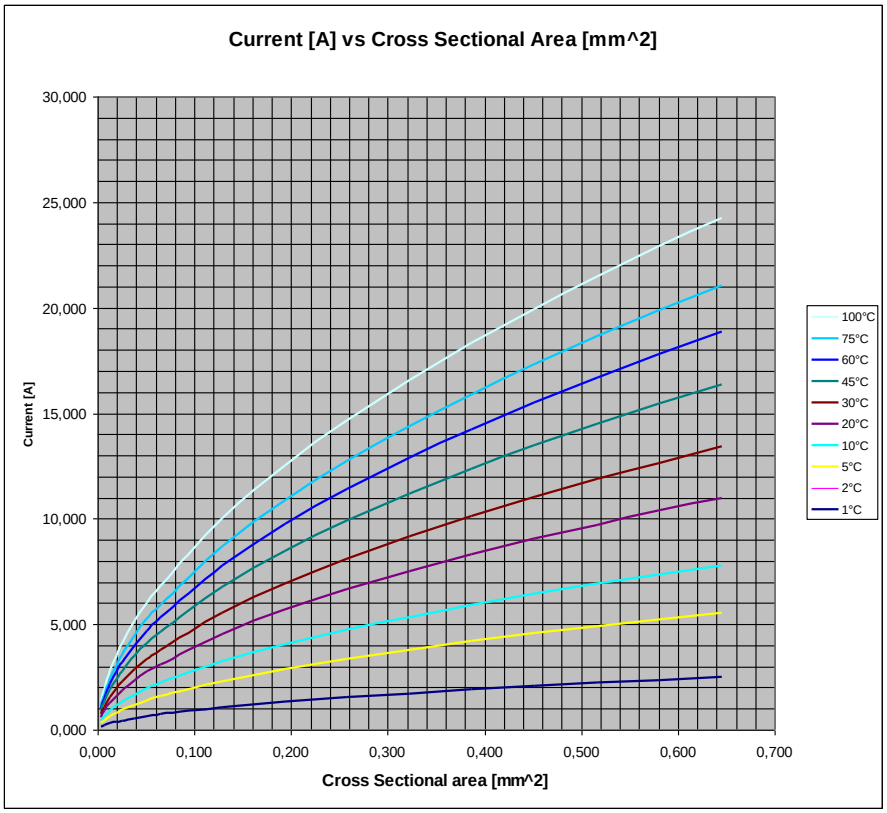


Figure D-10: CNES/QFT/IN.0113: Current rating based on Figure D-8, range 0-25 A

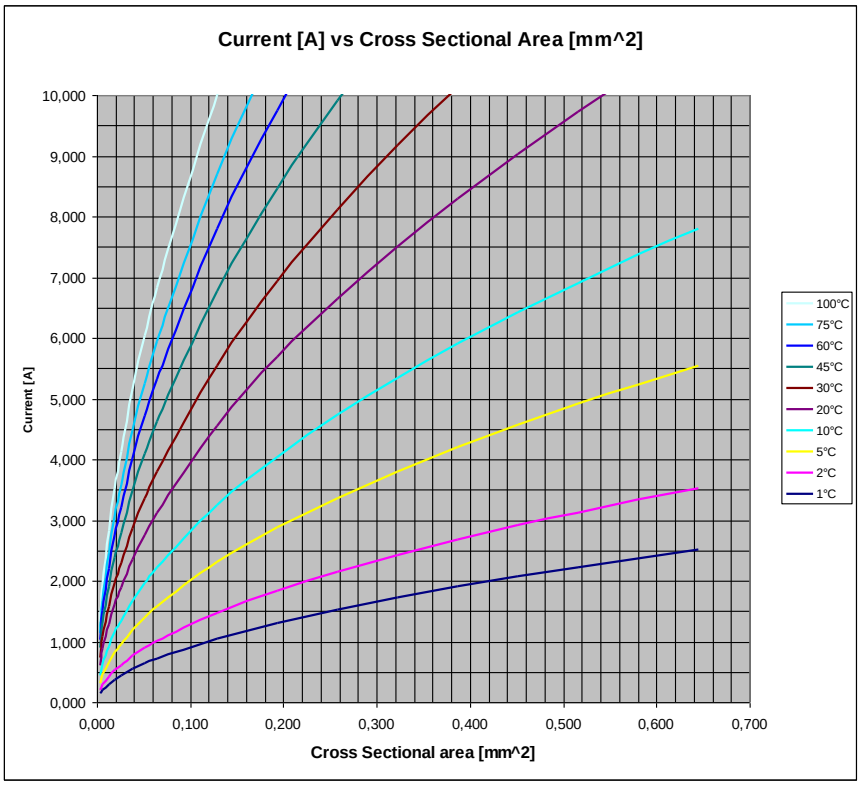


Figure D-11: CNES/QFT/IN.0113: Current rating based on Figure D-8, range 0-10 A

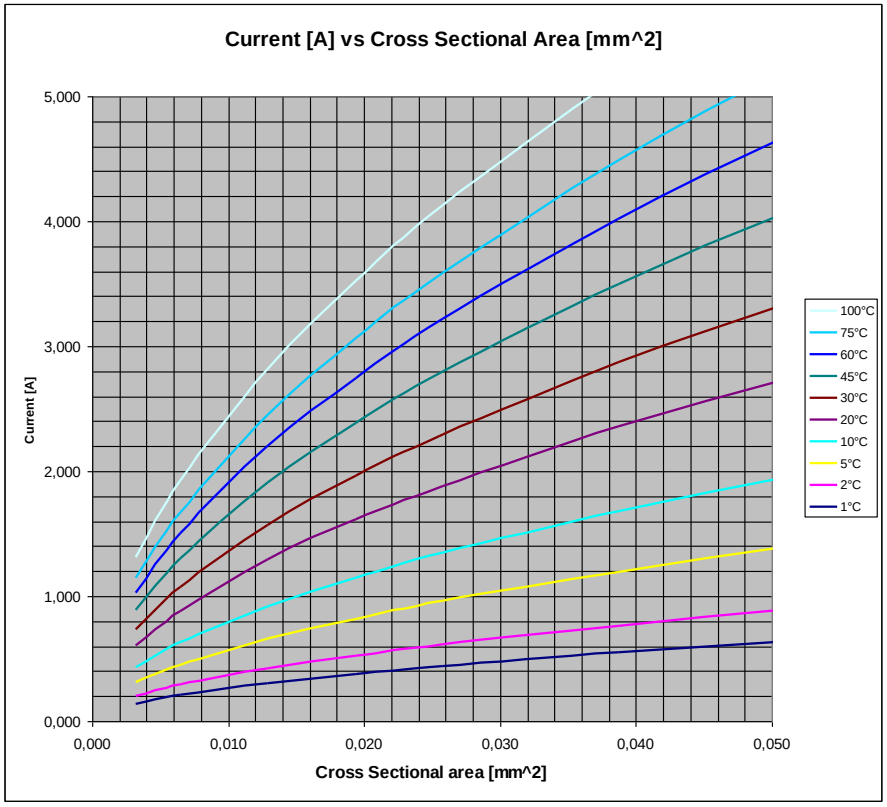


Figure D-12: CNES/QFT/IN.0113: Current rating based on Figure D-8, range 0-5 A

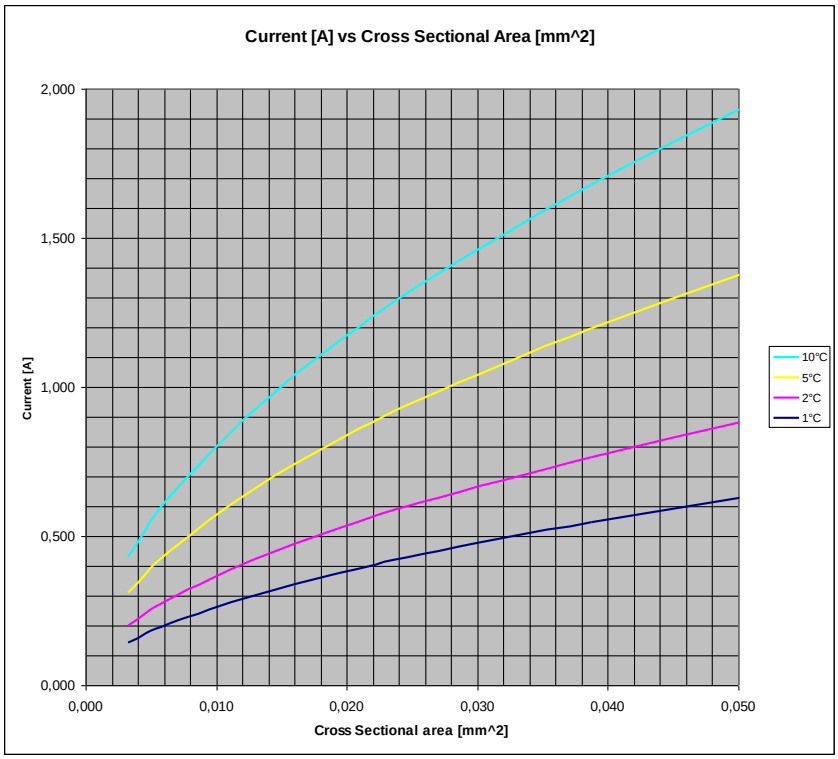


Figure D-13: CNES/QFT/IN.0113: Current rating based on Figure D-8, range 0-2 A

D.4 Track current rating computation based on IPC-2221A

The model presented in this clause is based on a curve fitting performed on figure C for internal conductors of Figure 6-4 of IPC-2221A.

IPC-2221A is the most conservative method of the three methods defined Annex D. Derating is not used in this model.

a. The current rating is calculated with the following conditions:

   1. I<0,7A for Trise 1 °C
   2. I<0,9A for Trise 2 °C
   3. I<1,0A for Trise 5 °C
   4. I<1,2A for Trise 10 °C

   Within these conditions the current rating is about 70% of the current rating calculated with IPC-2152.

b. Current rating and cross sectional area are calculated as per the formula in the clause D.1.2 with the following constants:

   1. k0 = 0,0240
   2. k1 = 0,4393
   3. m0 = 0,7252
   4. m1 = 0,0002

c. Example charts based on this model are shown in Figure D-14 to Figure D-19.

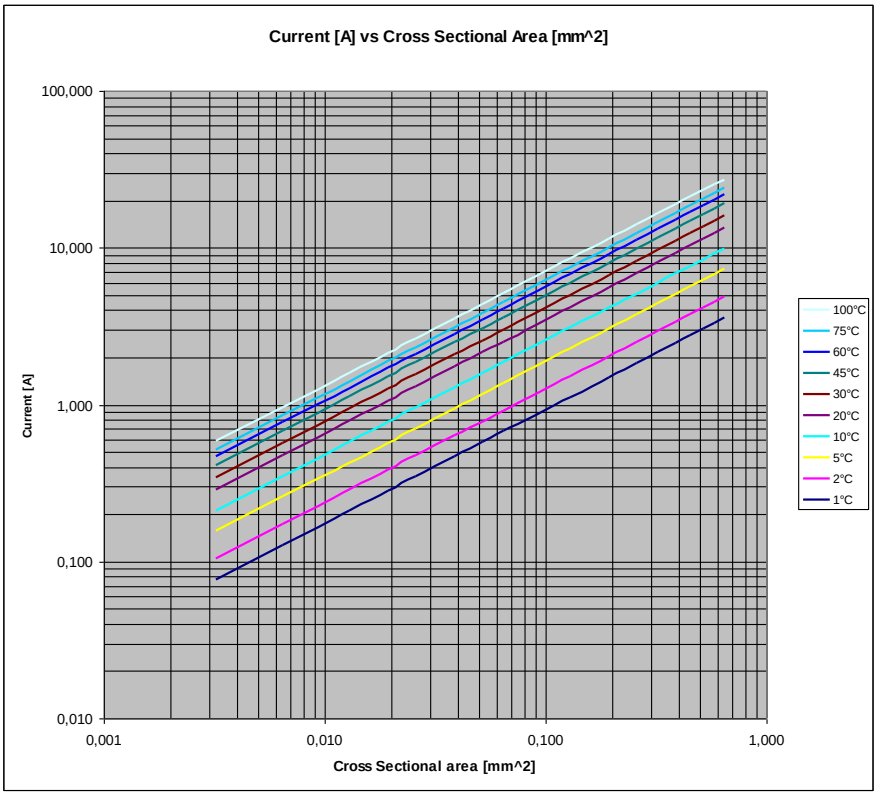


Figure D-14: IPC-2221A: Current rating [A] vs cross sectional area [mm²] in double log scale

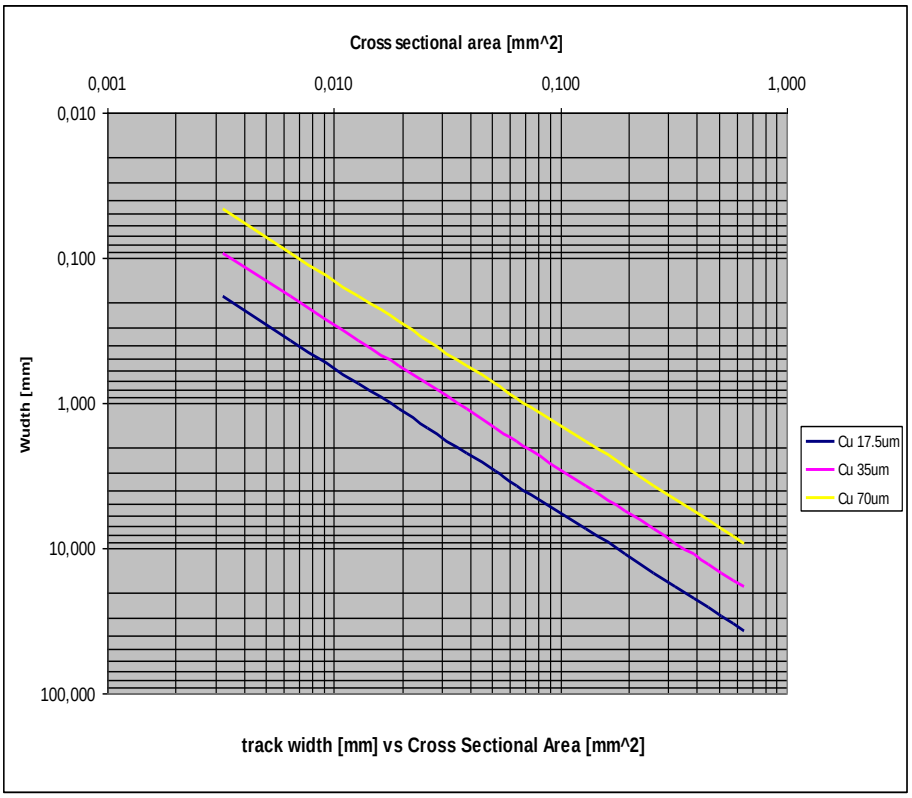


Figure D-15: IPC-2221A: Track width [mm] vs cross sectional area [mm²]

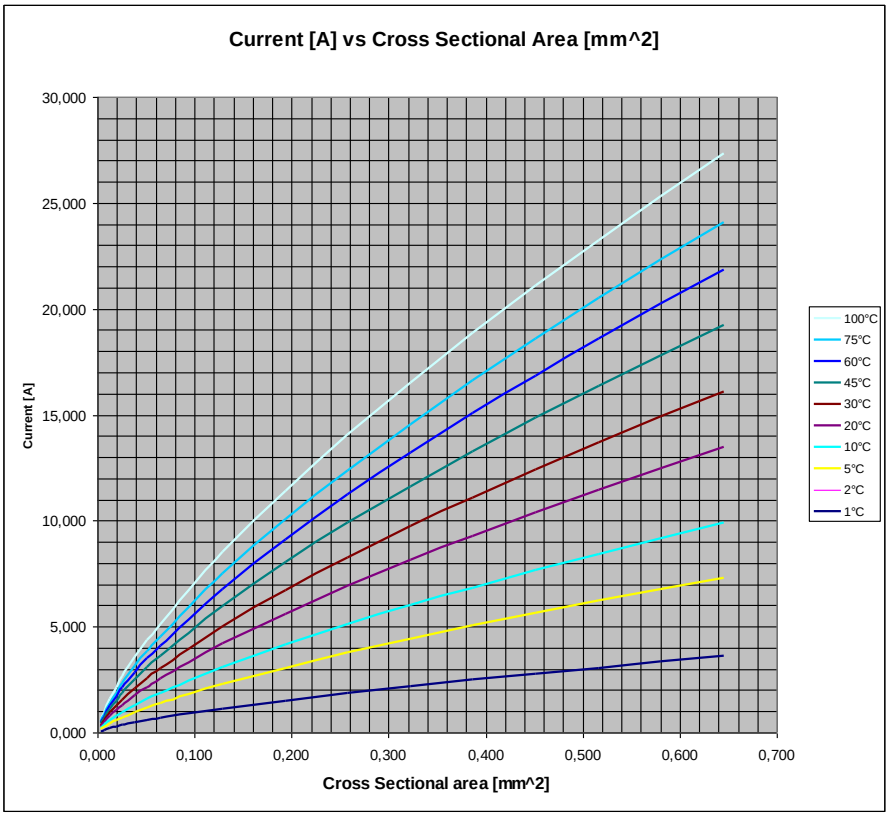


Figure D-16: IPC-2221A: Current rating based on Figure D-14, range 0-25 A

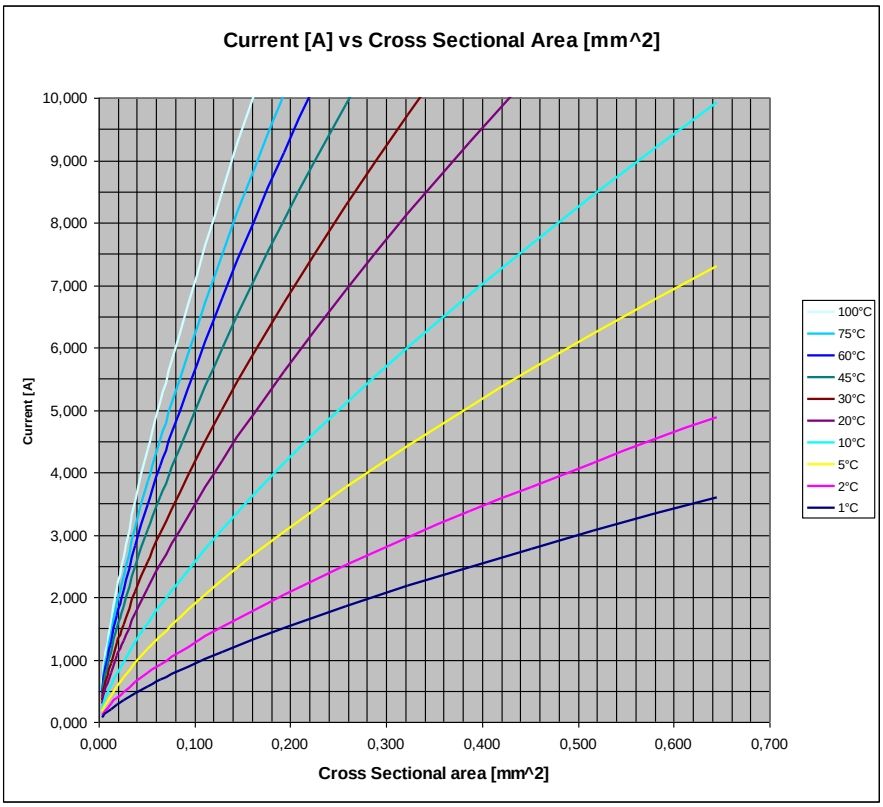


Figure D-17: IPC-2221A: Current rating based on Figure D-14, range 0-10 A

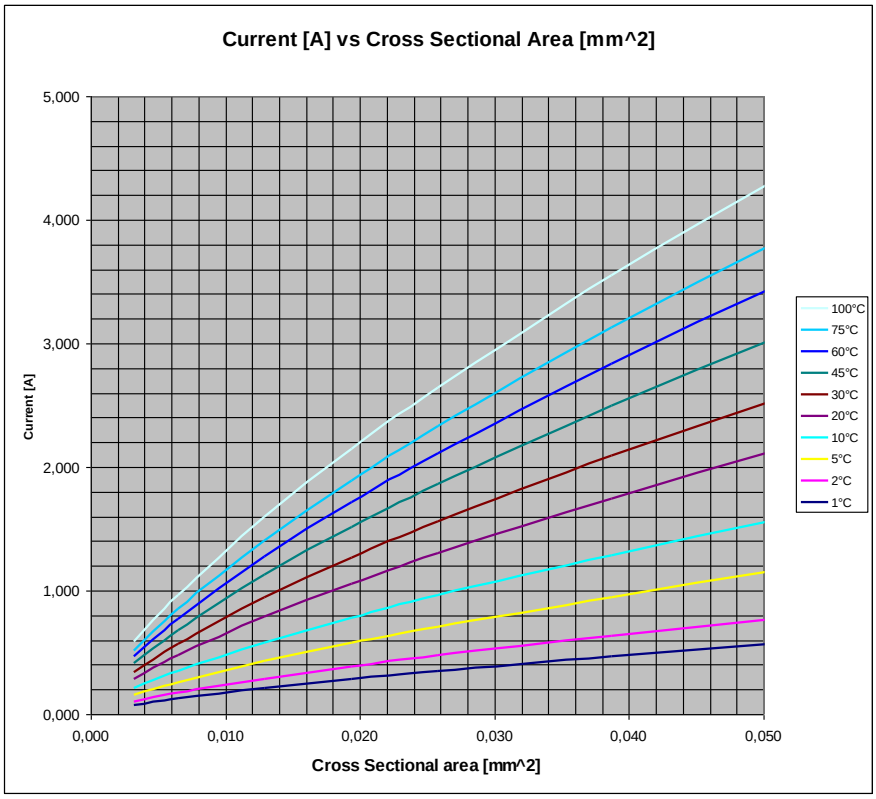


Figure D-18: IPC-2221A: Current rating based on Figure D-14, range 0-5 A

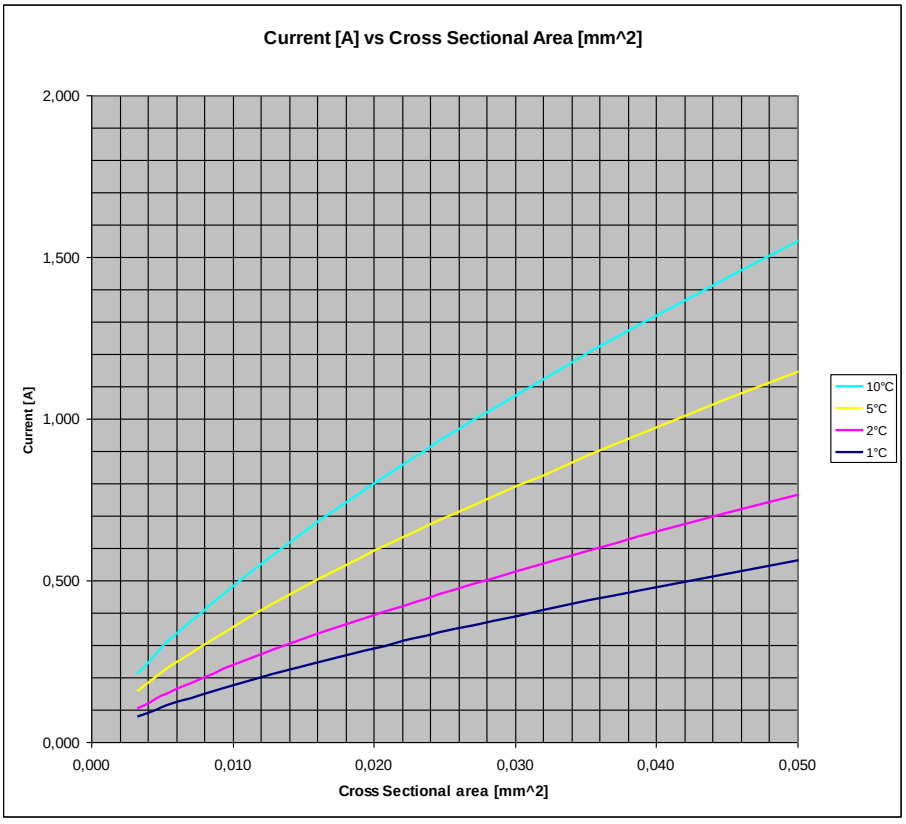


Figure D-19: IPC-2221A: Current rating based on Figure D-14, range 0-2 A

Annex E (informative) Example of calculation of PTH pad dimensions

Two examples of calculations of PTH pad dimensions are shown below. These calculations shown in Figure E-1 and Figure E-2 are specific for the PCB manufacturer as specified in the PID and depend on the complexity of the PCB designs.

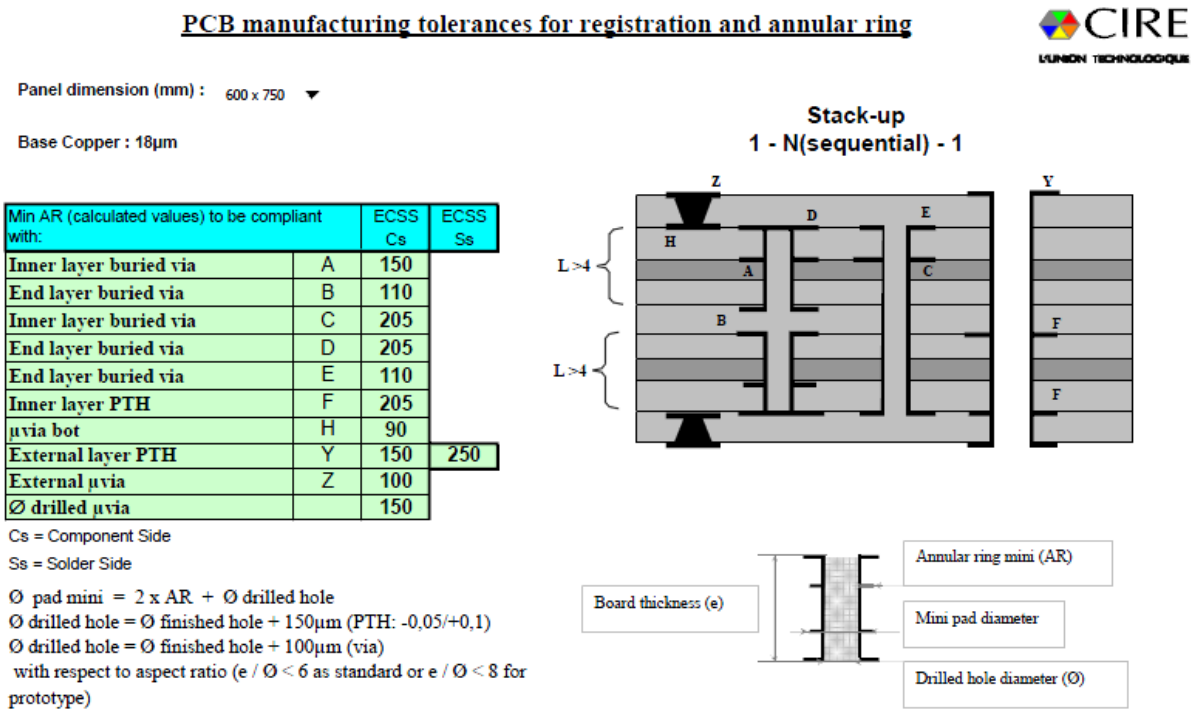


Figure E-1: PCB manufacturing tolerances for registration and annular ring for HDI PCB

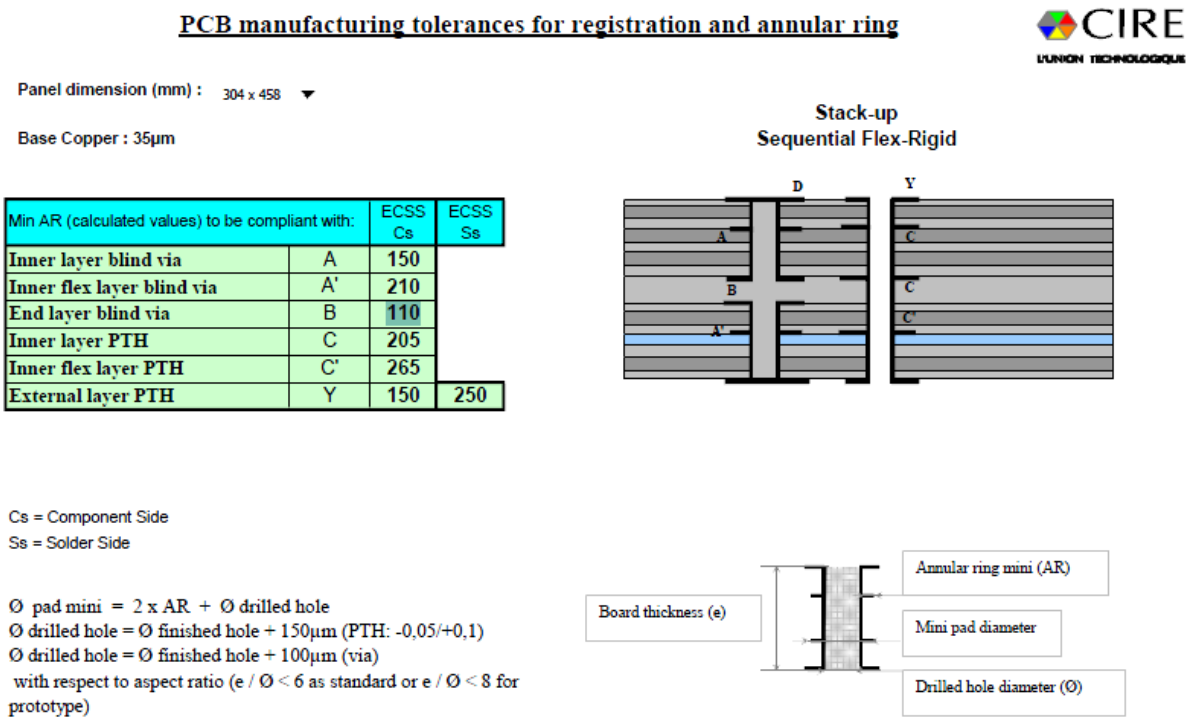


Figure E-2: PCB manufacturing tolerances for registration and annular ring for rigid-flex sequential PCB

Annex F (informative) Prevention of resin starvation and cracks

F.1 Prevention of resin cracks.

Under some conditions, cracks can develop in the laminate resin. They are more likely to appear:

a. In brittle resin types;

b. In locations with only resin and no reinforcement, such as openings in thick ground planes;

c. If the resin is mechanically stressed by drilling or routing.

The cause for the cracking can be mechanical impact or volume shrinkage during curing of the prepreg. Once a crack is formed, it can propagate into the laminate. The board manufacturing process can influence the formation of cracks. Design precautions to reduce the risk of crack formation include the following measures:

a. Avoid large volumes of resin without prepreg reinforcement.

NOTE Heat sinks often include large volumes of resin that can increase the risk of cracks. To avoid this, prepreg inserts in openings can be used.

b. Avoid low pressure areas due to opposite openings in superimposed copper layers.

c. Keep non-functional pads in planes.

d. Review the selection of material with PCB manufacturer.

NOTE Prepreg with filled resin can provide improved mechanical properties.

F.2 Prevention of resin starvation

Resin starvation is defined as a condition of insufficient resin to completely wet the glass reinforcement and fill the space between fibres. To reduce the risk for resin starvation the following can be done:

a. Allow sufficient prepreg thickness to fill the space between the copper pattern. High profile copper features throughout the PCB layers, such as a pad stack or superimposed tracks, can cause high pressure during lamination and can squeeze resin locally out of the prepreg if insufficient resin is available. The PCB manufacturer can implement additional prepreg between 70 µm copper layers compared to 35 µm copper layers.

Removal of non-functional pads can reduce the risk of resin starvation (see requirement7.5.2b.2).

b. Fill open areas in thick copper layers with a non-functional-copper pattern to reduce the amount of resin required for filling. This can also help improve the thickness uniformity of the board.

See IPC-2222A clause 9.1.4 which mentions resin starvation and cracks in a discussion of removal of non-functional pads.

Annex G (informative)
Example of MRR checklist

The following is an example of "MRR checklist" document.

Part 1, 2 and 3 to be completed by the procurement authority.

1. Procurement Traceability

PCB Manufacturer		Project and W.B.S number	
P/O No:		P/O Date	
FCSI Required		Model – EM; QM; EQM; PFM; FM; ~~FS~~	

2. Design Authority Declaration

Part No:*		Issue and revision*	
Part title:*		Equipment*	
Technical Requirement*			
Is this a new or a recurring design*			
Has this part been previously procured under a different part number?* ***If so please provide previous part number***			
If recurring please define all changes made to the data set since the last purchase or state none*			
Is the design fully compliant with ECSS-Q-ST-70-12C as applicable?			
If the design is not compliant to the applicable design standard (ECSS-Q-ST-70-12C) please list all deviations*			
Design to confirm that there is no floating copper in the design i.e. not attached to potential or ground when assembled.*			
Has method and position of identification marking been defined?*			
Is the design subject to double insulation requirements?*			
If subject to double insulation requirements has IPC 4101 appendix A compliant material been specified?* ***If no please provide technical justification***			

3. Technical Authority and Quality Review

For recurring product please reference **ALL Occurrence reports** and **NCRs** raised against previous procurements of this article/reference or state none*	
For recurring product please reference **ALL Concession requests** associated with previous procurements of this article/reference or state none*	
IST required?*	YES /NO
Are there special conditions for IST? If yes, pls specify.*	DELAM YES / NO Preconditioning ..... cycles @ ..... °C Standard IST ..... cycles @ ..... °C followed by:- Micro-via IST ..... cycles @ ..... °C
Has the IST coupon design been generated (in order of preference) - by PWB Corp upon review of the gerber data of the PCB, - by PWB Corp using a coupon worksheet, - by downloading a coupon from a database	
Is double visual inspection to be applied?* ***For complex PCBs with multiple fine pitch components only***	YES/NO
FAI Required?* ***FAI on a sample PCB is performed when specified by the procurement authority.***	YES/NO
Additional care or review points identified by Technical Authority	

4. Printed Circuit Board Manufacturer Declaration

Parts 4 to 10 to be completed by the PCB manufacturer

Supplier W/O No:		W/O Date	
If this is a recurring design please define all changes made to tooling or processing since the last purchase or state “none”.			

5. Manufacturer’s PID (Process Identification Document)

Approved PID Reference including issue and revision	
Deviations to the Approved PID List all modifications changes and non conformances relative to the approved PID or state “none”.	

6. Contract Review

Please confirm contract review has taken place and reference controlling procedure(s) used	
Please list any anomalies or deviations arising from the contract review or state none	

7. Design

Have any changes to the provided data been requested following design rule checking (DRC)	
Is the requested design fully in line with the qualified PID ***The PCB manufacturer reviews the PCB definition dossier including Review Items for compliance with the PID.***	

Please list all changes and provide references below

Reference of requesting e-mail, date, from, to.	Reference of procurement authority agreement, date, from, to.	Comments	Actions arising

Have all non functional pads been kept? If no, is the removal compliant to ECSS-Q-ST-70-12C	
Has coupon sample data been included in the data pack provided	
In the case superposed blind vias are present in the PCB, have they included in the design of the coupon B_n?	
Has data for any coupons designed by the PCB manufacturer been provided to the procurement authority for review during MRR?	
Has IST coupon sample data been included in the data pack provided	
Does the layer count and designation and the drilled hole sizes of the IST coupon match the construction of the PCB?	
Are all of the applicable via types and sizes included in the IST coupon(s)?	
Standard coupon (A/B) Has the maximum component hole size or most frequently used component hole size been included in the coupon?	
Is teardrop reinforcement of pads used within the PCB? ***If so, confirm that teardrop reinforcement has not been included in the coupon to ensure adequate verification of worst-case annular ring.***	
Has a rigid flex coupon been provided with the data	
Does the design require a custom coupon or coupons to verify controlled impedance? **If yes, how many?**	

Has the position and quantity of coupon sample(s) been agreed with the procurement authority?		
In case there are multiple PCBs per panel, has an IST coupon containing the highest risk features been located as close as practical to the centre of the panel, with another situated on the edge?		
Do outer layer nets and boards with mixed surface finishes conform with the minimum insulation distance as defined in the manufacturer's PID?		
Has the diameter of internal pads been reduced through use of teardrop reinforcement? ***If so record as a Review Item.***		
Does the design contain vias with an aspect ratio > 7? If so		
	Is the the aspect ratio is ≤ 10? ***If yes record as an additional Review Item.***	
	Are the vias used within the footprint of an AAD with a pitch of ≤1mm? ***If yes record as a Review Item.***	
	Are the high aspect ratio vias included in the coupon to validate plating on the coupon?	
PCB Manufacturer to confirm that no additional copper has been added within the active PCB profile without connection to potential or ground. ***If ANY copper has been added within the PCB profile please provide reference giving authorisation from procurement authority***		

8. Technical Review

In case there is the risk of deviation to the requirements of the purchase order or a risk of an identified undesirable artefact occurring, this should be recorded in section "Risks identified"

Please advise the base laminate and pre-preg references to be used in fulfilment of this order.	
In case of HDI technology using single ply prepreg or double insulation requirements, confirm the base materials for rigid laminates and prepreg are in conformance with IPC-4101E Appendix A.	
Is there an extended lead time in procuring these materials? ***If so please advise lead time***	
Has this configuration and combination of materials been utilised previously?	
Is the stack-up of materials symmetrical for each pressing cycle?	
How many press cycles lamination – drilling cycles will be required in the manufacture of this design?	
Are there two plies of glass present between every conductive layer – laminate and pre-preg?	_____

Where pre-preg is intended to be used to backfill vias, is the resin content and board geometry suitable to support this?	
Does the pattern distribution for NiAu plated features support even and controlled distribution of the plating across the panel?	
Does the copper distribution on plated layers support even and controlled distribution of the plating across the surface of the panel? ***For sequentially laminated product this includes sub-layer plating operations***	
FLEX RIGID	
For flex rigid only, is the process open or closed window?	
How many flexible laminate layers are included in the design?	
Is copper foil of ≥ 70µm utilised on flexible layers or in contact with low flow pre-preg? ***If yes record as a review item***	
Is the value for coverlay extending into the rigid portion of the PCB in line with the qualified PID?	
Does the design feature multiple flex laminates joined together utilising bondply? ***If yes confirm that the ends of the bondply and the coverlay are offset by ≥ 1mm within the rigid section and are in line with the qualified PID.***	
Manufacturer to confirm that coverlay cannot overlap any aspect of an internal pad in the rigid section of the PCB.	
Is the rigid-flex PCB delivered in a support frame? ***If no, manufacturer to confirm how the PCB is packaged for delivery to prevent damage during transit***	

9. Risks Identified

Have any risks to the manufacture of this product been identified ? ***If no risks are identified, a default level of 1 shall be considered***		
Risks identified	Risk Rating (1 Low, 5 High)	Risk Parameters requiring control

Risk level 1: No perceived risk, manufacturer accepts full liability for remake in case of batch rejection.

Risk level 2: Low level of perceived risk, easily controlled with standard processes, manufacturer accepts full liability for remake in case of batch rejection.

Risk level 3: Medium level risk, some challenging elements, expected to be fully controlled with standard processes and loading, manufacturer accepts full liability for remake in case of batch rejection.

Risk level 4: Upper medium risk, challenging elements with significant concerns regarding ability to meet specification requirements, procurement authority accepts full liability for remake in case of risk level 4 elements being realised.

Risk level 5: High risk, multiple challenging elements, expectation that specification requirements cannot be met, procurement authority accepts full liability or remake in case of risk level 5 elements being realised.

10. PCB Manufacturer Completing Signature

Position	Print Name; Sign and Date

11. Procurement authority review

Parts 11 to 13 to be completed by the procurement authority

Is the procurement authority in agreement with the risks identified and the rating applied by the manufacturer	
If no, provide details of dis-agreement	
ECSS requirements applicable to project Is the PCB technology covered by a valid ECSS qualification? **Yes:** record PID reference, low to intermediate risk **No:** initiate requirement for group 6 test plan, medium risk	
Have any additional risks been identified by the procurement authority as a result of this review.	
If yes give details	

12. Procurement Authority Recommendations

Recommendation	Print Name, Sign and Date
Low to intermediate levels of risk 1 – 2. Manufacture may continue without project counter-signature	
Medium levels of risk 3 – 4. Risks to be entered in project risk register. Project manager and project PA manager responsible countersignature to confirm acceptance and recording of risk before manufacture may commence.	
High risk 5. Continuation against recommendation of procurement authority. To be subject to internal review with inclusion in project risk register. Project manager and project PA manager responsible countersignature to confirm acceptance and recording of risk before manufacture may commence.	

13. Procurement authority authorising signatures

Entity	Print Name, Sign and Date
technical authority	
Optional project PA manager (medium and high risk only)	
Optional project manager (medium and high risk only)	

Bibliography

ECSS-S-ST-00	ECSS system – Description, implementation and general requirements
ECSS-Q-ST-70-28	Space product assurance - Repair and modification of printed circuits board assemblies for space use
ASTM-B386-03, 2011	Standard Specification for Molybdenum and Molybdenum Alloy Plate, Sheet, Strip, and Foil
IPC-2141, Mar 2004	Design Guide for High Speed Controlled Impedance Circuit Boards
IPC-2221A, May 2003	Generic standard on printed board design
IPC-2221B, Nov 2012	Generic standard on printed board design
IPC-2222A, Dec 2010	Sectional design standard for rigid organic printed boards
IPC-2223C, Nov 2011	Sectional design standard for flexible printed boards
IPC-2226, Apr 2003	Sectional design standard for high density interconnect boards
IPC-2251, Nov 2003	Design guide for the packaging of high speed electronic
IPC-2315, Jun 2000	Design guide for high density interconnects (HDI) and microvias
IPC-4104, May 1999	Specification for high density interconnect (HDI) and microvias materials
IPC-4121, Jan 2000	Guidelines for selecting core constructions for multilayer printed wiring board applications
IPC-4202A, Apr 2010	Flexible base dielectrics for use in flexible printed circuitry
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IPC-7351B, Jun 2010	Land pattern and calculator
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RNC-CNES-Q-ST-70-101, version 8, Apr 2009	Spécifications de conception des cartes imprimées
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NOTE See also Clause 2 for referenced normative IPC standards.