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Space product assurance

Design, selection, procurement and use of die form monolithic microwave integrated circuits (MMICs)

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Foreword

This Standard is one of the series of ECSS Standards intended to be applied together for the management, engineering and product assurance in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards.

Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

The formulation of this Standard takes into account the existing ISO 9000 family of documents.

This Standard has been prepared by the ECSS-Q-60-12 Working Group, reviewed by the ECSS Product Assurance Panel and approved by the ECSS Steering Board.

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Introduction

This Standard provides guidelines for the design, selection, procurement and use of III-V monolithic microwave integrated circuits (MMICs) for space equipment.

It defines the design activity for the technical (methodology, phases to be followed) and quality (quality assurance, design review) aspects, and, the selection and procurement rules for these components taking into account whether or not the processes have been validated.

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Scope

This Standard applies to all types of MMIC (monolithic microwave integrated circuit) based on III-V compound materials for RF applications (i.e. frequency range ≥ 1 GHz). The requirements for the procurement of components in die form are defined.

It is not within the scope of this Standard to address packaged MMICs and discrete microwave components, these are dealt with in the relevant ESCC specification (ESCC 9010 and ESCC 5010).

When viewed from the perspective of a specific project context, the requirements defined in this Standard should be tailored to match the genuine requirements of a particular profile and circumstances of a project.

NOTE Tailoring is a process by which individual requirements or specifications, standards and related documents are evaluated and made applicable to a specific project, by selection and, in some exceptional cases, modification of existing or addition of new requirements.

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Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

ECSS-P-001	ECSS — Glossary of terms
ECSS-Q-30-11	Space product assurance — Derating - EEE components
ECSS-Q-60	Space product assurance - Electrical, electronic and electromechanical (EEE) components
ECSS-Q-60-01	Space product assurance - European preferred parts list (EPPL) and its management
ECSS-Q-60-05	Space product assurance — Generic procurement requirements for hybrid microcircuits
MIL-STD-883	Tests methods and procedures for microelectronics
ESCC 20100	Requirements for qualification of standard electronic components for space application
ESCC 20600	Preservation, packaging and despatch of ESCC electronic components
ESCC 24600	Minimum quality management system requirements
ESCC 2049010	Internal visual inspection of monolithic microwave devices
ESCC 2269010	Evaluation test programme for MMICs
ESCC 2439010	Requirements for capability approval of MMICs
ESCC 9010	Generic specification for MMICs

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Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purpose of this document, the terms and definitions given in ECSS-P-001 and the following apply.

3.1.1
batch lot
wafers from the same basic raw materials processed as a single set in the manufacturing sequence (diffusion, metalization and passivation process) in a limited and controlled period of time

NOTE A unique identifier or code is assigned to a batch lot and to each wafer for processing traceability purposes.

3.1.2
design rules check
control procedure for verifying that design rules have been satisfied

NOTE 1 Design rules are generally issued by the vendor.

NOTE 2 DRC is performed using software.

3.1.3
designer
organization responsible for the design of the MMICs

3.1.4
die lot
all dies coming from a single wafer lot

3.1.5
electrical rule check
control procedure for verifying that the electrical rules have been satisfied

NOTE Electrical rules are generally issued by the vendor.

3.1.6
evaluated process
mature technology that has been successfully submitted to a set of electrical and environmental testing to demonstrate performance and reliability limits

NOTE 1 ECSS-Q-60-01 contains a list of evaluated processes.

NOTE 2 The ESCC 2269010 specification defines the requirements for the evaluation.

3.1.7
manufacturer
foundry responsible for the manufacturing of the MMICs

3.1.8
process control monitor
test vehicle used by the vendor to assess the stability of the manufacturing process by means of controls conducted during a wafer production cycle

NOTE The PCM is repeated a number of times (depending on the vendors) on each wafer lot. The measurements taken during the PCM are used to accept or reject the wafer according to the relevant DC and RF criteria defined in the design manual.

3.1.9
process identification document
document that defines the approved technology domain, the reference of approval status, and one that freezes the configuration of the manufacturing line and the approved domain

[ECSS-Q-60-05]

3.1.10
production lot
device types manufactured from the same basic raw materials on the same production line, processed under the same manufacturing techniques and controls using the same type of equipment

NOTE A production lot may be composed of one or many batch lots.

3.1.11
qualified process
process that has been successfully submitted to a formal qualification testing

NOTE The ESCC 20100 specification defines the requirements for the qualification.

3.1.12
reticule
group of circuit layouts (MMIC, TCV, DEC, PCM) defined by design at the mask level, for duplication over the entire wafer during the MMIC manufacturing

3.1.13
statistical process control
tool to aid the vendor and user to control the quality and the stability of the technological process

NOTE SPC is implemented by measuring key parameters during the different manufacturing steps and their analysis using appropriate methods.

3.1.14
tile
see “reticule”

3.1.15
user
procurer of the MMICs that is responsible for their integration

EXAMPLE MMICs are integrated by users into, for example, modules, hybrids, piece of equipment.

3.1.16
validated design
design that is successfully submitted to application approval testing and an MMIC user LAT test

3.1.17
validated process
process that is evaluated or qualified

3.1.18
wafer lot
wafers manufactured from one or more batch lots

NOTE Depending on the maturity of the process a wafer lot is defined as follows:

- Case 1 (non-evaluated or qualified process): a wafer lot is a single wafer.
- Case 2 (evaluated or qualified process and new MMIC design): a wafer lot is one batch lot.
- Case 3 (mature process and recurrent MMIC design): a wafer lot is considered to be a production lot of 4 batches manufactured within a 3 month period.

3.1.19
vendor
see "manufacturer"

3.2 Abbreviated terms

The following abbreviated terms are defined and used within this document:

Abbreviation	Meaning
AQL	acceptance quality level
CTA	circuit type approval
DEC	dynamic evaluation circuit
DRC	design rules check
ERC	electrical rule check
HTRB	high-temperature reverse bias
LAT	lot acceptance test
LTRB	low-temperature reverse bias
MMIC	monolithic microwave integrated circuit
PAD	part approval document
PCM	process control monitor
PID	process identification document
RGA	residual gas analysis
SAM	scanning acoustic microscopy
SEM	scanning electron microscope
SEU	single event upset
SPC	statistical process control
TCV	technological characterization vehicle
WAT	wafer acceptance testing

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General requirements

4.1 General

This Clause defines the requirements for die MMIC procurement. It completes the user LAT requirements for MMIC die lot procurement as defined in ECSS-Q-60-05.

The responsibilities of the participants (e.g. designer, vendor or end-user) are given from the prototype phase to the delivery of the dies for flight model hybrid manufacturing.

4.2 Flight model MMIC dies lots procurement

The steps involved in procuring MMICs for Space applications are as follows:

a. Process selection (Clause 5).

b. Allocation of responsibilities (Clause 6).

c. MMIC design (Clause 7).

d. Application approval (Clause 8).

e. Procurement and LAT specifications (Clause 9).

f. Die form procurement sequences (Clause 10).

Requirements for the qualification and procurement of MMIC packaged devices are given in ESCC 9010.

4.3 Minimum quality requirements

The minimum requirements for processing, production control and clean room conditions are defined in ESCC 24600.

The vendor shall implement and maintain a product quality programme, to ensure that reliability and quality is maintained throughout all the phases of manufacturing and testing in conformance with the requirements in ECSS–Q-60.

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Selection

5.1 General

During the selection of the manufacturing process by the user, components are assessed for their conformance to the requirements on reliability, application and environmental resistance as defined for the project.

a. The selection of a foundry shall take into account the maturity of the technology, the validation status and the qualification domain as defined in ESCC 2439010.

b. The MMIC design shall be analysed and validated in terms of application domain compared to the qualification domain and space application requirements.

NOTE The qualification domain is documented in terms of the following boundaries with respect to any potential failure mode identified on the process:

- The physical design and procedures that are closely related to the manufacturing process (no major process change identified since the evaluation testing).
- The electrical design in term of extreme limits (thermal, DC and RF parameters).
- Function (e.g. oscillator, gain block), and application (e.g. small signal, pulsed, high drive).
- The performances, the reliability figures, and the environmental resistance.

5.2 Process selection

a. The selection of the foundry, and the manufacturing process, shall be justified by the user, and approved by the customer.

b. The agreement shall be based on the specific application for which the MMIC is designed and on further considerations such as:

- The maturity of the process (e.g. large volume production or experimental technology).
- The adequacy of the application to the electrical foundry manual. In particular, as a minimum, the following items shall be considered:
  - Equivalent circuits based on measurement results for all passive elements, including lumped and distributed components (e.g. transmission lines and discontinuities), in a format compatible for use with standard circuit simulators.
  - Small signal (at various bias points) and large signal models of active components (e.g. transistors but also Schottky and varactor diodes) based on measurement results, in a format compatible for use with standard circuit simulators.
  - Availability of standard components (e.g. Lange couplers).
  - Layout libraries, in a format compatible for use with standard circuit simulators.
  - Thermal, reliability, process variation design parameters.
  - Space evaluation or qualification status including the results of reliability evaluations performed by the foundry.

c. A foundry manual for each process used, shall be delivered to the customer (provided the current issue is not already available) prior to the design phase.

d. The MMIC specifications (satisfying the overall equipment requirements) shall be established within the technical limits of the MMIC process used, and be finalised following an iterative process.

5.3 Models, and design tools

a. Only approved models (fully experimentally verified and included in the foundry manual) and design tools shall be used to design all the passive and active (linear and non-linear) elements.

b. Any non-standard models and design tools shall be justified, and approved by the customer.

6
Responsibilities

There are two modes for developing and procuring MMICs:

- "Foundry" mode: the user designs the MMIC and is entirely responsible for the design, and the vendor only guarantees the technology.
- "Catalogue" mode: the vendor designs the MMIC and is entirely responsible for both the design and the technology, except for issues related to incompatibility between the MMIC and the environment in the user application.

Table 1 summarizes the responsibilities of the vendor and the user.

Table 1: User and vendor responsibilities for the "foundry" and "catalogue" modes

Description	Reference	Responsibility	
		Vendor	**User**
Process selection	Clause 5	X	X
Design model validated and design tasks conducted	7.2		X
Design reviews	7.3	X	X
Procurement specification			
– for MMIC chip procurement under manufacturer and user shared responsibility	7.3.14	X	
– for LAT under user responsibility),	Clause 9		X
Application approval	Clause 8 and 10.4.5		X
Procurement activity including:	Clause 10		
– wafer screening and WAT	10.2.4	X	
– dies incoming control	10.3		X
– LAT	10.4.2 to 10.4.4		X
– DPA	10.4.6		X
– Failure analysis	10.5		X

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7

User MMIC design

7.1 Principles of user MMIC design

7.1.1 General

In this Clause the steps in the design phases and the responsibilities of the designer in the development of the prototype MMICs are defined.

This Clause does not apply to catalogue MMICs designed by the vendor and for which the vendor guarantees the microwave performances.

a. The synergies between the specific application for which the MMIC is designed and other application areas (e.g. commercial, professional, military applications) shall be investigated for possible utilization.

b. If the contractor is developing, or has already developed, for another application, an MMIC having a similar functionality to that required by the customer, this MMIC can be considered as a starting point for the new design.

7.1.2 Number of design iterations

A design iteration consists of circuit development, simulation, fabrication and measurement.

a. The decision to proceed with a second design and manufacturing iteration (redesign) shall be made, for each MMIC, based on the conformance of the electrical design specification and the electrical measurements of the first iteration.

b. Additional iterations shall be carried out until sufficient margins can be demonstrated.

7.1.3 Design trade-offs

A design trade-off shall be performed including, as a minimum, the following:

- circuit principles and heritage circuit topology and dependability;
- gain and compression distribution inside the circuit;
- overall electrical performance;
- testability;

- radiation;
- assembly;
- integration;
- cost effectiveness of the packaging.

7.2 Design tasks

7.2.1 Electrical design specification

a. Prior to any design, the user shall develop an electrical design specification of the electrical performances for the application.

b. This specification shall contain, as a minimum, the following:

  - electrical performances and application,
  - die dimension,
  - in and out interfaces.

7.2.2 Design variations

a. Several design variations for circuit architecture shall be implemented when the critical characteristics of the circuit are such that multiple variations on a design iteration maximise the probability of first-pass success.

b. The differences between the variations should be such that the probability of success of at least one of the variations is maximized.

c. Test structures of the most sensitive and critical passive and active circuit elements or sub-parts may be included in the design iteration to increase the diagnostic capabilities.

7.2.3 Parasitic effects

a. Parasitic effects shall be considered in all the designs and simulated with appropriate (e.g. electromagnetic) design tools.

EXAMPLE Examples include the effect of transmission line discontinuities (especially for unusual geometry and for those elements having a very critical influence on overall performance), on-die coupling, interconnections (e.g. bonding wires, external capacitors, impedance of interconnected circuits), assembly, and packaging.

b. The simulation may be complemented with experimental data from circuits having a similar layout and characteristics.

c. Additionally, if the confidence in a selected structure or component simulation is not sufficient, measures shall be taken to avoid this structure in the design, whenever possible, or the design modified to reduce the criticality of this structure.

7.2.4 Transient simulation

a. Transient simulations shall be made when circuits operate in pulse conditions.

b. Simulated results shall be derived for parameters such as, turn on and off times, variations versus pulse length and pulse repetition frequency.

c. Requirements a. and b. also apply to oscillators for determining, for example, the build up time.

7.2.5 Thermal analysis

a. The maximum channel (or junction) temperature shall be computed for the maximum equipment base-plate temperature (operating temperature range).

b. Measures shall be taken to minimise the temperature by selecting the appropriate size or combination of active devices, their location on the die, and the mounting techniques (e.g. eutectic attachment versus epoxy attachment).

c. The effects and characteristics of the packages on the circuits shall be analysed (e.g. power dissipation).

7.2.6 Sensitivity to temperature, process variation and supply voltages

a. The sensitivity to temperature, process variation and supply voltages shall be simulated using foundry data or measured data from test components.

b. Yield analysis and estimates based on the design book data shall be carried out to ensure that the circuit operates as specified in the wafer-acceptance criteria (both RF and DC parameters), and that it can withstand uncertainties such as, the accuracy of electrical model parameters and variations.

NOTE This includes the choice of, for example, optimum topologies, components, sizes, design centring, worst-case analysis, yield analysis and yield estimate.

c. The analysis shall be carried out for all parameters subjected to process variations and include, whenever possible, correlations between the different elements that cause variations.

d. When delivered by the foundry, SPC data should be used.

7.2.7 Design testability

a. Ground-source-ground pads with the standard pitch defined in the design book, shall be included for all RF ports.

b. For specific cases, alternative pad arrangements (e.g. G-S or S+ S- pads) may be used after justification is provided (for example, a significant area reduction effect on the die).

c. DC pads should be positioned orthogonally to the RF pads.

d. For critical cases and at higher frequencies, an on-wafer calibration standard can be inserted in the tile (e.g. to remove uncertainties related to substrate thickness variation).

7.2.8 Design stability analysis

a. Design stability analysis shall be carried out from the DC to the maximum frequency of the active devices used.

b. The analysis (e.g. using μ factor or both K and B1 factors) shall be complemented by an internal multi-loop analysis to exclude any possibility of oscillations of the odd-mode type.

c. For a cascaded structure, as a minimum, the stability of each block shall be checked individually.

d. The analysis shall also include the effect of feedback paths caused by the following:

- the biasing elements (on and off-die);
- the final packaging;
- the effects of process variations, temperature, and slight changes of biasing conditions.

e. Circuit stability during on-wafer characterization shall be addressed.

7.2.9 Maximum rating and robustness

a. The designer shall apply and verify the maximum rating specified by the manufacturer.

b. The designer shall also apply the additional derating in conformance to ECSS-Q-30-11 or an equivalent customer specification as long as the customer specification does not relax ECSS-Q-30-11 requirements.

c. The maximum current densities and maximum voltages shall be evaluated in the whole circuit both at DC and RF operating conditions (e.g. multi-carrier signal).

d. The maximum level of stress under RF conditions (e.g. gain compression, effects of multi-carrier loading) in any device shall be limited to conditions equivalent to those for which the process reliability evaluation is carried out.

e. The circuit topology shall take into account the circuit reliability (e.g. use of L-parallel, C-series matching networks at input to reduce sensitivity to static discharge, choice of transmission line size) while maintaining acceptable electrical characteristics.

f. The effect of radiation shall be included (if applicable to the process used).

g. Any new MMIC design shall be analysed with respect to the process reliability figures compatible with the future application.

h. If the results of the analysis of the design and the application are out of the qualified domain, the user (or the vendor) shall define a quality or reliability test plan for documenting the shortcomings.

7.2.10 Layout optimization

a. The die area shall be optimised to improve yield and reduce cost, without compromising on the functional performance of the die and testability.

b. A hierarchical design should be used.

c. The circuit layout shall be delivered in GDSII format.

d. The number of available die sites per tile shall be specified, and the layout of the complete tile shall be delivered (except PCM die).

e. The location and function of any connecting pads shall be specified and numbered.

f. Testability considerations shall be taken into account.

g. Assembly drawing shall be complete and include all other components additional to the MMIC (e.g. filtering capacitors).

h. The packaging drawing (if applicable) shall be included.

7.2.11 DRC or ERC

a. The successful output of the design rules checking (DRC) performed at the foundry shall be demonstrated to show conformance with the foundry layout rules (e.g. no errors detected).

b. The successful output of the electrical rules checking (ERC) performed at the foundry (if performed) shall be demonstrated to show conformance with the foundry electrical rules (e.g. no errors detected).

c. For all the points not covered by a. and b., the contractor shall demonstrate that the design is made within a domain for which the selected process is fully proven (e.g. frequency range of applicability of models, biasing ranges).

7.3 Design reviews

7.3.1 General

a. Design and layout review meetings shall be held between the designer, the vendor and the user.

b. When the design is completed, the designer shall send the file to the vendor for assembly of the final reticule and performance of the DRC.

c. The design review shall be at the vendor's facilities and both parties (designer and vendor) be involved in assessing whether the circuits are ready for manufacturing.

d. In the design review meeting, the requirements in 7.3.2 to 7.3.14 shall be addressed in the given order.

7.3.2 MMIC architecture

a. The designer shall provide a description of the function(s) and their features.

b. The vendor shall verify that the characteristics are realistic with regard to the domain of the process.

7.3.3 Schematic

The designer shall present the electrical scheme of the circuits.

7.3.4 Simulation results

a. The designer shall state the software or hardware type used for the design.

b. The designer shall provide the simulation results demonstrating that the circuit belongs to the functionality domain specified and that the MMIC was designed using, for example, models and cells, specified in the design manual.

c. Any discrepancy or modification in, for example, the models and cells, shall be clearly identified, and justification and documentation supplied.

d. The designer shall demonstrate that the electrical models used in the simulations are valid for the specified application domain (including the worst case analyses).

7.3.5 Sensitivity and stability analysis

a. The designer shall provide the results of the sensitivity analysis.

b. Variations in the manufacturing process shall be taken into account in the design.

c. Variations in the environment shall be taken into account by the user.

7.3.6 Derating

a. The designer shall provide the derating for each passive or active element (calculated from the vendor maximum rating).

b. The derating analysis shall be performed for the worst case of use scenario and conform to the requirements of the ECSS-Q-30-11.

ECSS

7.3.7 Layout

a. The vendor shall provide the DRC and ERC results.

b. If no software is available, the ERC shall be made "manually" on a large-scale drawing with the following:

- highlight the connection nodes;
- surround the basic cells;
- mark the DC and RF paths;
- measurement of the track dimensions and compare them to the design rules (current density).

c. For the manual ERC, the designer shall provide, for the review and for each circuit, a schematic of the electrical connections.

7.3.8 Tests matrix

a. The testing matrix, to be performed by the vendor at wafer level or at individual die level, shall be provided by the designer.

b. The vendor shall ensure that he has adequate test facilities to perform the tests.

7.3.9 Assembly

a. The designer shall specify the mounting technique for assembling the MMICs.

b. The user shall verify that the MMIC process is compatible with the intended mounting technique.

7.3.10 Compliance matrix

a. The vendor, the designer and the user shall issue a compliance matrix for custom MMIC designs (check-list) which shall be available for customer review.

b. The existence of the compliance matrix is indicated in the PAD sheet.

c. The compliance matrix shall summarise the following:

1. The function description and associated main characteristics.
2. The software or hardware used for the design.
3. Verification that the circuit belongs to the specified functional domain and is designed using, for example, the models and cells, described in the design manual. If not, an extension of the qualification domain shall be provided.
4. The results of the sensitivity and stability analyses.
5. The derating of the elementary parts.
6. The DRC results.
7. The ERC results.
8. Verification from the vendor that he can perform the set of tests specified by the designer for the wafer or dies release.

7.3.11 MMIC detail specification

The designer shall provide the preliminary MMIC detail specification of the circuit based on ESCC format (or equivalent).

7.3.12 Development plan

a. The development plan of the circuit(s) defining the planning of manufacturing and testing shall be agreed upon by the customer.

b. The design review shall be completed and the authorization for manufacturing given when all the items indicated in the conformance matrix and in the development plan are accepted.

c. If there are nonconformances, the end of the review shall be pronounced when the corrective actions are closed.

d. All the reviews shall be recorded as minutes of a meeting, written and signed in session.

7.3.13 Design documentation

a. For the design of an MMIC, a design package document shall be provided and approved by the customer before the MMIC manufacturing can commence.

b. The design package document shall include the following:

1. Description of functionality and any functional blocks.
2. List of the major critical items in the circuit design and the trade‐offs performed.
3. Schematic diagrams.
4. Linear simulation including out‐of‐band response.
5. Noise analysis, including phase noise (if applicable to the specific circuit).
6. Non‐linear simulation, steady state (if applicable to the specific circuit).
7. Transient simulation.
8. Electromagnetic analysis (if applicable to the circuit: this depends on, for example, the frequency of operation, sensitivity of the circuit, density on the die, thickness of the substrate, type of transmission lines used, similarity with already produced die).
9. DC analysis (if applicable to the circuit), for example, for non‐linear circuits or circuits using DC coupled active elements.
10. Tolerance analysis, stability analysis, thermal analysis, reliability analysis.
11. Layout.
12. DRC or ERC.
13. On‐wafer testing (when performed).
14. Cost analysis budgetary cost estimates for production runs of the MMIC designed. This estimate shall be detailed for circuits to be produced in large quantities.
15. Test plan or procedures (these shall also contain the calibration approach and accuracy).
16. On‐wafer and test‐jig measurements (including test‐jig mechanical and electrical characteristics).

c. The contractor shall provide a compliance table between target requirements and simulated results.

7.3.14 MMIC summary design sheet

a. Once the design of the MMIC is finalised and verified by tests, a summary design sheet shall be prepared.

b. The design sheet shall include the following:

1. Name of the circuit.
2. Function.
3. Electrical diagram.
4. Main performance characteristics.
5. Compliance table between target and simulated performance.
6. Name of the final GDSII file.
7. Layout drawing (with dimensions and identification of each connection pad position and function).
8. Foundry process used.
9. Assembly drawing (including external components needed).
10. List of nominal biasing and control voltages or currents, and total power consumption.
11. List of nominal RF signals to be applied or measured.
12. Photograph (in colour and details).

8 Application approval

8.1 General

a. Application approval shall be carried out on each new designed MMIC in order to validate the compatibility between the MMIC and its specified application.

b. Dedicated test flow and test procedures shall be implemented as per subclause 8.2.

c. For microwave hybrids, the testing shall be complementary to the circuit type approval (CTA) as described in the ECSS-Q-60–05.

d. Additional hybrids shall be made available with the same quality level as for the CTA (minimum EM hybrid quality level).

e. Deviations and test conditions to this flow shall be justified by the hybrid manufacturer and agreed with the customer through the part approval document (PAD) procedure.

8.2 Test flow and test procedures

The test sequence shall be included as part of the hybrid CTA activities in accordance with ECSS-Q-60-05. Table 2 summarises the test groups and procedures.

Table 2: CTA tests and procedures for testing in sequence D

Test No.	Test	Procedure and conditions	Sample size	Related failure mechanism
1	Thermal	Thermal analysis of the MMIC to identify hot spots or excess temperature during worst-case operations. Thermo-graphic measurement shall be carried out when the thermal analysis has indicated a less than 20 °C margin to the maximum rated temperature under worst-case operation.	2	– Acceleration factor of failure mechanisms. – Thermo‐metallurgical. – Diffusion effect (gate sinking, ohmic metal diffusion).
2	Electrical	Current density analysis on the MMIC for worst-case operation and comparison with the design book maximum rating.	NA	Electromigration
3		Characterization of MMIC behaviour over temperature range, under DC or RF and continuous or pulse operation (e.g. stability, lagging).	2	Trapping effect
4		RF Stress overdrive. RF step stress at room temperature, 168 h minimum for the last step. Last step stress shall demonstrate a minimum of 4dB margin against worst-case operation including modulation with no drift on DC and RF parameters.	4	– Application related with impact ionization. – High RF reverse gate current. – Power slump burn out due to RF.
5	Radiation	Heavy ions: analysis versus mission profile. Heavy ions testing under room temperature reverse bias conditions.	4	– Burn out. – SEU for digital application.
6		Electron, proton, neutron: applicability to be addressed on a case-by-case basis.	4	Atoms displacement
7	Environment (see a. and b.)	Hydrogen: high-temperature storage test or HTRB under N_2/H_2 (minimum 5% H_2) environment for a minimum of 240 h or equivalent. RGA analysis extended to all elements after test.	6	– H_2 poisoning. – DC parameters drift. – Sudden I_{dss} drop.
8		Epoxy or other contaminant: DC life test HTRB) at 150 °C for a minimum of 240 h or equivalent. Drift recovery under high-temperature storage with leads short-circuited at T=150 °C, 168 h. RGA extended to all elements.	6	– Ionic contaminant (epoxy, residue, RF absorbers). – DC parameters drift.
9		Moisture, LTRB (T_{amb} < dew point) 168 h under user humidity environment due to assembly and storage condition or due to additional element in package e.g. RF absorbent. RGA extended to all elements.	6	– Electrical parameters drift. – Burn-out.

a. The environment testing shall validate the compatibility of the new MMIC design circuits with the package environment.
b. It shall not be considered to be a duplication of environmental testing carried out in the context of the hybrid evaluation and qualification activities used for validating the compatibility between the MMIC and hybrid technologies.

9
Procurement and LAT specification

a. A procurement specification shall be associated with each MMIC and shall include, as a minimum, the following:

1. The physical description of the tile and all associated die (name, dimensions, cells).
2. The electrical test plan (DC biasing, RF input conditions) for on-wafer probing.
3. All parameter specification limits to be applied for die sort.
4. Packaging definition.
5. Quality level of visual inspection for die delivered.

b. A lot acceptance specification for user LAT shall be implemented and shall contain, as a minimum, the following:

1. Die reference submitted to user LAT (using either a TCV, a DEC or an MMIC).
2. The description of the package to be used for the mounting with lead identification.
3. The description of the mounting and wiring processes (if the mounting and wiring processes are different from the user hybrid process, the procured lot shall be validated with respect to the user process by performing an additional LAT or by using the LAT performed at hybrid level providing sufficient confident data are available).
4. Table 1: maximum ratings. This table shall include the limiting electrical, mechanical and thermal parameters.
5. Table 2: electrical measurements at ambient temperature with static and dynamic parameters.
6. Table 3: electrical measurements at high and low temperatures.
7. Table 4: parameter drifts. This table shows the electrical parameters before and after burn-in with the maximum drift allowed.

8. Table 5: burn in conditions. This table shows the oven temperature and power applied.
9. Table 6: electrical measurements after endurance tests. This table shows the parameters measured and the minimum and maximum values tolerated following the life test at the ambient temperature.
10. Table 7: life test conditions. This table shows the oven temperature and power applied.

c. Both specifications can be merged on completion of all testing by the vendor and user for the finalization of the MMIC detail specification.

Clause 10 defines the requirements for these documents.

10

Procurement

10.1 Methodology

This Clause contains the deviations and amendments to ECSS- Q-60-05, specific to MMIC procurement.

The procurement activity comprises three steps:

a. Wafer screening and wafer acceptance testing (WAT) (MMIC vendor responsibility).

b. Dies incoming inspection (hybrid manufacturer responsibility).

c. User lot acceptance testing (LAT) (hybrid manufacturer responsibility).

10.2 Wafer screening and WAT

10.2.1 General

Wafer screening and wafer acceptance testing (WAT) shall be the responsibility of the vendor. The test flow and relevant test conditions are described in 10.2.2 to 10.2.6.

10.2.2 Wafer screening and WAT flows

Figure 1 illustrates the sequence of activities for wafer screening and WAT.

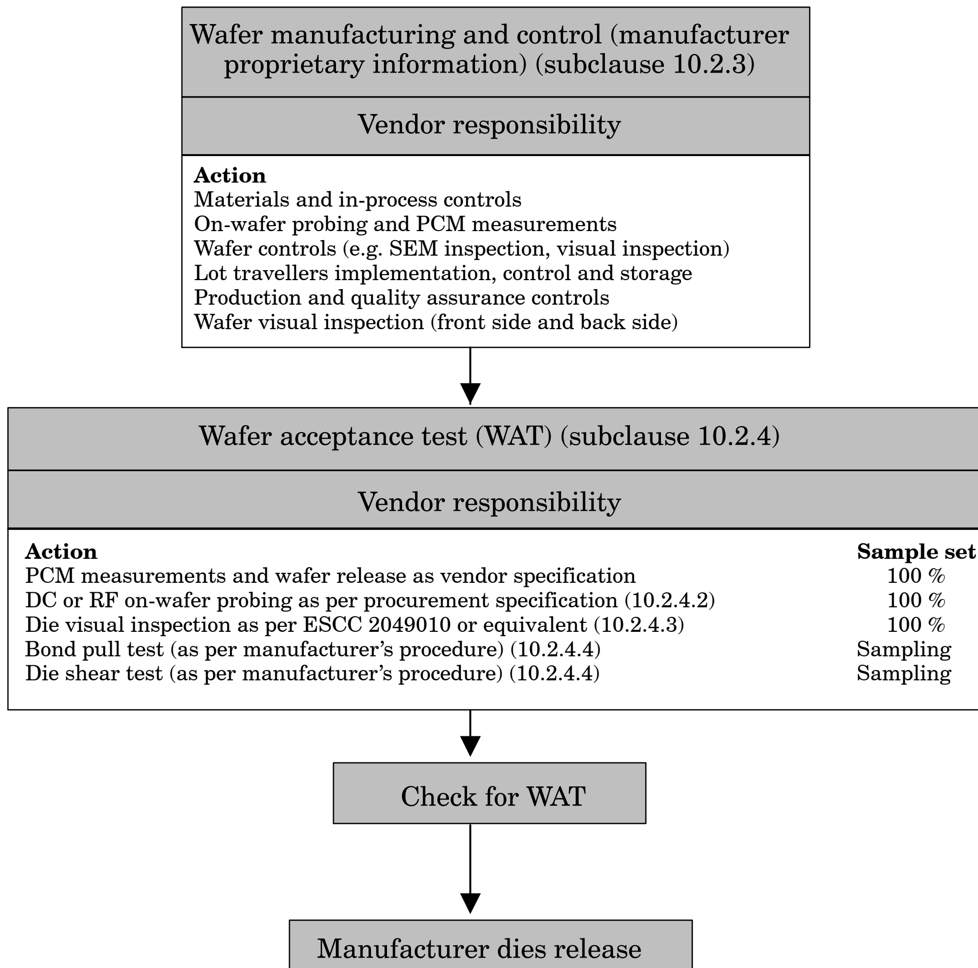

Figure 1: Wafer screening and WAT

10.2.3 Wafer manufacturing and control

a. PCM measurements, rules and controls, shall be in conformance with the vendor design book requirements.

b. Wafers shall be accepted, based on PCM specifications, as defined by the vendor.

c. PCM data that is vendor proprietary information, can be delivered, if agreed upon by the vendor and user.

d. DC and RF on-wafer probing shall be performed by the vendor prior to the dicing and be used to sort the dies as defined in the procurement specification.

e. Optional reviews such as a customer source inspection, may be agreed between the user and the vendor.

f. During the optional reviews in e., documentation shall be available that includes:

- materials and in-process controls;
- lot travellers;
- PCM acceptance;
- SPC data review;
- SEM of specific processing step;
- production and quality assurance controls;
- manufacturer visual inspection data documents and reports.

10.2.4 Wafer acceptance test

10.2.4.1 General

a. Wafer acceptance testing (WAT) is the responsibility of, and shall be performed by, the vendor.

b. The WAT shall verify that the process and the MMIC designs are compliant to the space grade quality level.

c. The WAT shall comprise the following:

- PCM measurements and a check for wafer release according to the vendor specification;
- 100% DC and RF on wafer probing;
- 100% die visual inspection;
- a vendor assembly test (bond pull test and die shear test).

d. On completion of the WAT, the wafers (issued from the same batch) shall be guaranteed and delivered after dicing in die form as specified in the procurement specification.

10.2.4.2 DC and RF probing

a. All the MMICs shall be electrically probed for DC and RF, as defined in the procurement specification.

b. The dies that pass shall be identified and stored with the appropriate packaging and under suitable conditions.

10.2.4.3 Dicing and 100 % visual inspection

a. All visual inspection sequences shall be performed according to ESCC 2049010 or MIL-STD-883, method 2010 condition A or according to standard professional grade (vendor or user procedure) if validated by the customer.

b. 100% of the naked die shall be visually inspected after dicing.

c. A summary sheet of the visual inspection shall include all references for traceability purpose and, as a minimum, the quantities of the following:

- good dies, sorted after DC and RF testing;
- rejected dies after visual inspection;
- accepted dies for each type of MMIC.

10.2.4.4 Vendor assembly test

a. In order to guarantee the quality of the interface (bonding pad metals and die back face metals), the vendor shall implement an assembly test sequence if specified in the procurement specification.

b. The assembly test sequence shall be performed by sampling rejected dies (assembled using the vendor process) from the wafers manufactured, and includes the following:

- A bond pull test on 10 wires as per MIL-STD-883 method 2011.
  No failures allowed.
- A die shear test on 2 parts as per MIL-STD-883 method 2019.
  No failure allowed.

c. If the test sequence performed is based on the user assembly process and in accordance with the user assembly test defined for the incoming inspection, then this test shall not to be repeated by the user when dies are received.

d. For c., a document shall be issued by the user stating that the assembly process used by the vendor is representative of the hybrid process.

10.2.5 Packaging

a. All deliverable dies shall be packed in accordance with ESCC 20600.

b. Waffle packs should be used but can attract dust and cause scratching if not handled with care.

c. Gel packs shall be validated with respect to any contamination or residue after storage.

d. All packaging shall be opened in a suitable clean room using the appropriate procedure.

e. Several categories of dies may be delivered (including yield information):

- good DC or RF and good visual;
- good DC or RF and bad visual;
- test structures (TCV, DEC, PCM).

10.2.6 Deliverables

a. The data package shall comprise the results of the controls described in 10.2.3 to 10.2.5.

b. If a data package is not delivered, all data shall be retained by the vendor for a minimum of 5 years during which time it shall be available to the customer for review, upon request.

c. The vendor data package documentation shall consist of the following:

1. Cover sheet or certificate of compliance, full traceability (including for lot, batch, wafers, dies), purchase order reference, manufacturer's name and location of manufacturing plant.
2. Certificate of conformity (manufacturer's name and location of manufacturing plant, date and manufacturer's QA signature, reference to the generic and detail specification, including issue and date).
3. Wafer acceptance test data and PCM data summary sheet.
4. DC or RF measurement data for every MMIC type and associated yields.
5. QA visual inspection report (front side and back side).

d. In the "foundry" mode, each type of MMIC shall be delivered, with traceability and quantity information written on the packaging, in two categories:

- "accept: good dies (DC or RF) and good visual",
- "reject: good dies (DC or RF) and bad visual".

10.3 Dies incoming testing

10.3.1 General

This subclause details the requirements that are the responsibility of the user.

a. Dies incoming testing shall be carried out when a new die lot is received as per Figure 2 (see also 3.1.4).

b. The testing shall include the following test sequence:

- bondability testing;
- visual inspection;
- electrical characterization.

c. Testing shall be carried out by the user for every MMIC die lot and prior to the user LAT.

10.3.2 Assembly test

a. The assembly test shall verify the compatibility between the MMIC process and the hybrid technology.

b. The mounting process and the type of package used for the tests shall be representative of the processes employed for the FM hybrids by the user.

c. The mounting process and the type of package used for the tests shall be described in the specifications included in the PID of the user.

d. Dies rejected during the front side visual inspection issued from the controls can be used to perform the test.

e. The MMIC selected for the tests shall have, if possible, the maximum via hole density.

f. Wire pull testing shall be performed according to MIL-STD-883 method 2011 on 22 wires or on all the wires if less.

No failure allowed.

g. The shear test on mounted dies shall be according to MIL-STD-883 method 2019 on 4 dies.

No failure allowed.

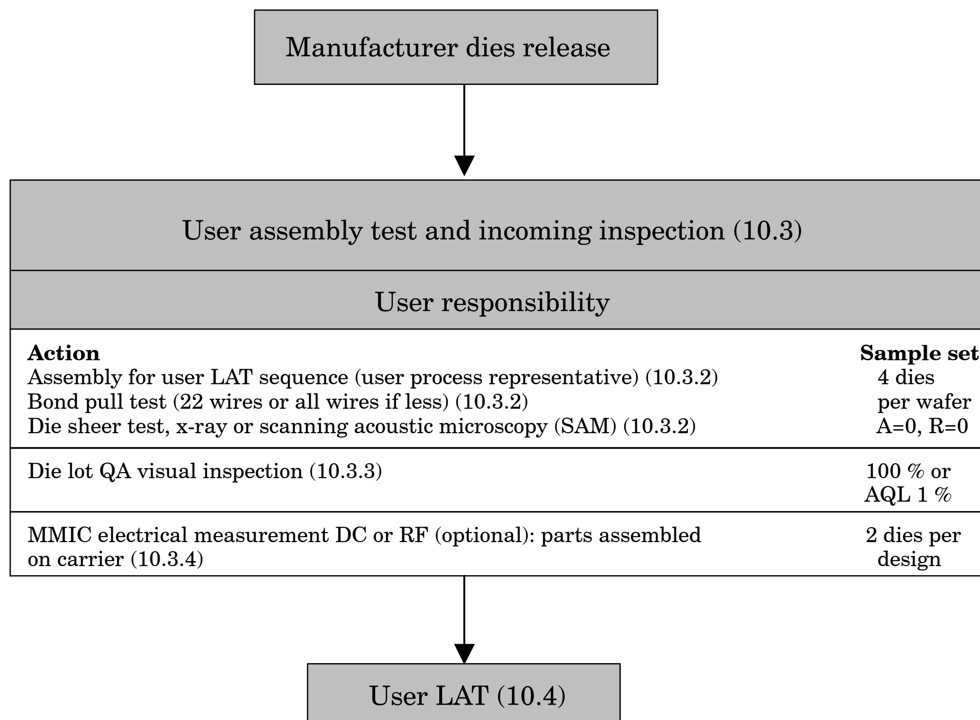

Figure 2: Dies or die incoming testing

10.3.3 Visual inspection

The user quality assurance inspector shall carry out a visual inspection of the lot on a 100 % basis or on an AQL 1 %.

10.3.4 Electrical characterization

The objective of this optional testing is to select dies lots for specific application requirements, which cannot be characterised on the wafer.

For this test, 2 parts per design shall be assembled on a carrier or in a package similar to the one used for hybrid FM production.

10.4 User LAT procurement sequences

10.4.1 General

The purpose of the LAT performed by the vendor is to assess the reliability of the technology (LAT DEC or TCV) and the reliability of the MMIC design (LAT MMIC). The purpose of the LAT performed by the user is to assess the technology and MMIC design, and the compatibility of the MMIC with the assembly process.

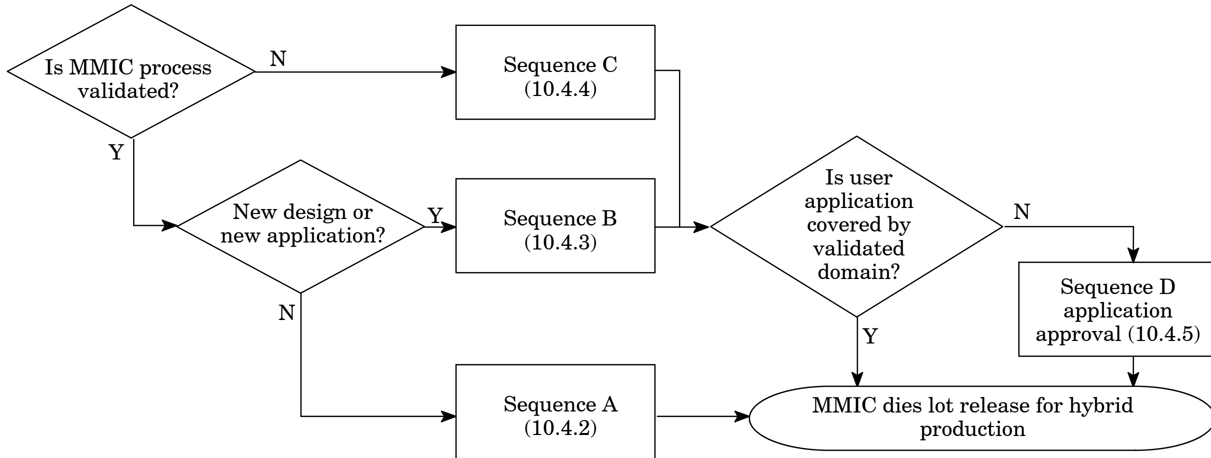

Figure 3: Acceptance flow for flight model die lots

Depending on the validated process status of the MMIC, the maturity of the design and the application, the acceptance flow for FM dies is defined in three flow test sequences (Figure 3):

- Sequence A: This flow applies when process, design and application have already been validated.
- Sequence B: This flow is applies when the process is validated and a new design or a new application needs to be validated.
- Sequence C: This flow is applies when the MMIC design, application and the process are not validated.

a. From the three sequences, the severity of acceptance testing shall be specified in order to obtain consistent Space grade quality levels.

b. Sequence D is the application approval as defined in Clause 8 and shall be performed to validate new designs or new applications.

c. The user LAT shall be performed using TCV, DEC or MMICs as per Figure 4 in accordance with ESCC 2439010.

d. Test vehicles shall be mounted in packages that enable tests (maximum junction temperature T_j = 175 °C), electrical measurements and inspections to be performed.

e. For a LAT performed by the user, the assembly processes and the type of package used for TCV, DEC and MMIC mounting shall be representative of the processes defined in the user’s PID.

f. The number of units that are assembled shall be sufficient to ensure that after screening, the specified number of units as defined in Figure 4 are available.

g. The screening of the assembled devices shall include the following:
   - visual inspection (if specified);
   - sealing and serialization;
   - hermeticity (if applicable) (fine and gross leak test) as per MIL-STD-883 method 1014;
   - DC and RF initial electrical measurement at room temperature (including one control device for reproducibility verification) under nominal DC biasing and nominal RF input;
   - DC burn in at T_{ch} = 175 °C, for 96 h under nominal biasing condition (no RF);
   - DC and RF final electrical measurement at room temperature (including one control device for reproducibility verification) under nominal DC biasing and nominal RF input.

h. A specification for user LAT shall be issued as per Clause 9.

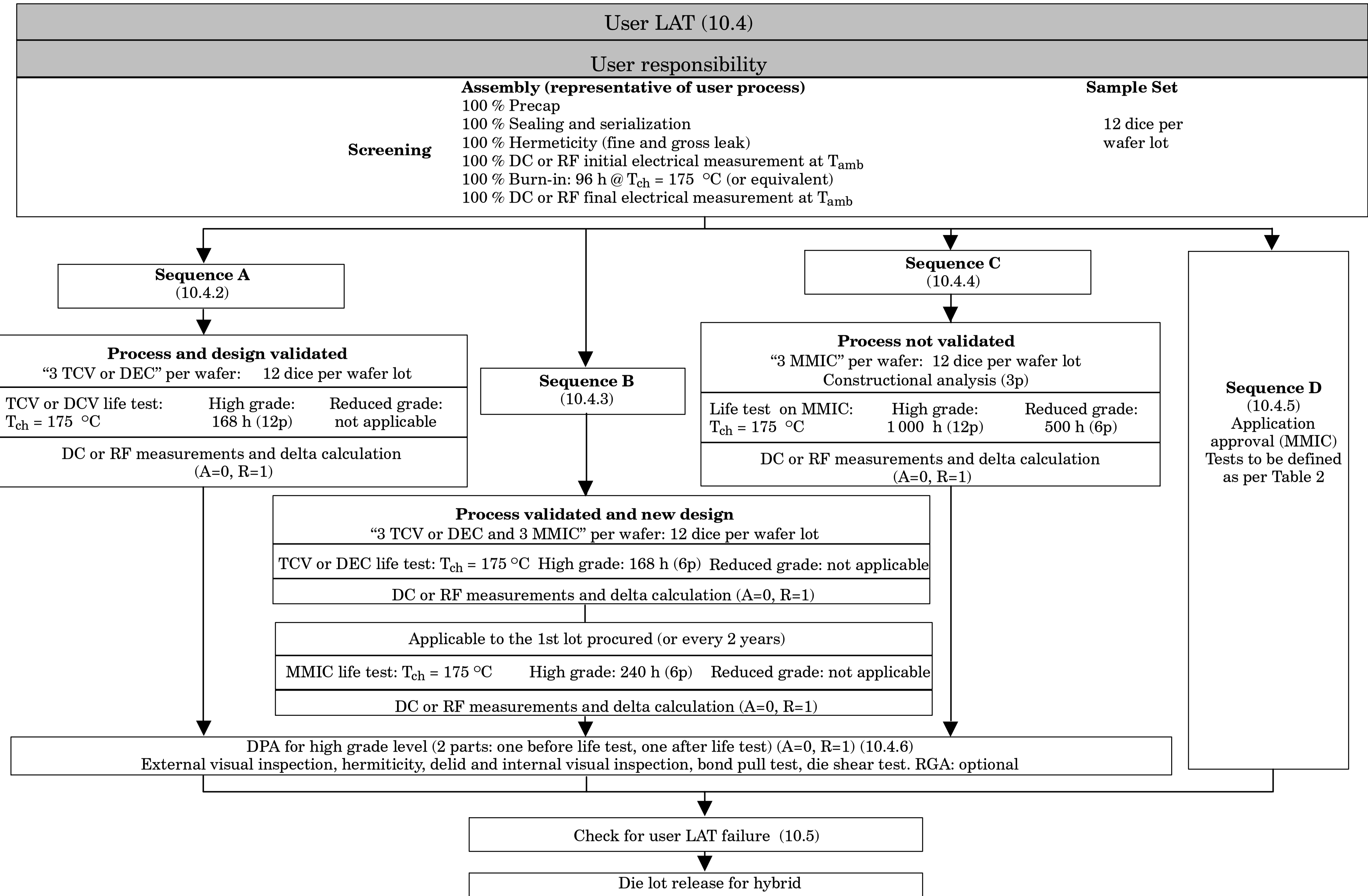

Figure 4: User LAT flow

10.4.2 Sequence A: process, design and application validated

a. The user LAT sequence A shall be applied to the procurement of MMICs processed with a validated process in accordance with customer's requirements and for which the designs have been validated from a reliability point of view by performing application approval testing.

b. For high-grade level, the sequence A shall be conducted on DEC or TCV structures only.

c. The sampling is related to the number of wafers and shall be 3 DEC or TCV per wafer with a total 12 parts per wafer lot and one control device.

d. A life test shall be performed on the 12 parts assembled using processes defined in the user's PID and under nominal biasing conditions (no RF) and high temperature, in an oven, in order to achieve a maximum channel temperature of 175 °C with a tolerance of -5 °C.

e. The duration of the test shall be 168 hours for high-grade level (failure criteria A=0, R=1).

f. If epoxy die attach is used:

1. the temperature within the oven shall be a maximum of 130 °C with a tolerance of -5 °C; and
2. the duration of the life test shall be based on the Arrhenius acceleration factor with Ea=0,6 eV.

g. 100 % final electrical measurements at room temperature and delta calculation shall be made.

No failure allowed.

h. A DPA shall be performed on 2 parts as per 10.4.6.

No defect allowed.

i. Sequence A is not applicable for low grade level.

10.4.3 Sequence B: process validated and new design or new application

a. Sequence B shall be applied to the procurement of MMICs processed with a validated process according to the customer's requirements and for which the design is new and not validated from a reliability point of view.

b. For high-grade level, sequence B shall be conducted on DEC or TCV structures and on MMIC dice assembled using the processes defined in the user's PID.

c. The sampling is related to the number of wafers and shall be 3 DEC or TCV per wafer and 3 MMIC (new) per wafer with a total 12 parts per wafer lot and one control device.

d. A 168 h life test shall be performed as per 10.4.2.d. and e. on 6 parts DEC or TCV structures.

e. A 240 h life test shall also be performed on 6 MMIC.

f. If the parts are epoxy die attached, the same restrictions as given in 10.4.2.f. shall apply and the calculations for the duration of the test shall be based on the same acceleration factor.

g. 100 % final electrical measurement at room temperature and delta calculation shall be made.

No failure allowed.

h. A DPA shall be performed on 2 parts (either TCV, DEC or MMIC) as per 10.4.6.

No defect allowed.

i. Sequence B is not applicable for low-grade level.

10.4.4 Sequence C: process, design and application not validated

a. Sequence C shall be applied to the procurement of MMIC processed with a non-validated process according to the customer's requirements.

b. The user LAT shall be considered to be the lot validation.

c. It shall be performed on MMICs with the modified conditions given in d. to j.

d. For high-grade level, a 1 000 h life test shall be applied on 12 packaged MMIC per wafer lot (assembly process as per user's PID).

e. If the parts are epoxy die attached, the same restrictions as given in 10.4.2.f. shall apply and the calculations for the duration of the test shall be based on the same acceleration factor.

f. For low-grade level, the duration of the life test shall be reduced to 500 h on 6 parts per wafer lot only.

g. 100% final electrical measurement at room temperature and delta calculation shall be made.

   No failure allowed.

h. For both levels, a DPA shall be performed on 2 parts (one before the life test and one after) (either TCV, DEC or MMIC) as per 10.4.6.

   No defect allowed.

i. A construction analysis (CA) shall be performed on 3 dice for the first procured lot.

j. The CA shall include, as a minimum, the following analyses:
   - external visual inspection (MIL STD 883 method 2009);
   - internal visual inspection (MIL STD 883 method 2010);
   - SEM inspection (MIL STD 883 method 2018);
   - identification of bonding pad and back side metals and their thicknesses;
   - passivation material and thickness;
   - die dimension;
   - micro-section showing the gate zone (with dimensions).

10.4.5 Sequence D: application approval testing

a. When specified, sequence D shall be applied, prior to the user LAT sequences.

b. A test plan shall be issued and agreed upon by the customer.

c. The test plan shall detail the tests to be performed on a defined quantity of CTA as described in ECSS-Q-60-05 (see Table 2 of subclause 8.2).

d. The test plan shall be documented and some tests may be omitted if the heritages on the technology or on the design are sufficient and demonstrated.

e. The user shall be responsible for defining the tests to support the reliability tests based on Table 2.

f. Hybrids or dedicated packaged MMIC (one MMIC per package) can be used to complete this sequence of test.

g. For f., the packaged parts shall be representative of the production process defined in the PID (assembly and sealing process) and be screened according to the flow defined in Figure 4 and subclause 10.4.

h. Due to the conditions of stress, some tests may be conducted up to and above the failure limits with the purpose of assessing the existing margin due to a specific constraint.

i. If h. is performed, it should be stated in the test plan document.

10.4.6 Destructive physical analysis after user LAT

The following tests shall be performed as part of the DPA:

• External visual inspection	MIL-STD-883 Method 2009.8
• Seal test	MIL-STD-883 Method 1014 condition A2 – condition C
• Internal visual inspection	ESCC 2409010 or equivalent
• Bond pull test	MIL-STD-883 Method 2011 condition D
• Die shear test	MIL-STD-883 Method 2019
• RGA (option)	MIL-STD-883 Method 1018.2.

10.5 Failure criteria and lot failure

a. A component shall be considered to be failed if one or more of the electrical parameters (DC and RF) exceed the limits defined in Table 4 of the corresponding detail specification.

b. In the case of a LAT performed by the vendor, failures due to the assembly of the test structures shall be excluded from the results, and therefore not lead to lot failure.

c. In the case of a LAT performed by the user, a part shall be considered failed if at least one test does not satisfy the limits defined in the specification associated to the process.

d. Any relevant failures (see f.) observed in assembly tests shall be included in a nonconformance sheet and the problem subjected to a review.

e. The customer shall be informed of the nonconformance and decide when it can be closed.

f. A relevant failure is one that only address a problem at die level (for example: bond pull failure criteria at wire neck shall not be counted as a defect from the die point of view).

g. During user LAT, if the number of components failed during assembly or screening exceeds 10% of the components submitted to these tests and associated electrical measurements, the lot shall be considered as failed.

h. In the case of g. the lot shall be treated using the nonconformance procedure.

i. Parts failed during the LAT screening may be replaced by new assembled and re-screened parts in order to make up the quantity for the life test sequence.

j. A component shall be counted as failed if one or more electrical parameters (DC and RF) exceed the limits defined in Table 4 of the corresponding detail specification.

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Bibliography

ECSS-E-00	Space engineering – Policy and principles
ESCC QPL	ESA qualified parts list
ESCC 5010	Generic specification for discrete microwave semiconductor components
ESCC/REF 001	List of ESCC documents and specifications under configuration control.
CECC 00200	Register of approvals
ISO 14621-1	Space systems - Electrical, electronic and electromechanical (EEE) parts - Part 1: Parts management
ISO 14621-2	Space systems - Electrical, electronic and electromechanical (EEE) parts - Part 2: Control programme requirements

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1. Originator's name: Organization: e-mail:				2. ECSS Document number: 3. Date:	
4. Number.	5. Location of deficiency clause (e.g. 3.1	page 14)	6. Changes	7. Justification	8. Disposition

Filling instructions:

1. **Originator's name -** Insert the originator's name and address
2. **ECSS document number -** Insert the complete ECSS reference number (e.g. ECSS-M-00B)
3. **Date -** Insert current date
4. **Number -** Insert originator's numbering of CR/DIP (*optional*)
5. **Location -** Insert clause, table or figure number and page number where deficiency has been identified
6. **Changes -** Identify any improvement proposed, giving as much detail as possible
7. **Justification -** Describe the purpose, reasons and benefits of the proposed change
8. **Disposition -** not to be filled in (*entered by relevant ECSS Panel*)

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