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Space product assurance

Procurement of printed circuit boards

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Foreword

This Standard is one of the series of ECSS Standards intended to be applied together for the management, engineering and product assurance in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards.

Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

The formulation of this Standard takes into account the existing ISO 9000 family of documents.

This Standard has been prepared by the ECSS Q-70-11 Working Group, reviewed by the ECSS Technical Panel and approved by the ECSS Steering Board.

This Standard is based on ESA PSS-01-710.

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Introduction

PCBs are used for the mounting of components in order to produce printed board assemblies performing complex electrical functions. The PCBs are subjected to thermal and mechanical shocks during their assembly such as mounting of components by soldering, rework and repair under normal terrestrial conditions, and in addition the complex printed board assembly is subjected to the environment imposed by launch and space flights. Therefore the qualification of a PCB supplier to ECSS-Q-70-10 is of extreme importance before the procurement of PCB for space usage.

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Scope

This Standard defines the requirements imposed on both the customer and the qualified PCB supplier for PCB procurement. This Standard also details the basic requirements for procurement of PCBs as well as the minimum requirements for the different types of PCBs.

This Standard is applicable for the following type of boards:

- rigid printed boards (single-sided, double-sided, multilayer, sequential- laminated multilayer and metal core);
- flexible printed boards (single-sided and double-sided);
- rigid-flex printed boards (multilayer and sequential-laminated multilayer);
- high frequency printed boards;
- special printed boards.

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Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references the latest edition of the publication referred to applies.

ECSS-P-001	Glossary of terms
ECSS-Q-70	Space product assurance — Material, mechanical parts and processes
ECSS-Q-70-02	Space product assurance — Thermal vacuum outgassing test for the screening of space materials
ECSS-Q-70-07	Space product assurance — Verification and approval of automatic machine wave soldering
ECSS-Q-70-08	Space product assurance — The manual soldering of high-reliability electrical connections
ECSS-Q-70-10	Space product assurance — Qualification of printed circuit boards
ECSS-Q-70-28 [1)]	Space product assurance — Repair and modification of printed circuit board assemblies for space use
ECSS-Q-70-38 [1)]	Space product assurance — High-reliability soldering for surface-mount and mixed technology printed-circuit boards
IEC 60249-1-am-4 (1993-05)	Base materials for printed circuits. Part 1: Test methods
IEC 60326-2-am1 (1992-06)	Printed boards. Part 2: Test methods
IPC-4101	Specification for base materials for rigid and mulitlayer printed boards
IPC-MF-150F	Metal foil for printed wiring applications

1) To be published.

IPC-CF-152B	Composite metallic material specification for printed wiring board

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Terms, definitions and abbreviated terms

3.1 Terms and definitions

The following terms and definitions are specific to this Standard in the sense that they are complementary or additional to those contained in ECSS-P-001.

3.1.1
blister
delamination in the form of a localized swelling and separation between any of the layers of a lamination base material, or between base material and conductive foil or protective coating

[IEC 60194 (1999-04)]

3.1.2
cover lay (flexible circuit)
the layer of insulating material that is applied covering totally or partially over a conductive pattern on the outer surfaces of a printed board

[IEC 60194 (1999-04)]

3.1.3
crazing
an internal condition that occurs in reinforced base material whereby glass fibres are separated from the resin at the weave intersections

NOTE 1 This condition manifests itself in the form of connected white spots or crosses that are below the surface of the base material. It is usually related to mechanically induced stress.

NOTE 2 See also “measling”.

[IEC 60194 (1999-04)]

3.1.4
delamination
a separation between plies within a base material, between base material and a conductive foil, or any other planar separation with a printed board. (See also “Blister”.)

[IEC 60194 (1999-04)]

3.1.5
dewetting
a condition that results when molten solder coats a surface and then recedes to leave irregularly-shaped mounds of solder that are separated by areas that are covered with a thin film of solder and with the basis metal not exposed

[IEC 60194 (1999-04)]

3.1.6
flexible printed board
a printed board either single, double sided or multilayer consisting of a printed circuit or printed wiring using flexible base materials only *[IEV 541-04-03, modified]*

[IEC 60194 (1999-04)]

3.1.7
haloing
mechanically-induced fracturing or delamination, on or below the surface of a base material, that is usually exhibited by a light area around holes or other machined features

[IEC 60194 (1999-04)]

3.1.8
high frequency printed board
printed board used for high frequency applications, that has specific requirements to the dielectric properties of the base laminates as well as special dimensional requirements to the lay-out for electrical purposes

3.1.9
inclusions
foreign particles, metallic or non-metallic, that may be entrapped in an insulating material, conductive layer, plating, base material or solder connection

[IEC 60194 (1999-04)]

3.1.10
key personnel
personnel with specialist knowledge responsible for defined production or product assurance areas

3.1.11
measling
a condition that occurs in laminated base material in which internal glass fibres are separated from the resin at the weave intersection

NOTE 1 This condition manifests itself in the form of discrete white spots or “crosses” that are below the surface of the base material. It is usually related to thermally-induced stress.

NOTE 2 See also “crazing”

[IEC 60194 (1999-04)]

3.1.12
metal core printed board
printed board using a metal core base material *[IEV 541-04-03]*

[IEC 60194 (1999-04)]

3.1.13
multilayer printed board
the general term for a printed board that consist of rigid or flexible insulation materials and three or more alternate printed wiring and/or printed circuit layers that have been bonded together and electrically interconnected

[IEC 60194 (1999-04)]

3.1.14
prepreg
a sheet of material that has been impregnated with a resin and cured to an intermediate stage, i.e., B-staged resin

[IEC 60194 (1999-04)]

3.1.15
printed board
the general term for completely processed printed circuit and printed wiring configurations

NOTE This includes single-sided, double sided and multilayer boards with rigid, flexible, and rigid-flex base materials. *[IEV 541-04-03, modified]*

[IEC 60194 (1999-04)]

3.1.16
printed circuit board
printed board that provides both point-to-point connections and printed components in a predetermined arrangement on a common base

[IEC 60194 (1999-04)]

3.1.17
rigid double-sided printed board
double-sided printed board, either printed circuit or printed wiring, using rigid base materials only *[IEV 541-04-03, modified]*

[IEC 60194 (1999-04)]

3.1.18
rigid-flex printed board
a printed board with both rigid and flexible base materials

[IEC 60194 (1999-04)]

3.1.19
rigid-flex double-sided printed board
double-sided printed board, either printed circuit or printed wiring, using combinations of rigid and flexible base materials

[IEC 60194 (1999-04)]

3.1.20
rigid-flex multilayer printed board
multilayer printed board, either printed circuit or printed wiring, using combinations of rigid multilayer and flexible single and double-sided base materials

3.1.21
rigid printed board
a printed board using rigid base materials only *[IEV 541-04-03, modified]*

[IEC 60194 (1999-04)]

3.1.22
rigid single-sided printed board
single-sided printed board, either printed circuit or printed wiring, using rigid base materials only *[IEV 541-04-03, modified]*

[IEC 60194 (1999-04)]

3.1.23
rigid multilayer printed board
multilayer printed board, either printed circuit or printed wiring, using rigid base materials only *[IEV 541-04-03, modified]*

[IEC 60194 (1999-04)]

3.1.24
scratch
a narrow furrow or grove in a surface

NOTE It is usually shallow and caused by the marking or rasping of the surface with a pointed or sharp object.

[IEC 60194 (1999-04)]

3.1.25
sequentially laminated multilayer printed board
a multilayer printed board that is formed by laminating together through hole plated double-sided or multilayer boards

NOTE Thus, some of its conductive layers are interconnected with blind or buried vias.

[IEC 60194 (1999-04)]

3.2 Abbreviated terms

The following abbreviated terms are defined and used within this Standard.

Abbreviation	Meaning
C of C	certificate of conformance
n.a.	not applicable
PCB	printed circuit board
PTH	plated-through hole
PTFE	polytetrafluoroethylene
r.m.s.	root-mean-square
TBD	to be defined

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Procurement of PCBs

4.1 General

Printed circuit boards shall be procured from a PCB supplier with a qualification approval for an identified technology according to ECSS-Q-70-10.

The customer may procure space quality PCB from a PCB supplier with qualification approval according to ECSS-Q-70-10 during the valid period of the approval.

The minimum applicable requirements are those specified in this Standard.

The product quality is the responsibility of the supplier.

In all cases the incoming inspection and control of the delivered PCBs are the responsibility of the procuring customer.

4.2 Recommendations and requirements

- The customer and supplier may make an agreement on a specific procurement specification.
- The agreement between the customer and the supplier can be described in the specific procurement document. This document shall include as a minimum the requirements of this Standard.
- The customer and the supplier should agree how the plotting, drilling and routing data are transferred from the customer to the supplier and how the numbering system for the different issues is assigned to avoid serious mistakes. This should be done also for all construction data, such as hole sizes, contours and thickness dimensions as well as specific requirements regarding electrical requirements and dielectric properties. The customer should further provide the supplier with the net list documentation and agree on a suitable format for this. The net list is used to verify that the customer's data files are correctly transferred to the supplier and to set up the electrical functional testing of the finished PCBs.
- The customer shall consider the manufacturing tolerances given by the PCB supplier when designing the PCB layout. The tolerances and minimum requirements for the various finished PCB are specified in the tables in clause 9.
- The layout and the build of multilayer PCBs should be as symmetrical as possible. A minimum of two prepregs, between layers should be used. The number of electrical layers shall be an even number.

- For rigid-flex boards the board should be ordered with its frame attached in order not to stress the flexible parts during handling and mounting of components. The frame can be detached after the assembly of the boards.
- For planarity reasons the layout shall be carefully discussed with the PCB supplier so that the amount of copper in the boards is evenly distributed.
- For surface mount technology and circuits to be wave soldered, only pads on the external layers should be used (high density circuitry on external layers is not reliable).
- Teardrop design should be used for fine lines and small annular rings.
- Hot air solder levelling (HAL or HASL) and infrared reflow shall not be used. (Normally destructive because of overheating of the board. Also it does not appear possible to fulfil the requirement for the SnPb surface finish with regard to dimensions).
- Before mounting of components or soldering operations a baking shall be performed as specified in ECSS-Q-70-08.

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Base materials

5.1 Base laminate materials

All base materials are mentioned in clause 9, Tables 1 to 5.

All materials shall conform to ECSS-Q-70, IEC 60249 and IPC 4101 Standards.

5.2 Basic metallic layer

External: basic copper size: 70 μm, 35 μm, 17,5 μm and 9 μm.

Internal: basic copper size: 70 μm, 35 μm and 17,5 μm.

Cu-foil: copper quality "HTE" (IPC-MF-150F).

5.3 Plated metallic layers and finishes

5.3.1 Copper (electrolytic)

Minimum purity: 99,5 %.

Minimum ductility: 12 % (18 % is recommended).

Minimum thickness of plated copper in plated-through holes: soldering holes 25 μm and via holes 20 μm.

Minimum thickness of basic and plated copper on surface layer for soldering pads: 40 μm.

Minimum thickness of basic and plated copper for internal layer: 17,5 μm.

5.3.2 Electroplated tin-lead thickness over copper

Before reflow: (15 ± 7) μm is recommended.

After reflow:

- a minimum of 2 μm is required on angle of hole corners (1 μm is tolerated);
- a minimum of 8 μm is required on half the height of the hole wall and a minimum of 2 μm is required on the rest of the hole wall;
- a reflow over the pad and conductor edge is recommended, but not required.

5.3.3 Nickel electrolytic plating (optional) over copper plating

Thickness shall be from 2 μm to 10 μm.

5.3.4 Gold (electrolytic)

Minimum purity: 99,8 % and shall not contain more than 0,2 % of silver.

Thickness: 3 μm to 7 μm over bare copper,
1 μm to 7 μm over nickel plating.

Au for high frequency circuits or other assembly methods, as specified by customer.

Alternative type gold (e.g. for high frequency circuits) may be used, provided that the gold has been proven to be satisfactory during execution of the qualification programme.

If tin-lead plating is applied together with gold plating on the same PCB, a tin-lead overlap on gold of minimum 200 μm should be used on the surface of the board in order to ensure protection of the plated copper layer. This overlap area shall be a minimum of 200 μm distance from the termination pad designated for soldering as given in ECSS-Q-70-08A subclause 8.4.

5.4 Special materials

5.4.1 Metal core

Copper - Invar - Copper: (IPC-CF-152B).

Copper - Molybdenum - Copper: (IPC-CF-152B).

5.4.2 Heat-sinks: material and surface treatment

Copper: as specified by customer (DML).

Aluminium: as specified by customer (DML).

Brass: as specified by customer (DML).

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Printed board delivery

6.1 Marking

The boards shall be marked as follows:

- Supplier logo.
- Board reference code and serial number.

  In the event that there is not sufficient space on the boards for the marking, the customer shall ensure total traceability by other means or ask for a waiver.
- Number of layers (if required).

Marking inks shall be permanent polymer inks, and shall be specified in the procurement documentation. Marking inks shall be capable of withstanding fluxes, cleaning solvents, soldering, cleaning and coating processes encountered in later manufacturing processes according to ECSS-Q-70-07, ECSS-Q-70-08, ECSS-Q-70-28, ECSS-Q-70-38 and conform to the outgassing requirements of ECSS-Q-70-02.

If a conductive marking is used, the marking shall be treated as a conductive element on the board.

6.2 Documentation and quality test specimen

As a minimum the following documents shall be delivered together with the PCBs: Certificate of conformance (C of C) with the requirements set out in this Standard and customer specification and shall contain the following:

a. list of base materials used;

b. results of tests and inspections;

c. quality test specimen (one per panel);

d. microsection of as received plated-through holes (one per panel);

e. any approved nonconformance with the above specifications.

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Packaging

7.1 Handling and storage

Boards shall be stored in a dry environment (see 7.2) until they are soldered. If assembly involves two or more steps, the boards shall be stored in containers either with desiccant or in dry nitrogen environment.

The boards shall be handled only with clean lint-free gloves.

7.2 Packaging

The supplier shall be responsible for the packaging of printed boards and specimen and use the appropriate methods to prevent degradation due to corrosion, deterioration or physical damage, and to ensure safe delivery to the customer.

The boards shall be individually packaged in a non-corrosive material in such a manner that they are protected against damage during shipment and storage.

The packaging shall consist of individual, airtight plastic containers. PVC packaging shall not be used. Desiccant or dry nitrogen filling shall be used in the packaging. If a siccative is used, easy means for indication of moisture content shall be provided.

Containers enclosing packaged boards and quality test specimen shall be suitably padded to avoid direct pressure on, or friction between, the boards; they shall be of the type and size that ensure acceptance by common carrier and safe delivery at destination.

Each shipment shall include the associated documentation.

Each shipping container shall be marked according to customer requirements.

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8

Customer acceptance

8.1 Customer acceptance inspection

Each of the delivered PCBs shall be examined according to printed board delivery clause 6 and subjected to a visual inspection in accordance with the procedure shown in annex A.1.

A PCB with a major nonconformance shall be rejected.

The quality test specimen shall be retained until end of project and may be used for supplementary testing.

8.2 Quality test specimen

In addition to the quality test specimens for in-house use the manufacturer shall produce one quality test specimen per panel, the design of which is representative of the boards to be supplied to the customer. Its design shall be agreed between customer and supplier and, as a minimum, shall enable continuity testing and rework simulation.

8.3 Electrical test

The electrical test shall be agreed between customer and supplier.

As a minimum, functional testing shall be performed either by test bed electrical tester or by flying probe tester.

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Types of PCBs covered by this Standard

9.1 General

The minimum requirements acceptable for high reliability PCBs used for space programmes are defined in the tables below.

These requirements shall apply to both qualification and procurement.

The requirements apply to the finished PCB and do not include the manufacturing tolerances (see 4.2).

The types of PCBs covered by this Standard are:

- Rigid double-sided printed boards:
  - Rigid single-sided and double-sided boards: see subclause 9.2 Table 1
  - Rigid single-sided and double-sided boards for high frequency application: see subclause 9.2 Table 2.
- Flexible printed boards: see subclause 9.3 Table 3.
- Rigid-flex printed boards: see subclause 9.4 (see subclause 9.3 Table 3 for the flexible part and subclause 9.5 Table 4 for the rigid part).
- Rigid multilayer boards: see subclause 9.5 Table 4.
- Sequential rigid multilayer boards: see subclause 9.6 Table 5.
- Special circuits: see subclause 9.7.

9.2 Rigid single-sided and double-sided printed boards

These are the minimum requirements acceptable for qualification and procurement of rigid single-sided, double-sided and high frequency PCBs.

Table 1: Limits of approval and characteristics of finished rigid single-sided and double-sided boards

Item	Limits
Base materials	
(according to ECSS-Q-70, IEC specifications and IPC 4101)	- Woven-glass-reinforced epoxy resin FR4 - Woven-glass-reinforced polyimide resin
Dimensional characteristics	
External dimension tolerance	± 0,2 mm
Thickness tolerance	± 10 %
Active board size, maximum	TBD by the supplier
Board thickness maximum	3,2 mm
Positioning tolerance between registration mark and edge of circuit	± 0,2 mm
Conductor width	200 µm minimum (for fine pitch 120 µm width is tolerated if less than 5 mm from component pad)
Spacing between conductors	300 µm minimum (for fine pitch 150 µm spacing is tolerated if less than 5 mm from component pad)
Conductor tolerance (minimum/maximum)	TBD by the supplier, ±20 % maximum
Tolerance on diameter of terminal pads	TBD by the supplier, ±20 % maximum
Minimum hole diameter:	
- component hole	According to ECSS Q-70-08
- via hole	0,25 mm minimum and maximum aspect ratio t/d = 6
Tolerance on diameter of plated-through holes:	
- nominal Ø ≥ 0,7 mm	Δ maximum 0,15 mm for component hole
- nominal Ø < 0,7 mm	Δ maximum 0,20 mm
Tolerance on diameter of non-plated-through holes	Δ maximum 0,20 mm
Positioning tolerance of holes with respect to reference mark	± 0,1 mm
Relative misregistration pad/hole	≤ 0,15 mm
Misalignment determined by measuring minimum annular ring:	
- solder side	0,20 mm
- component side (reduced pads)	0,10 mm
- non-soldering hole	0,10 mm
Electrolytic coatings	
Electrolytic copper plating	
- minimum purity	99,5 %
- thickness	
• surface pattern	≥ 25 µm
• plated-through holes	≥ 25 µm
• via holes	≥ 20 µm

Table 1: Limits of approval and characteristics of finished rigid single-sided and double-sided boards *(continued)*

Item	Limits
Tin lead plating after reflow	
– tin content of alloy	(63 ± 8) %
– thickness on surface	8 µm in highest part
– thickness in plated-through holes	8 µm in highest part (minimum half height of hole wall)
– thickness on corner angle	2 µm
Electrolytic gold plating	
– minimum purity	99,8 % (shall not contain more than 0,2 % silver)
– thickness on nickel	(4 ± 3) µm
– thickness on copper	(5 ± 2) µm
Electrolytic nickel plating	Optional under gold
– thickness	2 µm to 10 µm
Mechanical characteristics	
Warp and twist	≤ 1,1 % for board thickness ≥1,6 mm ≤ 1,5 % for board thickness <1,6 mm
Conductor adhesion/peel strength	
– on epoxy	≥ 16 N/cm
– on polyimide	≥ 12 N/cm
Pull strength	
– for terminal pads 4 mm Ø	
• on epoxy	≥ 140 N
• on polyimide	≥ 80 N
– for terminal pads 2 mm Ø	
• on epoxy	≥ 35 N
• on polyimide	≥ 20 N
Electrical characteristics	
Insulation resistance	
– intralayer [a]	> 10^4 MΩ
– interlayer [b]	> 10^5 MΩ
Withstanding voltage per mm spacing between conductors	
– intralayer and interlayer	1 000 V r.m.s.
Short time overload	
– 0,035 mm copper thickness	7 A for 4 s
– 0,070 mm copper thickness	14 A for 4 s
Long time overload, destructive current	
– 0,035 mm copper thickness	I ≥ 8 A
– 0,070 mm copper thickness	I ≥ 16 A

[a] i.e. in the same layer.

[b] i.e. between opposite layers.

Table 2: Limits of approval and characteristics of finished rigid single-sided and double-sided boards for high frequency application

Item	Limits
Base materials	
(according to ECSS-Q-70, IEC specifications and IPC 4101)	– Random-glass-reinforced PTFE resin with or without Al backing – Woven-glass-reinforced PTFE resin – Ceramic filled woven-glass reinforced PTFE resin – Ceramic filled PTFE resin with or without Al backing – Ceramic filled × linked hydrocarbon/thermo-set polymer – Woven-glass-reinforced epoxy resin FR4 – Quartz filled polyimide resin
Dimensional characteristics	
External dimension tolerance	±0,2 mm
Thickness tolerance	±10 %
Active board size, maximum	TBD by the supplier
Board thickness (minimum/maximum)	TBD by the supplier and customer according to electrical performance
Positioning tolerance between registration mark and edge of circuit	±0,2 mm
Conductor width/spacing	TBD by the supplier and customer according to electrical performance
Tolerance on conductor (minimum/maximum)	TBD by the supplier
Tolerance on diameter of terminal pads	TBD by the supplier and customer according to electrical performance
Minimum hole diameter	
– component hole	According to ECSS Q-70-08
– via hole	0,25 mm minimum and maximum aspect ratio t/d = 6
Tolerance on diameter of plated-through holes	
– nominal Ø ≥ 0,7	Δ maximum 0,15 mm for component hole
– nominal Ø < 0,7	Δ maximum 0,20 mm
Tolerance on diameter of non-plated-through holes	Δ maximum 0,20 mm
Positioning tolerance of holes with respect to reference mark	±0,1 mm
Relative misregistration pad/hole	≤ 0,15 mm
Misalignment determined by measuring minimum annular ring	
– solder side	0,2 mm
– component side (reduced pads)	0,1 mm
– non-soldering hole	0,1 mm

Table 2: Limits of approval and characteristics of finished rigid single-sided and double-sided boards for high frequency application *(continued)*

Item	Limits
Electrolytic coatings	
Electrolytic copper plating	
– minimum purity	99,5 %
– thickness	
• surface pattern for soldering pads	≥ 25 µm (total thickness of basic – plus electrolytic copper ≥ 40 µm)
• plated-through holes	≥ 25 µm
• via hole	≥ 20 µm
Tin lead plating after reflow	
– tin content of alloy	(63 ± 8) %
– thickness on surface	≥ 8 µm in highest part
– thickness in plated-through holes	≥ 8 µm in highest part (minimum half height of hole wall)
– on corner angle	≥ 2 µm
Electrolytic gold plating	
– minimum purity	99,8 % (shall not contain more than 0,2 % silver)
– thickness on nickel	1 µm to 7 µm
Electrolytic nickel plating	Optional under gold
– thickness	2 µm to 10 µm
Mechanical characteristics	
Warp and twist	
– random-glass-reinforced PTFE resin	n.a.
– woven-glass-reinforced PTFE resin	n.a.
– ceramic filled PTFE resin	≤ 1,1 %
– ceramic filled x-linked hydrocarbon/thermoset polymer	≤ 1,1 %
– woven-glass-reinforced epoxy resin FR4	≤ 1,1 % for board thickness ≥1,6 mm ≤ 1,5 % for board thickness <1,6 mm
– quartz filled polyimide	≤ 1,1 % for board thickness ≥1,6 mm ≤ 1,5 % for board thickness <1,6 mm
Conductor adhesion/peel strength	
– on PTFE reinforced/ceramic filled or non-filled	≥ 8 N/cm
– X-linked hydrocarbon	≥ 8 N/cm
– on epoxy	≥ 16 N/cm
– on polyimide quartz	≥ 12 N/cm

Table 2: Limits of approval and characteristics of finished rigid single-sided and double-sided boards for high frequency application *(continued)*

Item	Limits
Pull strength	
– for terminal pads 4 mm Ø on PTFE reinforced/ ceramic filled or non-filled	≥ 60 N
• X-linked hydrocarbon	≥ 60 N
• on epoxy	≥ 140 N
• on polyimide quartz	≥ 60 N
– for terminal pads 2 mm Ø on PTFE reinforced /ceramic filled or non-filled	≥ 12 N
• X-linked hydrocarbon	≥ 12 N
• on epoxy	≥ 35 N
• on polyimide quartz	≥ 20 N
Electrical characteristics	
Insulation resistance	
– intralayer	> 10^4 MΩ
– interlayer	> 10^5 MΩ
Withstanding voltage per mm spacing between conductors	
– intralayer and interlayer	1 000 V r.m.s.
Short time overload	
– 0,009 mm copper thickness	n.a.
– 0,017 mm copper thickness	n.a.
– 0,035 mm copper thickness	7 A for 4 s
– 0,070 mm copper thickness	14 A for 4 s
Long time overload, destructive current	
– 0,009 mm copper thickness	n.a.
– 0,017 mm copper thickness	n.a.
– 0,035 mm copper thickness	I ≥ 8 A
– 0,070 mm copper thickness	I ≥ 16 A
Permittivity	TBD by the supplier and customer according to electrical performance
Loss angle Tg δ	TBD by the supplier and customer according to electrical performance

9.3 Flexible printed boards

These are the minimum requirements acceptable for qualification and procurement of flexible PCBs.

Table 3: Limits of approval and characteristics of finished flexible printed boards

Item	Limits
Base materials (according to ECSS-Q-70, IEC specifications and IPC 4101)	Flexible copper-clad polyimide film
Dimensional characteristics	
External dimension tolerance	±0,4 mm
Thickness tolerance	±20 %
Active board size, maximum	TBD by the supplier
Board thickness maximum	0,4 mm
Positioning between registration mark and edge of circuit	±0,4 mm
Conductor width/spacing	(250 µm/250 µm) minimum
Conductor tolerance (minimum/maximum)	TBD by the supplier
Tolerance on diameter of terminal pads	TBD by the supplier
Minimum diameter of plated-through holes	0,25 mm
Tolerance on diameter of plated-through holes for components:	
- nominal $\varnothing \geq 0{,}7$	Δ maximum 0,15 mm
- nominal $\varnothing < 0{,}7$	Δ maximum 0,20 mm
Tolerance on diameter of non-plated-through holes	Δ maximum 0,20 mm
Positioning of holes with respect to reference mark	±0,10 mm
Relative misregistration pad/hole	±0,15 mm
Registration of sides	±0,10 mm
Cutting of insulation coating tolerance	
- internal cutting	±0,50 mm
Misalignment determined by measuring minimum annular ring	
- solder side	0,25 mm
- reduced terminal pads (oblong)	0,10 mm
- non-soldering holes	0,10 mm
Misalignment of insulation coating determined by measuring rest of metal:	
- plated-through holes	0,15 mm
- non-plated-through holes	0,25 mm
Number of layers	2

Table 3: Limits of approval and characteristics of finished flexible printed boards *(continued)*

Item	Limits
Electrolytic coatings	
Electrolytic copper plating	
– minimum purity	99,5 %
– thickness	
• surface pattern	≥ 25 µm
• plated-through holes	≥ 25 µm
Tin lead plating after reflow	
– tin content of alloy	(63 ± 8) %
– thickness on surface	≥ 8 µm in highest part
– thickness in plated-through holes	≥ 8 µm in highest part (minimum half height of hole wall)
– on corner angle	≥ 2 µm
Mechanical characteristics	
Conductor adhesion/peel strength	≥ 10 N/cm
Pull strength	
– for terminal pads 4 mm Ø	≥ 60 N
– for terminal pads 2 mm Ø	≥ 12 N
Resistance to bending cycles	≥ 250 cycles
Bending test for rigid-flex boards	≥ 25 cycles
Electrical characteristics	
Insulation resistance	
– intralayer	≥ 10^4 MΩ
– interlayer	≥ 10^5 MΩ
– with temperature at 80 °C	≥ 10^2 MΩ
Withstanding voltage per mm spacing between conductors	1 000 V r.m.s.
Short time overload	7 A for 4 s
Long time overload, destructive current	≥ 8 A

9.4 Rigid-flex printed boards

For the minimum requirements acceptable for qualification and procurement of rigid-flex PCBs, the limits of approval and the characteristics of finished boards shall be in accordance with:

- subclause 9.3 Table 3 for the flexible part,
- subclause 9.5 Table 4 for the rigid part.

For the construction of multilayer rigid-flex, the flexible copper clad polyimide film shall be without adhesive.

9.5 Rigid multilayer printed boards

These are the minimum requirements acceptable for qualification and procurement of rigid multilayer PCBs.

Table 4: Limits of approval and characteristics of finished rigid multilayer printed boards

Item	Limits
Base materials	
(according to ECSS-Q-70, IEC specifications and IPC 4101)	- Woven-glass-reinforced epoxy resin - Woven-glass-reinforced polyimide resin - Woven-glass-reinforced bismaleimide/trazine modified epoxy (HTg) resin - Non-woven aramide-reinforced polyimide resin
Dimensional characteristics	
External dimension tolerance	±0,2 mm
Thickness tolerance	±10 %
Maximum active board size	TBD by the supplier
Maximum board thickness	3,2 mm
Positioning between registration mark and edge of circuit	±0,2 mm
Conductor width	
- internal	120 µm minimum
- external	200 µm minimum (for fine pitch 120 µm width is tolerated if less than 5 mm from component pad)
Conductor spacing	
- internal	150 µm minimum
- external	300 µm minimum (for fine pitch 150 µm spacing is tolerated if less than 5 mm from component pad)
Conductor tolerance (minimum/maximum)	TBD by the supplier
Tolerance on diameter of terminal pads	TBD by the supplier
Minimum drilled hole diameter	
- component hole	According to ECSS Q-70-08
- via hole	0,25 mm minimum and maximum aspect ratio t/d = 6
Tolerance on diameter of plated-through holes	
- nominal $\varnothing \geq 0,7$	Δ maximum 0,15 mm for component hole
- nominal $\varnothing < 0,7$	Δ maximum 0,20 mm
Tolerance on diameter of non-plated-through holes	Δ maximum 0,20 mm
Positioning of holes with respect to reference mark	±0,1 mm
Relative misregistration pad/hole	≤ 0,15 mm
Misalignment determined by measuring minimum annular ring	
- external layers	
• solder side	0,20 mm
• component side (reduced pads)	0,10 mm
• non-soldering hole	0,10 mm
- internal layers	50 µm

Table 4: Limits of approval and characteristics of finished rigid multilayer printed boards *(continued)*

Item	Limits
Layer to layer registration	±100 µm
Number of layers	18 maximum
Electrolytic coatings	
Electrolytic copper plating	
– minimum purity	99,5 %
– thickness	
• surface pattern	≥ 25 µm
• plated-through holes	≥ 25 µm
• via holes	≥ 20 µm
Tin lead plating after reflow	
– tin content of alloy	(63 ± 8) %
– thickness on surface	≥ 8 µm in highest part
– thickness in plated-through holes	≥ 8 µm in highest part (minimum half height of hole wall)
– on corner angle	≥ 2 µm
Electrolytic gold plating	
– minimum purity	99,8 % (shall not contain more than 0,2 % silver)
– thickness on nickel	(4 ± 3) µm
– thickness on copper	(5 ± 2) µm
Electrolytic nickel plating	Optional under gold
– thickness	2 µm to 10 µm
Insulation between layers	70 µm minimum
Mechanical characteristics	
Warp and twist	≤1,1 % for board thickness ≥ 1,6 mm ≤1,5 % for board thickness < 1,6 mm
Conductor adhesion/peel strength	
– on epoxy with Tg < 160 °C	≥ 16 N/cm
– on epoxy with Tg > 180 °C	≥ 12 N/cm
– on polyimide	≥ 12 N/cm
– on bismaleimide/trazine modified epoxy HTg	≥ 12 N/cm
– aramide/polyimide	≥ 6 N/cm

Table 4: Limits of approval and characteristics of finished rigid multilayer printed boards *(continued)*

Item	Limits
Bond strength/pull strength	
– for terminal pads 4 mm Ø	
• on epoxy Tg < 160 °C	≥ 140 N
• on epoxy Tg > 180 °C	≥ 80 N
• on polyimide	≥ 80 N
• on bismaleimide/trazine modified epoxy HTg	≥ 60 N
• on aramide/polyimide	≥ 60 N
– for terminal pads 2 mm Ø	
• on epoxy Tg < 160 °C	≥ 35 N
• on epoxy Tg > 180 °C	≥ 20 N
• on polyimide	≥ 20 N
• on bismaleimide/trazine modified epoxy HTg	≥ 12 N
• on aramide/polyimide	≥ 12 N
Electrical characteristics	
Insulation resistance	
– intralayer	> 10^4 MΩ
– interlayer	> 10^5 MΩ
Withstanding voltage per mm spacing between conductors	
– intralayer and interlayer	1 000 V r.m.s.
Short time overload	
– 35 µm copper thickness	7 A for 4 s
– 70 µm m copper thickness	14 A for 4 s
Long time overload, destructive current	
– 35 µm copper thickness	I ≥ 8 A
– 70 µm copper thickness	I ≥ 16 A
Internal short circuit	
– insulation resistance	≥ 10^3 MΩ

9.6 Sequential rigid multilayer printed boards

These are the minimum requirements acceptable for qualification and procurement of sequential rigid multilayer PCBs.

Table 5: Limits of approval and characteristics of finished sequential rigid multilayer printed boards

Item	Limits
Base materials (according to ECSS-Q-70, IEC specifications and IPC 4101)	– Woven-glass-reinforced epoxy resin – Woven-glass-reinforced polyimide resin – Woven-glass-reinforced bismaleimide/trazine modified epoxy (HTg) resin – Non-woven-aramide-reinforced polyimide resin
Dimensional characteristics	
External dimension tolerance	±0,2 mm
Thickness tolerance	±10 %
Maximum active board size	TBD by the supplier
Maximum board thickness	3,2 mm
Positioning between registration mark and edge of circuit	Δ maximum 0,20 mm
Conductor width	
– internal	120 µm minimum
– external	200 µm minimum (for fine pitch 120 µm width is tolerated if less than 5 mm from component pad)
conductor spacing	
– internal	150 µm minimum
– external	300 µm minimum (for fine pitch 150 µm spacing is tolerated if less than 5 mm from component pad)
Conductor tolerance (minimum/maximum)	TBD by the supplier
Tolerance on diameter of terminal pads	TBD by the supplier
Minimum drilled hole diameter	
– component hole	According to ECSS Q-70-08
– via hole	0,25 mm minimum and maximum aspect ratio t/d = 6
– buried via	TBD by the supplier maximum aspect ratio t/d = 6
– blind via produced sequentially	TBD by the supplier maximum aspect ratio t/d = 6
Tolerance on diameter of plated-through holes	
– nominal Ø ≥ 0,7	Δ maximum 0,15 mm for component hole
– nominal Ø < 0,7	Δ maximum 0,20 mm
Tolerance on diameter of non-plated-through holes	Δ maximum 0,20 mm
Positioning of holes with respect to reference mark	±0,10 mm
Relative misregistration pad/hole	≤ 0,15 mm

Table 5: Limits of approval and characteristics of finished sequential rigid multilayer printed boards *(continued)*

Item	Limits
Misalignment determined by measuring minimum annular ring	
– external layers	
• solder side	0,20 mm
• component side (reduced pads)	0,10 mm
• non-soldering hole	0,10 mm
– internal layers	0,05 mm
Layer to layer registration	±100 µm
Number of layers	18 maximum
Electrolytic coatings	
Electrolytic copper plating	
– minimum purity	99,5 %
– thickness	
• surface pattern	≥ 25 µm
• plated-through holes	≥ 25 µm
• via holes	≥ 20 µm
• buried via holes	≥ 18 µm
• blind via holes	≥ 18 µm
Tin lead plating after reflow	
– tin content of alloy	(63 ± 8) %
– thickness on surface	≥ 8 µm in highest part
– thickness in plated-through holes	≥ 8 µm highest part (minimum half height of hole wall)
– on corner angle	≥ 2 µm
Electrolytic gold plating	
– minimum purity	99,8 % (shall not contain more than 0,2 % silver)
– thickness on nickel	(4 ± 3) µm
– thickness on copper	(5 ± 2) µm
Electrolytic nickel plating	Optional under gold
– thickness	2 µm to 10 µm
Resin fill in buried vias	see annex A.2.3 b. 6.
Insulation between layers	70 µm minimum
Mechanical characteristics	
Warp and twist	≤ 1,1 % for board thickness ≥ 1,6 mm ≤ 1,5 % for board thickness < 1,6 mm
Conductor adhesion/peel strength	
– on epoxy with Tg < 160 °C	≥ 16 N/cm
– on epoxy with Tg > 180 °C	≥ 12 N/cm
– on polyimide	≥ 12 N/cm
– on bismaleimide/trazine modified epoxy HTg	≥ 12 N/cm
– aramide/polyimide	≥ 6 N/cm

Table 5: Limits of approval and characteristics of finished sequential rigid multilayer printed boards *(continued)*

Item	Limits
Bond strength/pull strength	
– for terminal pads 4 mm Ø	
• on epoxy Tg < 160 °C	≥ 140 N
• on epoxy Tg > 180 °C	≥ 80 N
• on polyimide	≥ 80 N
• on bismaleimide/trazine modified epoxy HTg	≥ 60 N
• on aramide/polyimide	≥ 60 N
– for terminal pads 2 mm Ø	
• on epoxy Tg < 160 °C	≥ 35 N
• on epoxy Tg > 180 °C	≥ 20 N
• on polyimide	≥ 20 N
• on bismaleimide/trazine modified epoxy HTg	≥ 12 N
• aramide/polyimide	≥ 12 N
Electrical characteristics	
Insulation resistance	
– intralayer	> 10^4 MΩ
– interlayer	> 10^5 MΩ
Withstanding voltage per mm spacing between conductors	
– intralayer and interlayer	1 000 V r.m.s.
Short time overload	
– 0,035 mm copper thickness	7 A for 4 s
– 0,070 mm copper thickness	14 A for 4 s
Long time overload, destructive current	
– 0,035 mm copper thickness	I ≥ 8 A
– 0,070 mm copper thickness	I ≥ 16 A
Internal short circuit	
– insulation resistance	≥ 10^3 MΩ

9.7 Special printed boards

All special board constructions not covered in the previous tables that underwent a qualification programme according to ECSS-Q-70-10.

Annex A (informative)

Inspection of PCBs

A.1 Visual inspection and non-destructive test

A.1.1 Verification of marking

a. Procedure

Each board shall be inspected with the naked eye for correct marking. The marking shall be legible and resistant to test stresses.

b. Nonconformance criteria

Identification impossible	**M**
Marking not conforming to customer specification	**M**
Defects not affecting identifications	**m**

A.1.2 Visual aspects

a. Procedure

Each board shall be inspected by magnification $\leq \times 10$ with suitable lighting conditions to verify that construction and workmanship meet the requirements. In case of any irregularity the area shall be examined under $\times 20$ - $\times 40$ magnification.

b. Nonconformance criteria

1. **General cleanliness and contamination**

Contamination visible to the naked eye and not removable by cleaning according to ECSS-Q-70-08	**M**
Contamination visible to the naked eye but removable by cleaning according to ECSS-Q-70-08	**m**

2. **Substrate**

Not in conformity with suppliers trademark and required quality.	**M**
Scratches cutting glass fibre or leaving marks in the dielectric affecting reliability	**M**
Scratches not affecting reliability	**m**

Dents, crazing and haloing – visible to the naked eye – not visible to the naked eye	 **M** **m**
Non-homogeneity regarding colouring and opacity	**m/M**
Discoloured copper oxide layer on internal layer is acceptable	
Inclusion of foreign matter, blistering or air bubbles – visible to the naked eye – not visible to the naked eye	 **M** **m**
Delamination	**M**
Measling – generalized – localized reducing insulation distance in the outer layer out of tolerance – localized not reducing insulation distance in the same layer out of tolerance	 **M** **M** **m**
Fungus growth	**M**
Delamination of cover lay (flexible PCB)	**m/M**

3. **Non-plated-through holes**

Holes plated unintentionally	**m/M**
Incompletely drilled holes, missing or additional holes	**m/M**

4. **Routing**

Incomplete routing of board, so that dimensional or mechanical requirements are not met	**M**
Random cutting defects acceptable within the dimensional requirements	**m**

5. **Surface metallization**

Conductors or pads not conforming to customer's layout	**M**
Terminal pads or conductors completely or partially missing, cut, forming a short circuit	**M**
Lifting of conductive pattern from substrate	**M**
Scratches exposing copper plating	**M**
Copper or nickel visible on top surface of plated areas	**M**
Large number of superficial scratches not attributed to a manufacturing process evidencing bad workmanship	**M**
Dewetting of solder pads on fused tin lead finish	**M**
Granular aspect of solder pads on fused tin lead finish	**m/M**
Corrosion of copper	**M**
Migration of copper through gold	**M**

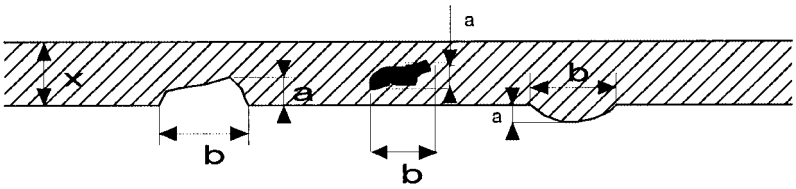
6. **Plated-through holes**

Incompletely drilled, additional or missing holes	**M**
Missing metallization	**M**
Component holes ≥ 0,6 mm filled or partially filled with solder resulting in out of tolerance diameter	**m/M**

7. **Random defects of conductors and terminal pads**

Intermittent and irregular defects which affect metallization, e.g. edge roughness (peak or valley), pits, pin holes, voids, protrusions or indentations.

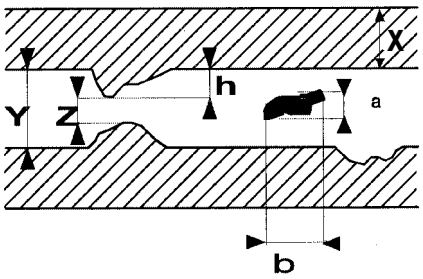
Protrusion or indentations of metallization on conductor edge or voids in conductor as shown in Figures A-1, A-2 and A-3.



x: nominal conductor width

Figure A-1: Random defects of conductors and terminal pads

a ≤ 20 % of x and conductor width > minimum requirement	**m**
a > 20 % of x or conductor width < minimum requirement	**M**
b ≤ x	**m**
b > x	**M**



y: nominal spacing between conductors

Figure A-2: Random defects between two conductors

Opposite peaks: if z < 80 % of y	**M**
Isolated peaks or valleys: h > 20 % of x and z < minimum requirement	**M**
Conducting island: a + h > 20 % of y and the isolation spacing < minimum spacing requirement	**M**
a > 20 % of y or y – a < minimum requirement	**M**
b > y	**M**
Cover lay (flexible PCBs) covering part of solder pad	**M**

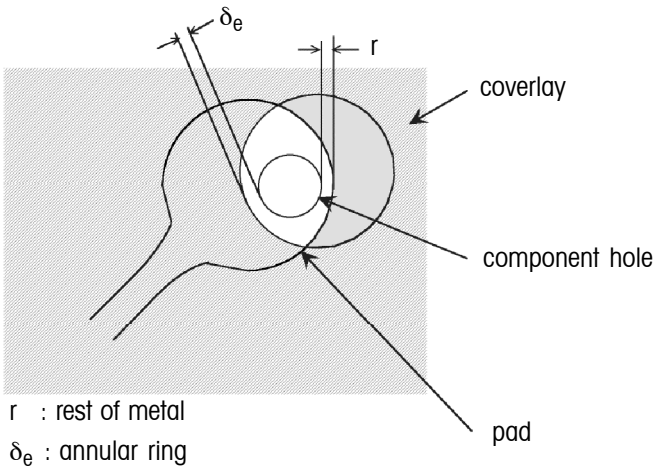


Figure A-3: Misalignment of coverlay

A.1.3 External dimensions

a. Procedure

Each board shall be measured by means of suitable standard measuring equipment to verify that the physical dimensions, including board thickness and external dimensions meet the customer's specifications.

b. Nonconformance criteria

1. Thickness of base laminate
(average of 4 measurements on the board)

If out of tolerance	**M**

2. Length and width of board
(average of 2 measurements on the board)

If out of tolerance	**M**

A.1.4 Warp

a. Procedure

The PCBs shall be placed unrestrained on a plane horizontal surface with the convex side upward. The warp shall be expressed in percentage.

- Measure maximum bow between the plane horizontal surface and the PCB as defined in Figure A-4.
- Measure the length of the PCB.
- Calculate the warp percentage:

$$\text{Warp} \quad \% = \frac{\text{Max. blow in mm}}{\text{Length of the PCB in mm}} \times 100$$

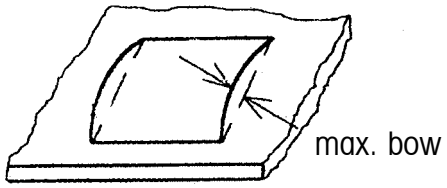


Figure A-4: Warp

b. Nonconformance criteria

If more than maximum bow	**M**

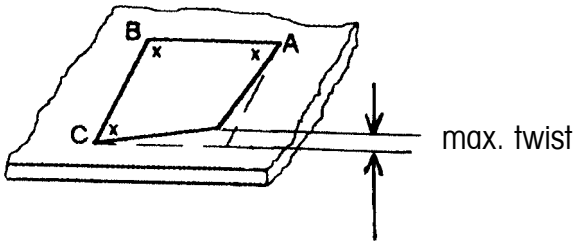
A.1.5 Twist

a. Procedure

The PCB shall be placed on a plane horizontal surface so that it rests on three corners. The height of the remaining corner from the surface shall then be measured (expressed in percentage terms).

- Measure the distance between the plane horizontal surface and the fourth corner of the PCB, as defined in Figure A-5.
- Measure the length of the diagonal.
- Calculate the twist percentage:

$$\text{Twist} \quad \% = \frac{\text{Max. twist in mm}}{\text{Length of the diagonal in mm}} \times 100$$



A, B and C are touching base

Figure A-5: Twist

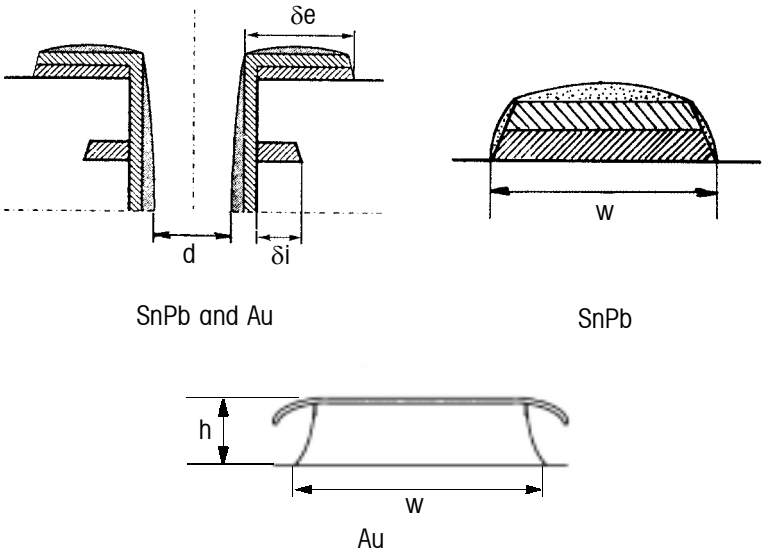
b. Nonconformance criteria

If more than maximum twist	**M**

A.2 Microsection inspection criteria

A.2.1 General

According to tests 1c and 15b of IEC 60326-2-am1 (1992-06), for high frequency conductors the customer shall specify at which height of the conductor the width shall be measured (see Figure A-6).



w	width of conductor
δe	minimum annular ring on external layer
δi	minimum annular ring on internal layer
d	diameter of plated-through hole
h	height of conductor

Figure A-6: Dimensional parameters to be measured

A.2.2 Thickness of metal-plating

a. Procedure

Test carried out on a microsection and observations made with magnification greater than or equal to ×250.

b. Nonconformance criteria

1. **Thickness of copper plating on external layers**

(a) basic copper

Value not conforming to that specified	**M**

(b) basic copper plus electrolytic copper on non-soldering areas

If thickness is less than specified	**M**

(c) basic copper plus electrolytic copper soldering pads (see Figure A-7 number 2)

If thickness < 40 μm	**M**

2. **Thickness of copper in plated-through holes (component holes)**

   Average thickness based on 3 measurements taken on the hole walls (see Figure A-7 number 1)

If less than minimum requirement	**M**

3. **Thickness of copper layer on internal layers**

If not conforming to specified thickness	**M**

4. **Thickness of copper in plated-through holes (via, buried via and blind via)**

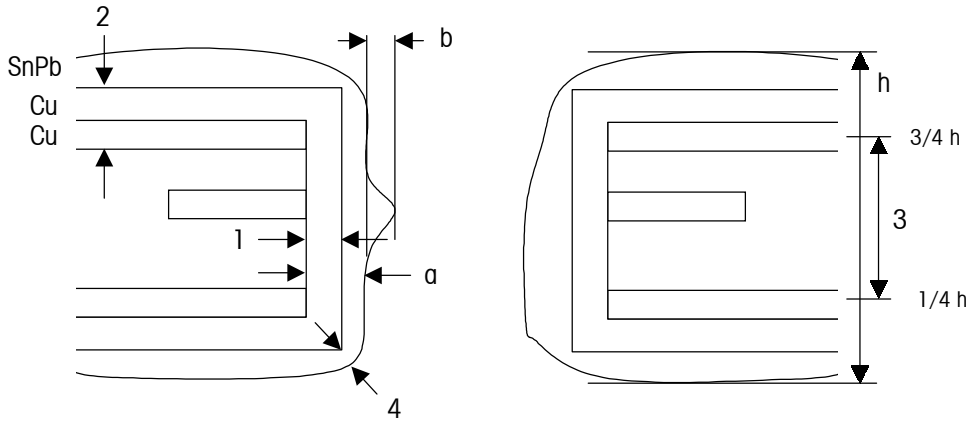
If less than minimum requirement	**M**

5. **Thickness of tin-lead alloy on surface (measured along the conductor longitudinal axis)**

If thickness > 5 µm and < 8 µm	**m**
If thickness < 5 µm	**M**

6. **Thickness of tin-lead alloy in holes**

If thickness < 8 µm in highest part of half of the hole wall height (see Figure A-7 number 3)	**M**
If thickness between 1 µm and 2 µm over angle of hole corner (see Figure A-7 number 4)	**m**
If thickness < 1 µm in angles (see Figure A-7 number 4)	**M**



Key

1 = Cu in PTH

2 = Cu at surface pattern

3 = SnPb in hole

4 = Sn/Pb in angle area

internal bulging b < a

Figure A-7: Microsection of a PTH

7. **Thickness of electrolytic Au or Au/Ni on surface and in holes (measured along the conductor longitudinal axis)**

Au for manual soldering on nickel	
– if thickness < 1 μm	**M**
– if thickness > 7 μm	**M**
Au for manual soldering on copper	
– if thickness < 3 μm	**M**
– if thickness > 7 μm	**M**
Au for high frequency circuits or other assembly methods - as specified by customer	
– if out of specified tolerance	**M**
Ni	
– if thickness < 2 μm	**M**
– if thickness > 10 μm	**M**

8. **Distance between SnPb and Au overlap and the termination pad designated for soldering**

If distance < 200 μm	**M**

9. **Etch undercut for fused SnPb (see Figure A-8) and Au with or without Ni finishes (see Figure A-9)**

External and internal layers	
– if undercut (u) > total copper thickness (h)	**M**
– if undercut (d) > 30 μm for Au with or without Ni finish	**M**

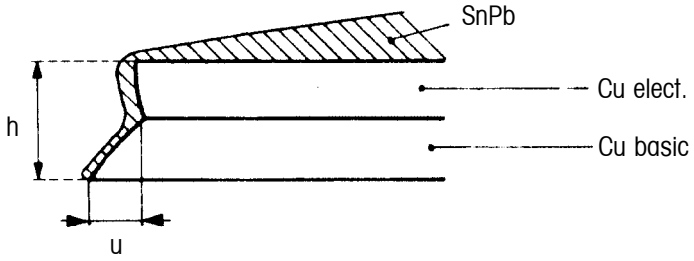


Figure A-8: Undercut for PCBs with fused SnPb finish

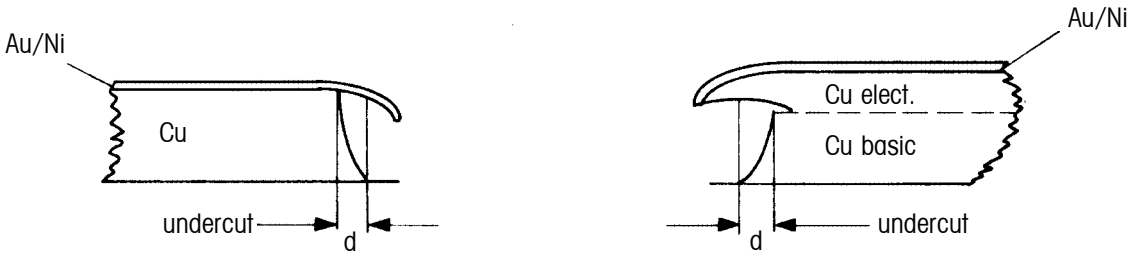


Figure A-9: Undercut for PCBs with Au/Ni or Au finish

10. **Etch overhang for Au with or without Ni finish (see Figure A-10)**

External layers if overhang (D) > 2 × thickness of total copper and Au/Ni or Au	**M**

NOTE For high frequency application overhang is normally undesirable and may be removed mechanically.

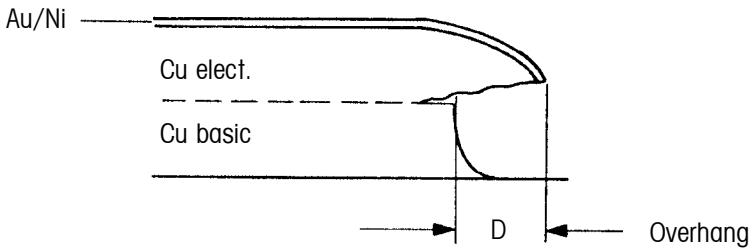


Figure A-10: Overhang for PCBs with Au/Ni or Au finish

A.2.3 Aspect of plated-through holes

a. Procedure

Sections of plated-through holes are observed with magnification greater than or equal to ×100.

b. Nonconformance criteria

Layer misregistration compared to the minimum annular ring on pads.

1. External layer

If δe less than minimum requirement	**M**

2. Internal layer

If δi less than minimum requirement	**M**
If minimum insulation between layers less than minimum requirement	**M**

3. Irregular drilling (see Figure A-11)

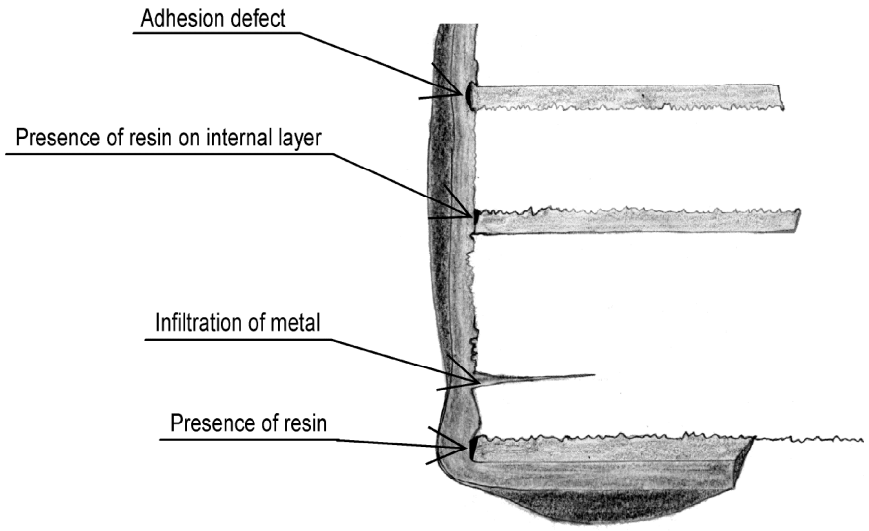
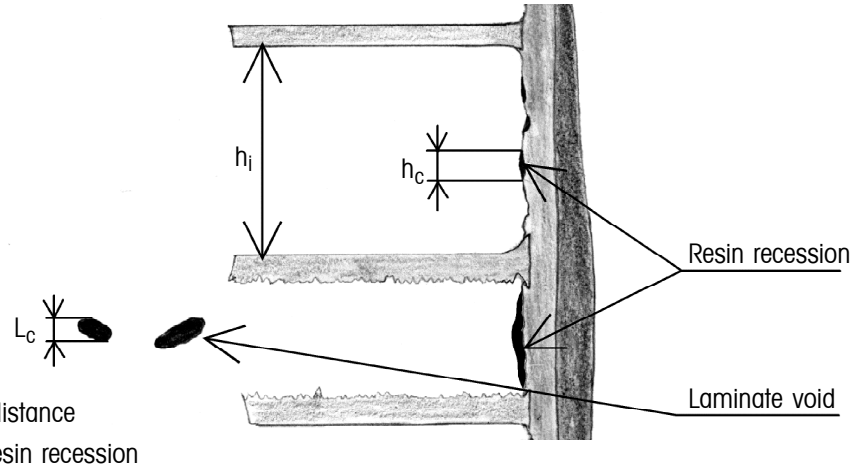


Figure A-11: Microsection in PTH: Possible defects

Infiltration of metal into base laminate - between 40 μm and 80 μm - greater than 80 μm	 **m** **M**
Presence of adhesive on basic copper not leading to rupture during fusing process or thermal shock	**m**
Adhesion defects between metal-plating and basic copper	**M**
Adhesion defects between metal-plating and inner layers	**M**
Resin smear on internal conductor/plated copper interface greater than 15 % of conductor thickness	**M**
Void in resin greater than 50 % of basic copper thickness	**M**

4. Voids in PCB base laminate substrate and resin recession in holes (see Figure A-12)



h_i = insulation distance
h_c = height of resin recession
L_c = size of the void

Figure A-12: Microsection of PTH: Possible defect

Voids in the PCB base laminate substrate and around the metal-plating (resin recession) – if void Lc > 80 μm At edge of metal-plating – if sum of resin recession h_c > 20 % sum h_i	 **M** **M**
Resin recession in hole before or after test – if 10 % of height of hole < resin recession < 20 % of height of hole – if resin recession > 20 % of height of hole	 **m** **M**

5. Copper plating inside buried, blind, via and component holes

Void of copper plating in holes	**M**

6. Resin inside buried vias (see Figure A-13)

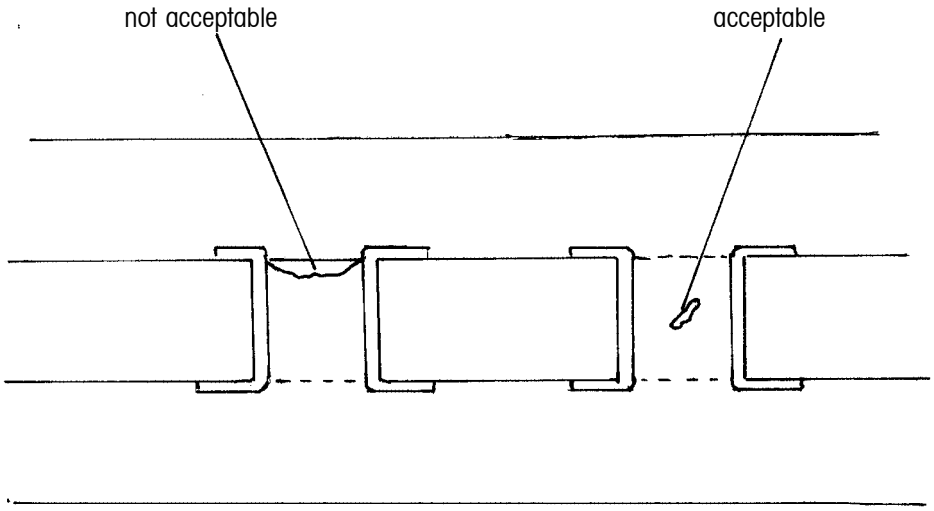


Figure A-13: Voids in resin inside buried vias

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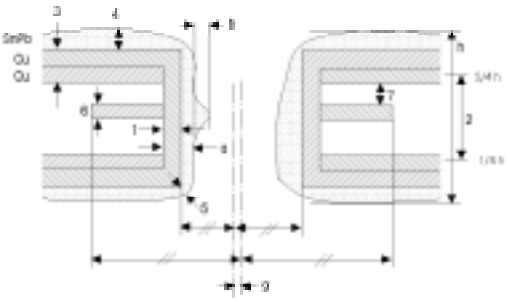
Annex B (informative)

Example of certificate of conformance

Certificate of conformance

Ref. specification:	Order no.:
Customer:	Conf. no.:
PCB no.:	File no.:

Microsection from appropriate test coupon. Result in microns.



	Min.	Max.	Remarks
1. Cu in PTH			
2. Sn/Pb in hole			
3. Cu on surface pattern			
4. Sn/Pb on surface pattern			
5. Sn/Pb in angle area			
6. Cu on internal layers			
7. Insulation distance			
8. Internal bulging b < a			
9. Misregistration			

Visual and dimensional inspection

Examination of base laminate		External dimensions	
Examination of conductive pattern		Dimensions of holes	

Tests

Tape test		Dielectric withstanding voltage 1 000 V AC/mm	
Bond strength		Current carrying capacity 10 A 4 s	
Peel strength		Heat sink high voltage test	
Insulation resistance (-layer):		Solderability	
- Within > 1 000 MΩ at 500 V DC		Thermal stress	
- Between > 100 000 MΩ at 500 V DC		Rework simulation test	
Bow and twist		Flexible test	
		Electrical test	

Remarks:

This is to certify that the material on your subject order, shipped from our plant has been processed, inspected and found in accordance with all specifications referred to on your drawing or purchase order.

We further certify that appropriate records or certificates are on file for your examination upon request.

Inspected QC: Date:	Approved PA: Date:

Figure B-1: Example of "Certificate of conformance"

Bibliography

ECSS-Q-20	Space product assurance — Quality assurance
ECSS-Q-20-09	Space product assurance — Nonconformance control system
IEC 60068-1-am1 (1992-04)	Environmental testing. Party 1: General and guidance
IEC 60194 (1999-04)	Printed board design, manufacture and assembly — Terms and definitions
IEC 60249 series	Base materials for printed circuits
IEC 60326 series	Printed boards
IEC 61249 series	Materials for printed boards and other interconnecting structures
IEC 62326-4 (1996-12)	Printed boards — Rigid multilayer printed boards with interlayer connections - Sectional specification

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ECSS Document Improvement Proposal

1. Document I.D.	2. Document date	3. Document title
ECSS-Q-70-11A	23 November 2001	Procurement of printed circuit boards

4. Recommended improvement (identify clauses, subclauses and include modified text or graphic, attach pages as necessary)

5. Reason for recommendation

6. Originator of recommendation

Name:	Organization:	
Address:	Phone: Fax: e-mail:	**7. Date of submission:**

8. Send to ECSS Secretariat

Name:	Address:	Phone: +31-71-565-3952
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Note: The originator of the submission should complete items 4, 5, 6 and 7.

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http://www.estec.esa.nl/ecss

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