**ECSS-Q-ST-60-05C Rev. 1**
6 March 2009


# Space product assurance

## Generic procurement requirements for hybrids

**ECSS Secretariat**
**ESA-ESTEC**
**Requirements & Standards Division**
**Noordwijk, The Netherlands**

## Foreword

This Standard is one of the series of ECSS Standards intended to be applied together for the management, engineering and product assurance in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards. Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

This Standard has been prepared by the ECSS-Q-ST-60-05 Working Group, reviewed by the ECSS Executive Secretariat and approved by the ECSS Technical Authority.

## Disclaimer



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# Change log

| | |
|---|---|
| ECSS-Q-60-05C<br>7 April 2006 | First issue |
| ECSS-Q-60-05B | Never issued |
| ECSS-Q-ST-60-05C<br>31 July 2008 | Second issue<br>The following editorial changes have been implemented to comply with the ECSS drafting rules:<br>• Terms and definitions have been divided in clauses 3.1 and 3.2.<br>• For synonymous, the ECSS format have been applied (see 3.2.5 and 3.2.6)<br>• When descriptive text and requirements were under the same heading, they have been split in two different headings (see e.g. 6.2.3)<br>• Clarifications to requirements have been presented as NOTES (see e.g. 6.2.1b NOTE)<br>• Each requirement has been given an individual identifier (see e.g. 6.2.1)<br>• Verbal forms have been used consistently, and in conformance with the ECSS drafting rules (see e.g. 6.3.3a)<br>• Headings have been provided for former hanging clauses (see e.g. 8.3.1)<br>• Former normative annexes other than DRDs have been moved to the main text of the standard (see clauses 10.3 and 14)<br>• The appropriate format has been given to the DRDs (see e.g. B.2.1 and B.2.2), and they have been complemented with their introductory material (see e.g. A.1) and with their corresponding special remarks (see e.g. A.2.2).<br>• Only documents explicitly mentioned in the text (other than requirements) have been included in Bibliography. References not explicitly mentioned in the text have been included in informative Annex E “References” |
| ECSS-Q-ST-60-05C Rev. 1<br>6 March 2009 | Second issue revision 1<br>Changes with respect to version C (31 July 2008) are identified with revision tracking. Main changes are:<br>• Various editorial corrections<br>• Adding the following new requirements :6.2.2g, 8.1.2b, 8.2.2b, 9.2b, 10.3.7c<br>• Modifying the following existing requirements: 6.2.2a, 6.2.2b, 6.2.2c, 6.2.2d, 6.2.2e, 7.3.2a.6, 7.3.2b, 10.2.1f.3, 10.2.2b, 10.3.7b, 10.4.2a, 10.4.2b, 10.5.1a, 10.5.2d, 12.1.2b, 12.2.1.3a.1, 12.2.2.4a.1, 14a.6 |

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# Introduction

The objective of this Standard is to define the requirements for the procurement of hybrid microcircuits for use in space systems.

This Standard covers the following requirement domains:

- Validation procedure for a hybrid microcircuit manufacturer.
- Design of hybrid microcircuits.
- Procurement of active and passive chips.
- Procurement of materials and piece parts.
- Screening of hybrid microcircuit lots.
- Lot acceptance tests for hybrid microcircuits.
- Customer involvement, key inspection points.
- Repair provisions.
- Hybrids and data package delivery.

# 1
# Scope

The procurement requirements for hermetic hybrid microcircuits for use in space projects are defined in this Standard.

This Standard also provides details concerning the documentation requirements and the procedures relevant to obtain approval for the use of hybrid microcircuits in the fabrication of space systems and associated equipment.

The provisions of this Standard apply to all participants in the production of space systems, at all levels and are applicable to manned and unmanned spacecraft, launchers, satellites, payloads, experiments, and their corresponding organizations.

This standard may be tailored for the specific characteristic and constraints of a space project in conformance with ECSS-S-ST-00.

# 2
# Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references subsequent amendments to, or revisions of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references the latest edition of the publication referred to applies.

| | |
|---|---|
| ECSS-S-ST-00-01 | ECSS system — Glossary of terms |
| ECSS-Q-ST-60 | Space product assurance — Electrical, electronic and electromechanical (EEE) components |
| ECSS-Q-ST-60-12 | Space product assurance - Design, selection, procurement and use of die form monolithic microwave integrated circuits (MMICs) |
| ECSS-Q-ST-30-11 | Space product assurance — Derating - EEE components |
| ECSS-Q-ST-70 | Space product assurance — Materials, mechanical parts and processes |
| MIL-STD-883G | Tests methods and procedures for microelectronics |
| MIL-STD-750D | Test method standard for semiconductor devices |
| ESCC 20600 | Preservation, packaging and despatch of ESCC components |
| ESCC 2043000 | Internal visual inspection of capacitors |
| ESCC 2044000 | Internal visual inspection of resistors |
| ESCC 2045010 | Internal visual inspection of microwave devices |
| ESCC 2049010 | Internal visual inspection of monolithic microwave devices |
| ESCC 2053000 | External visual inspection of capacitors |
| ESCC 2054000 | External visual inspection of resistors |
| ESCC 2093000 | Radiographic inspection of capacitors |
| ESCC 2094000 | Radiographic inspection of resistors |

# 3
# Terms, definitions and abbreviated terms

## 3.1 Terms from other standards

For the purpose of this standard, the terms and definitions of ECSS-S-ST-00-01 apply.

## 3.2 Terms specific to the present standard

### 3.2.1 approving authority

organization supplying approval certificate

NOTE In Europe the approving authority for space systems components is the ESCC system.

### 3.2.2 category 1 manufacturer

manufacturer with a technology domain approved or pending approval by the **approving authority**

### 3.2.3 category 2 manufacturer

manufacturer with a technology domain not approved by the **approving authority**

### 3.2.4 EM quality level hybrid

**hybrid** manufactured with the same parts (types, sources and design), materials, and processes as flight models but with acceptance of a lower quality level for visual inspection or screening during procurement or manufacturing

### 3.2.5 hybrid

see **"hybrid microcircuit"**

### 3.2.6 hybrid circuit

see **"hybrid microcircuit"**

### 3.2.7 hybrid microcircuit

combination of elements (interconnection substrate, added active or passive chips) sealed inside a package in order to perform an electronic function

NOTE 1 Interconnection substrate (e.g. thick film, thin film, co-fired, DBC) can be with or without integrated passive components (e.g. resistors, inductors, capacitors).

NOTE 2 Active parts can be monolithic or discrete, chips or packaged components.

NOTE 3 Electronic functions that are performed by hybrids include digital or analog, low frequency or radiofrequency, low power or high power functions. These functions may be mixed according to the application.

NOTE 4 The terms "**hybrid circuits**" and "**hybrids"** are synonymous for "Hybrid microcircuits".

### 3.2.8 process identification document

document that defines the approved technology domain, the reference of approval status, and one that freezes the configuration of the manufacturing line and the approved domain

### 3.2.9 process performance index

the long-term capability of the process which reflects the process centering and the variability with respect to specification requirements

### 3.2.10 production lot

number of units of a single device type manufactured on the same production line using the same production techniques, in one uninterrupted period, according to the same component or part design and having the same chips lots and the same materials

### 3.2.11 representative production lot

lot that represents several **production lots** grouping products from the same family, covered by one SEC type, manufactured on the same production line, in one uninterrupted period, using the same materials and processes

### 3.2.12 standard evaluation circuit

device that represents a family of products using the same materials and processes and which is processed on the same production line with the same manufacturing equipment and tools

### 3.2.13 technology review board

formal group at manufacturer level where design, materials and parts procurement, manufacturing, testing, reliability, and quality assurance functions are represented

## 3.3 Abbreviated terms

For the purpose of this Standard, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

| Abbreviation | Meaning |
|---|---|
| **CECC** | CENELEC Electronic Components Committee |
| **CTA** | circuit type approval |
| **COC** | certificate of conformance |
| **DCL** | declared component list |
| **DRD** | document requirements definition |
| **DBC** | direct bonded copper |
| **DPA** | destructive physical analysis |
| **EM** | engineering model |
| **ESA** | European Space Agency |
| **ESCC** | European Space Components Coordination |
| **ESD** | electrostatic discharge |
| **FM** | flight model |
| **FMECA** | failure modes effects and criticality analysis |
| **HTIF** | hybrid circuit technology identification form |
| **LAT** | lot acceptance test |
| **MMIC** | monolithic microwave integrated circuit |
| **MIP** | mandatory inspection points |
| **NCR** | nonconformance report |
| **PA** | product assurance |
| **PAD** | part approval document |
| **PDA** | percent defective allowable |
| **PDR** | preliminary design review |
| **PID** | process identification document |
| **PIND** | particle impact noise detection |
| **Ppk** | process performance index |
| **RFD** | request for deviation |
| **RFW** | request for waiver |
| **SAM** | scanning acoustic microscope |
| **SEC** | standard evaluation circuit |
| **SEM** | scanning electronic microscope |
| **SPC** | statistical process control |
| **TCV** | technological characterization vehicle |
| **TRB** | technology review board |

# 4
# Sequence of procurement activities

The sequences of activities involved in the procurement of hybrid microcircuits are illustrated in Figure 4-1. A more detailed illustration is further provided in Figure 4-2.

The initial steps in the process are the selection and validation of the manufacturer and the technology.

The technology of a hybrid circuit is defined as the set of processes and materials used to manufacture the hybrid, i.e.

- the substrate network and material: thick film or thin film;
- integrated components, i.e. resistors, capacitors and inductors used in the network;
- processes and materials for the attachment and connection of the added-on components (active and passive chips);
- packaging type and material.

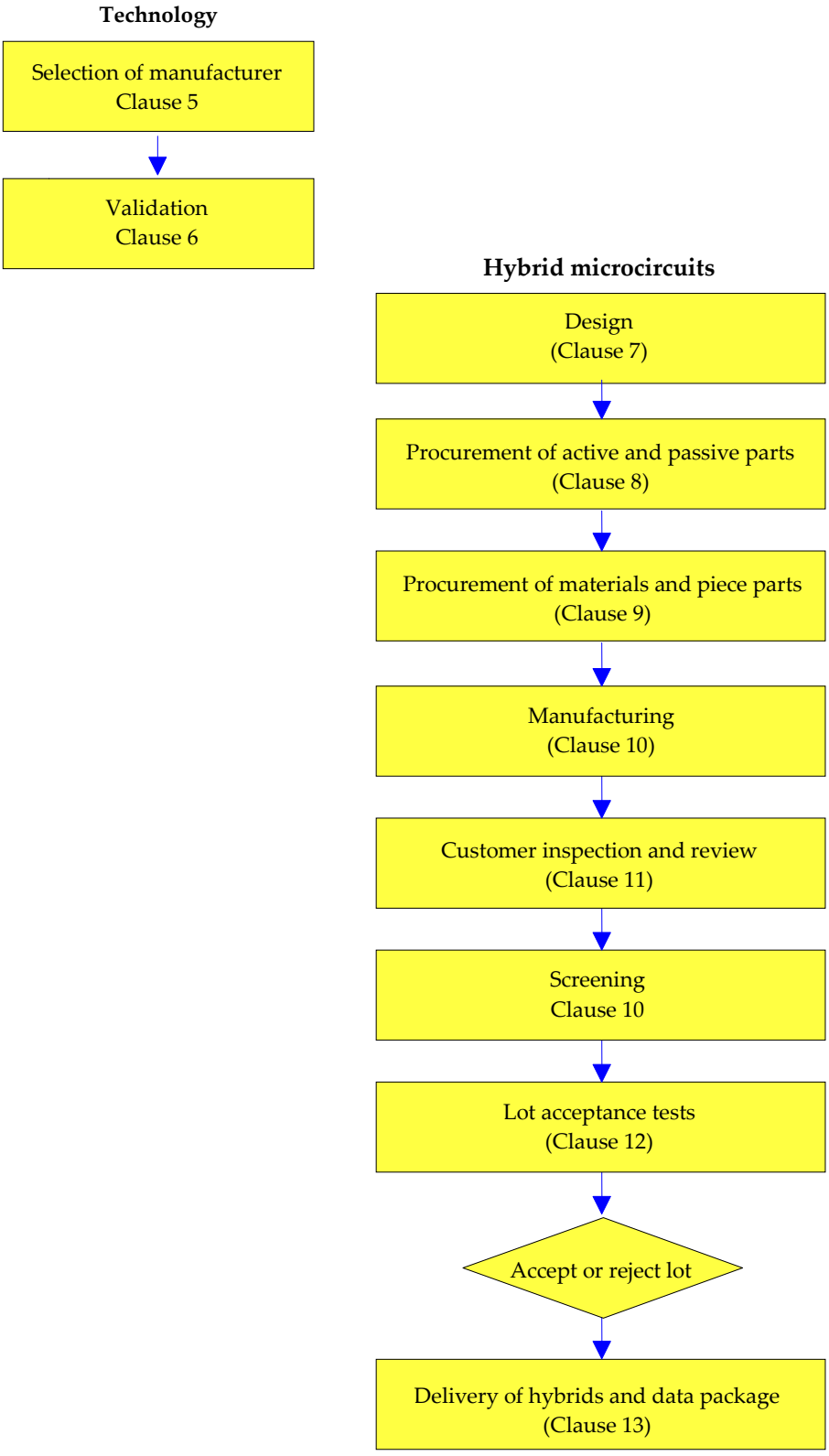



**Figure 4-1: Sequence of activities in the procurement of hybrid microcircuits**

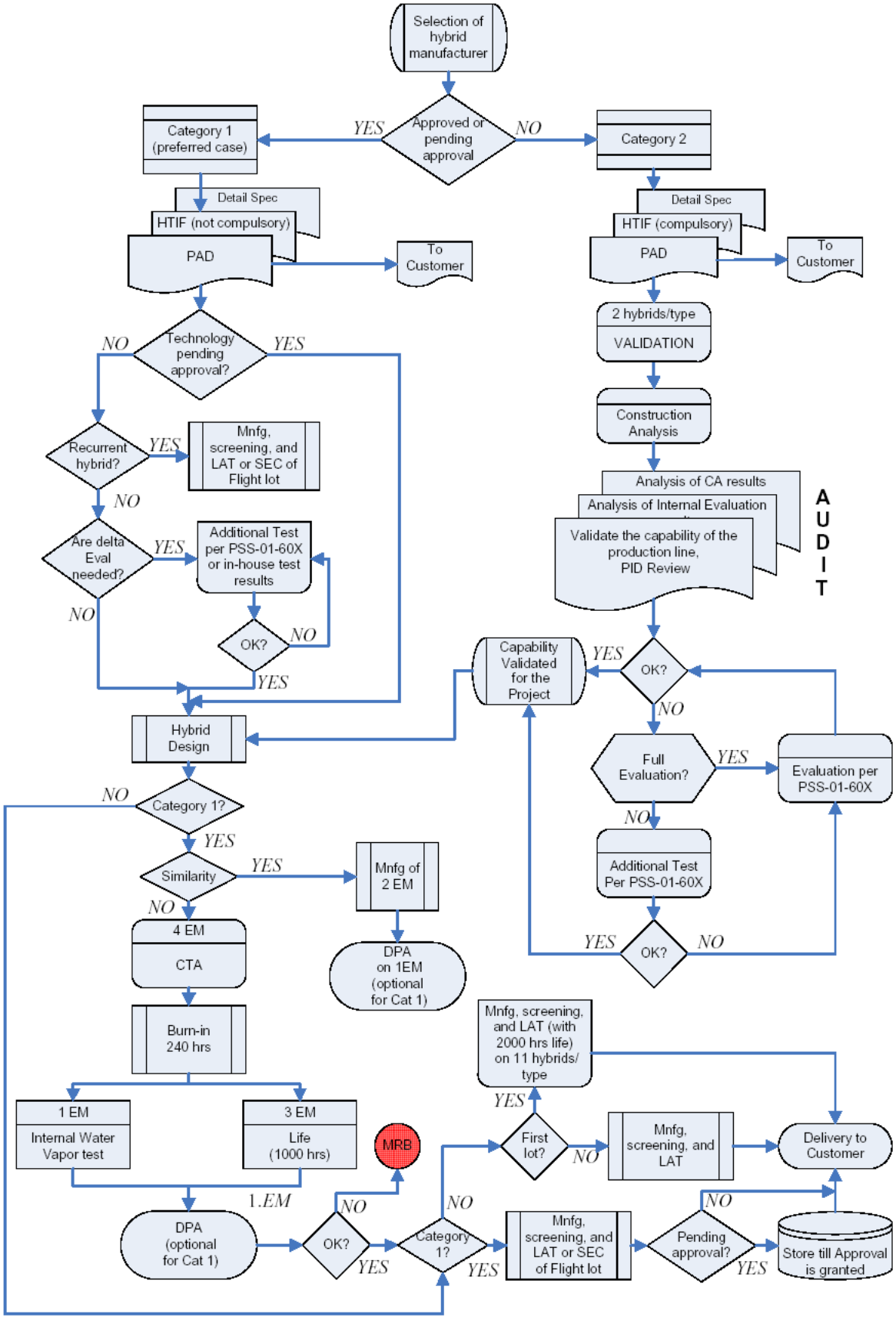



**Figure 4-2: Hybrids procurement flow**

# 5
# Selection of hybrid microcircuit manufacturer

## 5.1 General

a. All manufacturers that are selected for producing hybrids shall be validated as described in Clause 6.

## 5.2 Hybrid microcircuit manufacturer categories

### 5.2.1 Category 1 manufacturer (preferred case)

a. A supplier who wishes to use (or manufacture) hybrid circuits for a space project shall procure (or produce) them from a production line that has been approved or is pending approval by the approving authority.

b. All hybrid circuits shall be manufactured using the basic processes and materials, and in conformance with the manufacturing and inspection procedures as described in the PID that has been approved by the approving authority.

c. The PID shall contain as a minimum:

1. the manufacturing and inspection flow chart;
2. the list of applicable documents with approved revision;
3. the general organization of the production line;
4. the approved domain: authorized parts, materials, processes and reworks;
5. the list of manufacturing, inspection and failure analysis equipment;
6. the list of hybrids manufactured in conformance with the approved PID.

### 5.2.2 Category 2 manufacturer (non-preferred case)

a. A supplier wishing to use (or manufacture) hybrid circuits from a production line that has not been approved by the approving authority shall:

1. justify its requirements to the customer (especially if this involves developing a new circuit), and
2. satisfy the validation conditions described in Clause 6.

# 6
# Validation procedure for a hybrid microcircuit manufacturer

## 6.1 General

a. Validation of manufacturers and production lines shall be conducted jointly by the supplier using the hybrid circuit and the customer, and involving upper level customers where relevant.

b. In the case of confidential information, these activities may be conducted with the support of the approving authority.

## 6.2 Hybrid circuit technology identification form (HTIF)

### 6.2.1 General

a. Whatever his status (category 1 or 2) regarding the capability approval, a manufacturer wishing to produce or use hybrid circuits shall complete a hybrid circuit technology identification form (HTIF) for each circuit, in conformance with Annex A.

b. For category 2 manufacturers, this form shall be included with the part approval document (PAD) as described in 6.2.4.

NOTE The format of the PAD is defined in ECSS-Q-ST-60, Annex A.

### 6.2.2 HTIF for approved manufacturers (category 1)

a. With justification, it is not mandatory, for a category 1 manufacturer, to deliver the HTIF to the customer.

b. A category 1 manufacturer shall issue a CoC to the customer to confirm that the proposed hybrid circuit conforms to the domain approved by the approving authority.

c. As a minimum, the HTIF reference and CoC shall be included in the PAD with reference to the applicable PID.

d. If the technologies used are not entirely covered by the applicable PID, the manufacturer shall carry out additional (delta-)evaluation tests or prove that he has adequate in-house test results.

NOTE See the relevant PSS evaluation plans in ESA-PSS-01-605, ESA-PSS-01-606, and ESA-PSS-01-612.

e. This (delta-)evaluation programme shall be referenced in the PAD.

f. The test results shall be approved by the first level supplier.

g. The manufacturer shall supply these circuits according to the procurement rules defined for the project as per the requirements in this standard.

### 6.2.3 HTIF for manufacturer pending capability approval by the approving authority (category 1)

#### 6.2.3.1 Overview

Manufacturers of hybrid circuits are considered to be pending capability approval by the approving authority when:

- they have successfully completed the "evaluation" phase,
- their PID has been approved, and
- they have begun the "approval" phase (see ESA-PSS-01-605, ESA-PSS-01-606, and ESA-PSS-01-612).

#### 6.2.3.2 Requirements

a. Manufacturers shall only use the technologies that have been tested in the evaluation phase and are referenced in the PID.

b. Manufacturers may manufacture circuits while the approval phase is being carried out in conformance with the PID.

c. Manufacturers shall not deliver these circuits until capability approval has been formally acquired.

### 6.2.4 HTIF for manufacturer not approved by the approving authority (category 2)

#### 6.2.4.1 Overview

For category 2 manufacturers, the review and validation activities for the production lines are described in clause 6.3.

#### 6.2.4.2 Requirements

a. The review and validation activities for the production lines for category 2 manufacturers shall be implemented at the PDR milestone of the project.

b. A category 2 manufacturer shall supply an HTIF in conformance with Annex A and include it as part of the PAD.

c. In case of confidentiality of particular materials or processes, claimed by category 2 manufacturers, the HTIF attached to the PAD may leave undisclosed the confidentiality elements, provided that these aspects are covered and discussed during the quality and technical audit as described in clause 6.3.3.

d. The HTIF shall be in conformance with the technological domain validated for the project.

e. The manufacturer shall produce the hybrid circuits for the project which conform to the same common requirements as for category 1 manufacturers and additional requirements as defined in this Standard.

## 6.3 Validation of category 2 manufacturers

### 6.3.1 General

a. Category 2 manufacturers shall be validated in conformance with the requirements in this clause 6.3.

### 6.3.2 Construction analysis on representative samples

a. Two circuits per hybrid type shall be supplied by the supplier for construction analysis.

b. The quality level of these circuits shall be the same as the one specified by the project.

### 6.3.3 Quality and technical audit

a. After construction analysis, a quality and technical audit shall be carried out by the supplier as follows:

1. Present the results of the construction analysis.

2. Analyse the results of internal evaluations of the technologies implemented by the manufacturer. Compare these previously obtained results to the tests defined in the evaluation plans (see ESA-PSS-01-606, ESA-PSS-01-605, and ESA-PSS-01-612), and apply the following criteria.

(a) If the results of the tests are successful, consider the manufacturer “validated”, but only for the project.

(b) If only some of the results are successful, perform additional tests pertaining to the failures (see the evaluation plans ESA-PSS-01-606, ESA-PSS-01-605, and ESA-PSS-01-612).

(c) If all the results are unsuccessful, draw up a completely new evaluation plan (see ESA-PSS-01-606, ESA-PSS-01-605, and ESA-PSS-01-612).

3. Judge the validity of manufacturer's in-house data in conformance with the following criteria:

   (a) Equivalence of the test structure(s) subjected to the in-house evaluation tests and the hybrid circuits proposed by the project, this "equivalence" including assessment of the following:

   – technology of the circuit,

   – circuit function,

   – circuit complexity,

   – power dissipation.

   – Comparison between the in-house evaluation tests and the reference evaluation plans with respect to the severity of the tests (e.g. level, duration, temperature) and the accept or reject criteria applied.

4. Validate the capability of the production line to meet the quality requirements of the project and ensure the following:

   (a) The components, materials and processes used are governed by specifications written, approved by the manufacturer's quality control departments and that this documentation is applied at the time of the manufacturer's in-house evaluation tests.

   (b) The quality control operations on the production line conform in frequency and severity to the "high reliability" requirements.

   (c) The traceability of the finished product and its component parts is guaranteed by the manufacturer and can be used by the customer.

   (d) All the documentation relating to production and quality assurance specified in the process identification document (PID) is approved by the customer.

   NOTE For guidelines for carrying out such audits see ESA-PSS-01-607 and ESA-PSS-01-611.

# 7
# Design requirements

## 7.1 General

### 7.1.1 Overview

The "design" of a hybrid circuit includes the initial activities to be undertaken by a manufacturer in order to implement specific electrical functions, derived from a circuit diagram, in a finished hybrid.

### 7.1.2 Design activities

a. The design activities of a hybrid circuit shall, as a minimum, include the following:

   1. Selection of technology.
   2. Selection of added-on components, i.e. defining the types of chip components used in the hybrid and their manufacturers.
   3. Definition of the physical layout of the hybrid circuit, i.e. the interconnections in the hybrid to enable the electrical function.
   4. Application of the derating requirements in conformance with ECSS-Q-ST-30-11.
   5. Implementation of the thermal management criteria in the case of power circuits.
   6. Mechanical, dimensional verification.
   7. Verification of the radiation related requirements for the added-on components and the whole hybrid circuit.
   8. The activities requested by the customer to ensure that the predicted failure rate of the hybrid circuit is compatible with the reliability target of the equipment concerned (FMECA, reliability calculation and worst case analysis).

b. When selecting the technology in conformance with 7.1.2a.1, the technology shall be as specified in the PID and described in the hybrid technology identification form (HTIF) specified in Annex A.

c. When selecting the added-on components in conformance with 7.1.2a.2, the selection shall conform to the requirements specified in the PID.

d. When defining the physical layout of the hybrid circuit in conformance with 7.1.2a.3, the layout of the hybrid circuit shall conform to the design rules defined in the specification called up by the approved PID.

## 7.2 Detail specification for hybrid circuits

a. A detail specification for each type of hybrid circuit shall be drawn up in conformance with Annex B.

b. The maximum rating and drifts of electrical parameters shall be established from the following:

1. the detail specification for the chip components,

2. the results obtained on prototypes and engineering models.

c. The manufacturer shall demonstrate the consistency between the maximum ratings and drifts specified for the hybrid circuit and those for each of the chip components.

d. Any deviations in the burn-in and life test temperatures as specified in the detail specification (Annex B) shall be subject to a request for deviation.

## 7.3 Design approval (circuit type approval)

### 7.3.1 General

#### 7.3.1.1 Overview

The procedure for design approval of a hybrid circuit depends on the following:

- Its “non similarity” to a circuit developed or being developed for the project, or a circuit already developed and approved within the framework of a previous project.
- Its “similarity” to a circuit developed or being developed for the project, or a circuit already developed and approved within the framework of a previous project.
- The “recurrence” of a circuit which has already been used (developed, approved, manufactured) within the framework of a previous project.

#### 7.3.1.2 Requirements

a. Similarity shall be proposed by the manufacturer to the customer by using a similarity form in conformance with Annex C.

NOTE Similarity is assessed on the basis of the HTIF and this similarity form.

b. The similarity form shall be enclosed with the request for use (PAD).

### 7.3.2 Procedure for a new hybrid circuit which is "non similar" to a reference circuit

a. The procedure for the design approval for a new circuit which is not similar to an approved circuit shall respect the following:

1. Manufacture four hybrids with, as a minimum, an EM quality level.
2. Take electrical measurements at ambient temperature in conformance with Tables 2 and 4 of the detail specification provided in Annex B.

   NOTE Table 3 is optional.
3. Subject the four hybrids to burn-in over a period of 240 h in conformance with Table 5 of the detail specification provided in Annex B.
4. Take electrical measurements in conformance with Tables 4, 2 and 3 of the detail specification provided in Annex B.
5. Measure the internal water vapour content of one hybrid in conformance with MIL-STD-883 method 1018, taking as acceptance criterion: $5\,000 \times 10^{-6}$ parts water vapour maximum at 100 °C.
6. Perform a DPA on the hybrid submitted to 7.3.2a.5 in conformance with clause 14.
7. Analyse the observed defect to determine its cause

   NOTE For example, basic technology, component quality, design.

   (a) No failure allowed.

   (b) For category 1 manufacturers the DPA is optional.
8. Perform a life test shall for a duration of 1 000 h on three hybrids, in conformance with Table 7 of the detail specification provided in Annex B.
9. Take electrical measurements in conformance with Tables 2, 3 and 6 of the detail specification provided in Annex B.

   (a) No failure allowed.
10. Perform a DPA on one of the three hybrids submitted to life test.

    (a) No failure allowed.

    (b) For category 1 manufacturers the DPA is optional.

    NOTE CTA can be performed on the first flight model hybrid providing project agreement.

b. To perform the internal water vapour content measurement in conformance with 7.3.2.a.5, a screening reject may be used.

### 7.3.3 Procedure for a new hybrid circuit which is "similar" to a reference circuit

a. The procedure for the design approval of a new hybrid which is similar to an approved circuit shall be as follows:

1. Manufacture two hybrids with, as a minimum, an EM quality level.
2. Take electrical measurements in conformance with Tables 2 and 3 of the detail specification provided in Annex B.
   (a) No failure allowed.
3. Perform a DPA shall be performed on one of the two hybrids,
   (a) No failure allowed.
   (b) For category 1 manufacturers the DPA is optional.

### 7.3.4 Procedure for a "recurrent" hybrid circuit

a. A hybrid circuit shall be considered to be "recurrent" when the following conditions apply:

1. Its design has already been approved without any deviations (in conformance with the procedures described in clause 7.3.2 or 7.3.3) for a previous project.
2. Its FM version has the same references, detail specification, HTIF and list of chip component suppliers (if not included in the HTIF) as the flight hybrid produced within the framework of a previous project, taking into account alerts and deviations.
3. Its conditions of use and constraints are similar in nature and severity to those for a previous project.

b. A "recurrent" hybrid circuit may be manufactured without any further design validation.

c. If one of the conditions described not be met, the design shall be approved in conformance with clause 7.3.2 or 7.3.3.

d. The customer may reject the case for a recurrent circuit if the information supplied is considered to be inadequate.

# 8
# Procurement of passive and active chips

## 8.1 General

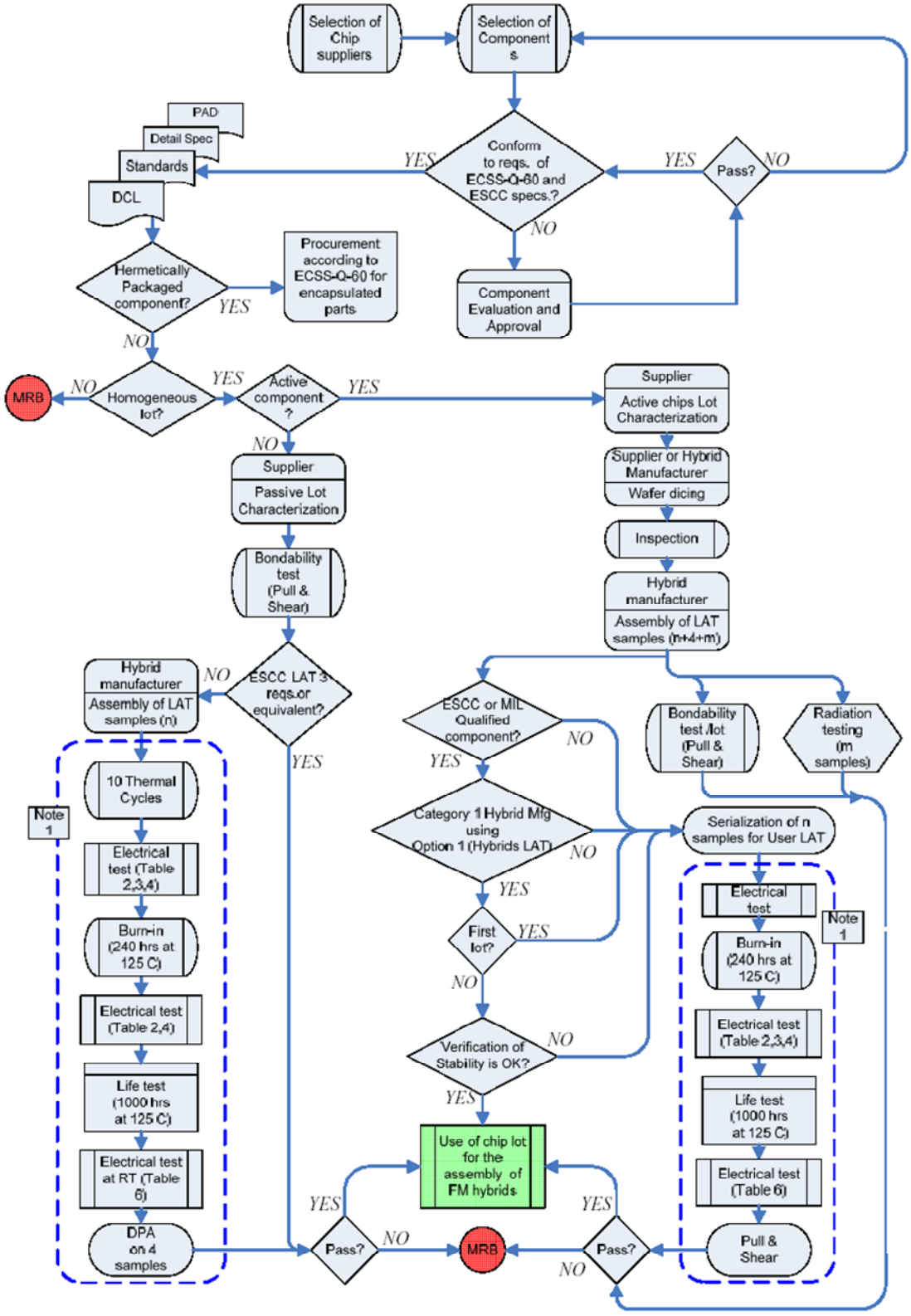
### 8.1.1 Introduction

The procurement of add on parts is detailed below. The flow for chip components is illustrated in Figure 8-1.

Active and passive chips form a subset of all electronic components.

Active chips are diodes, transistors, and integrated circuits supplied in the form of bare chips.

The most commonly used passive chips include resistors, capacitors and inductors.




NOTE: The tests inside the dashed area can be carried out by a supplier under the responsibility of the hybrid manufacturer.

**Figure 8-1: Flow of Procurement of Active and Passive components**

### 8.1.2 Selecting chip suppliers

a. The manufacturer of the hybrid shall ensure that the selected component manufacturers conform to the component selection requirements of ECSS-Q-ST-60 and the ESCC specifications.

b. Design and procurement of MMIC dies shall be done in conformance with ECSS-Q-ST-60-12.

c. The chip component supplier can be either the chip manufacturer or a "chip processor" approved by the hybrid manufacturer.

d. For chip components which are qualified in an "encapsulated version", it is the responsibility of the hybrid manufacturer to verify that "qualified chip components" are procured.

e. If non-qualified components are procured, a component evaluation and approval testing programme shall be implemented in conformance with the component approval requirements of ECSS-Q-ST-60.

f. It is the responsibility of the hybrid manufacturer to demonstrate that the procured chips are reliable in the hybrid environment, i.e. the materials and processes used are compatible.

### 8.1.3 Specifications

a. Existing European components specification systems, i.e. ESCC and CECC or equivalent MIL, should be used.

b. Whenever a new procurement specification is established, it shall conform to one of the existing European standardization systems.

c. All components shall be procured in conformance with the specifications in the PID and listed in the DCL, and all specifications shall be subject to configuration control.

d. The detail specifications for the chip components shall include the electrical parameters that have been verified during the lot characterization tests, the screening conditions, and life tests as well as aspects such as size and chip mask, when applicable.

### 8.1.4 Requirements for chip lots

a. All chips shall be procured as traceable homogeneous lots, defined as follows:

   1. For active chips, a homogenous lot is defined as a unique lot with respect to diffusion, metallization and passivation processes.

   2. For passive chips, a homogeneous lot is defined as a unique lot with respect to firing or metallization.

## 8.2 Procurement of passive chips

### 8.2.1 General

a. Each lot of passive chips shall be characterized by the supplier as follows and checked and accepted by the customer:

   1. Conformance of the passive chip to its detail specification (e.g. size, terminations).

   2. Traceability and homogeneity of the lot.

   3. 100 % electrical measurements at ambient temperature.

   4. 100 % visual inspection in conformance with ESCC 2043000, ESCC 2053000, ESCC 2093000, ESCC 2044000, ESCC 2054000, ESCC 2094000 or MIL-STD-883 method 2032 or equivalent.

b. For each lot of passive chips, a sample shall undergo a bondability test and a lot acceptance test.

### 8.2.2 Bondability test

a. The bondability test shall be performed on four chips per lot, or ten chips per family, assembled by the hybrid manufacturer, using its materials and processes.

b. If wire bonding is used a minimum of 22 wires shall be tested.

   NOTE If bimetallic bonding (Au-Al) is used 8.3.2.c applies

c. A shear test shall then be performed on all the chips.

d. Results shall conform to MIL-STD-883 method 2011 for bond pull strength and MIL-STD-883 method 2019 for die shear strength, with no failure allowed.

### 8.2.3 Lot acceptance test (LAT)

a. Lot acceptance test (LAT) requirements shall be selected depending on the origin of the passive chips, as follows:

   1. For ESCC or MIL-equivalent qualified, screened and burned-in passive chips, only ESCC LAT 3 requirements or equivalent are applicable.

   2. For all other cases, ensure that a sample batch of “n” chips is assembled by the hybrid manufacturer with its materials and processes, and the following sequence of tests is performed either by the manufacturer, or by a subcontractor under the responsibility of the manufacturer:

      (a) Perform thermal cycling (10 cycles) in conformance with MIL-STD-883 method 1010 condition B, if this was not already performed during the screening tests.

(b) Take electrical measurements before burn-in in conformance with Tables 2, 3 and 4 of the passive chip detail specification provided in Annex B and ensure that the maximum number of rejects is as given in Table 8-1.

(c) Subject the samples to burn-in over a period of 240 h at 125 °C.

(d) Take electrical measurements at ambient temperature and the drift values calculated in conformance with Tables 2 and 4 of the passive chip detail specification, and ensure that the maximum number of rejects is as given in Table 8-1.

(e) Perform a life-test for a period of 1 000 h at 125 °C.

(f) Take electrical measurements at 25 °C in conformance with Table 6 of the passive chip detail specification, and ensure that no failure occurs.

(g) Perform a DPA on four samples after the life-test as defined below, and ensure that no failure occurs:

- a visual inspection in conformance with MIL-STD-883 method 2032;
- a wire pull test in conformance with MIL-STD-883 method 2011;
- a shear test on chips in conformance with MIL-STD-883 method 2019 or in conformance with the PID.

b. The LAT acceptance criteria shall be as given in Table 8-1.

**Table 8-1: Sample size and acceptance criteria for LAT of passive chips**

| "n" samples | Number of defects allowed after: | | | Number of accumulated defects for: | |
|---|---|---|---|---|---|
| | Electrical test | Burn-in | Life test | Rejection | Acceptance |
| 18 | 1 | 1 | 0 | 2 | 1 |
| 11 | 0 | 0 | 0 | 1 | 0 |

## 8.3 Procurement of active chips

### 8.3.1 General

a. Each lot of active chips shall be characterized by the supplier as follows and checked and accepted by the customer:

1. Conformance of the active chip to its detail specification (e.g. size, masks).
2. Traceability and homogeneity of the lot.
3. 100 % probe testing of the wafers at 25 °C and marking of chips that do not conform.

4. Visual inspection of the wafer in conformance with:
   (a) MIL-STD-883 method 2010 condition A or B (integrated circuits);
   (b) MIL-STD-750 methods 2072 and 2073 (diodes and transistors).
5. SEM inspection in conformance with the component technology (i.e. in case of metallization over oxide steps).

b. Once the wafer has been scribed and diced, a 100 % visual inspection shall be carried out on the chip supplier's premises or as part of the hybrid manufacturer's incoming inspection in conformance with the following:
   1. MIL-STD-883 method 2010 condition A (integrated circuits), ESCC 2045010 (microwave devices), ESCC 2049010 (monolithic microwave devices).
   2. MIL-STD-750 methods 2072 and 2073 (diodes and transistors).

c. When radiation lot acceptance is considered necessary for a part in packaged form (lot by lot variability components), the same policy shall be applied for the part in die form.

d. For each lot of active chips, a sample shall undergo a bondability test and customer lot acceptance test (user LAT).

### 8.3.2 Bondability test

a. The bondability test shall be performed on four chips assembled by the hybrid manufacturer with its materials and processes.

b. A bond pull strength test shall be performed on 22 wires (or all the wires if less) and a shear test on the four chips.

c. For bimetallic bonding (gold-aluminium) ageing (1 h at 300 °C or the equivalent time-temperature combination with a 0,92 eV activation energy basis) shall be performed before the pull test.

d. Results shall conform respectively to MIL-STD-883 method 2011 for bond pull strength and MIL-STD-883 method 2019 for die shear strength, with no failure allowed.

### 8.3.3 User LAT

#### 8.3.3.1 Overview

User LAT is the performance of burn-in or life test and electrical measurements in order to verify the electrical characteristics of the chip lot when the chip is assembled with the hybrid manufacturer processes and package environment (which can be different from the chip manufacturer processes).

#### 8.3.3.2 User LAT requirements

##### 8.3.3.2.1 Qualified (ESCC or MIL) parts (family or type in packaged or non-packaged form)

a. User LAT shall be performed for the first lot procured in conformance with Table 8-2.

b. For the subsequent lot, and in the case of good results on the first lot, the hybrid manufacturer shall verify the stability of the front-end manufacturing.

c. If this verification is satisfactory, a user LAT may be deleted providing that the option 1 lot acceptance testing is performed at a hybrid level.

##### 8.3.3.2.2 Non-qualified parts:

a. User LAT shall be performed on each lot in conformance with Table 8-2.

##### 8.3.3.2.3 MMIC dies

a. User LAT shall be performed either on actual MMICs or on TCVs (technological characterization vehicles present on the same wafer of the MMICs) providing that these TCV dies are designed in conformance with the design manual of the MMIC foundry.

##### 8.3.3.2.4 General

a. User LAT shall be performed, for each type of active chip and for each lot, on a batch of "n" assembled and encapsulated samples.

b. The values for "n" and the acceptance criteria are given in Table 8-2.

**Table 8-2: Sample size and acceptance criteria for user LAT on active chips**

| "n" samples | Number of failures allowed for: | | | Number of accumulated failures for: | |
|---|---|---|---|---|---|
| | Electrical test [a] | Burn-in | Life test | Rejection | Acceptance |
| 38 | 3 | 2 | 0 | 4 | 3 |
| 25 | 2 | 1 | 0 | 3 | 2 |
| 18 | 1 | 1 | 0 | 2 | 1 |
| 11 | 0 | 0 | 0 | 1 | 0 |

[a] Defects due to the assembly process are not be considered to be a failure.

c. After encapsulation, the sample batch of "n" chips shall be subjected, either by the hybrid manufacturer or by a subcontractor under his/her responsibility, to the following procedure:

1. Serialization.

2. Take electrical measurements at ambient temperatures in conformance with Table 2 of the chip detail specification.

NOTE Table 3 optional.

3. Take electrical measurements before burn-in in conformance with Table 4 of the chip detail specification, values shall be recorded.
4. Subject the samples to burn-in over a period of 240 h at 125 °C in conformance with the chip detail specification.
5. Take electrical measurements at ambient and extreme temperatures in conformance with Tables 2 and 3 and the drift calculated in conformance with Table 4 of the chip detail specification, with the maximum number of rejects allowed given in Table 8-2.
6. Perform a life-test for a period of 1000 hours at 125 °C in conformance with the chip detail specification.
7. Take electrical measurements in conformance with Table 6 of the chip detail specification with the maximum number of rejects allowed given in Table 8-2.
8. Perform a wire pull test in conformance with MIL-STD-883 method 2011 on 22 wires or on all the wires if less, with no failure allowed.
9. Perform a shear test on the assembled chips in conformance with MIL-STD-883 method 2019 on 4 chips, with no failure allowed.

## 8.4 Procurement of hermetically encapsulated chips

a. Hermetically encapsulated chips shall be fully characterized, screened and tested before being mounted on the film network.

b. The hermetically encapsulated components to be used on hybrids shall be procured in conformance with component selection requirements of ECSS-Q-ST-60, or fully tested and screened in conformance with a procedure that is agreed upon by the approving authority during capability approval, and specified in the PID.

c. Assembly tests of the packaged component shall be performed as specified in the PID.

# 9
# Procurement of materials and piece parts

## 9.1 Overview

Materials and piece parts include:

- Package, lid and cover,
- Interconnection substrate,
- Attachment medium,
- Wires and ribbons,
- Carriers and mechanical parts.

## 9.2 Selection of materials and piece parts

a. The hybrid manufacturer shall ensure that the selected materials and piece parts conform to the "Material control" requirements in ECSS-Q-ST-70.

b. Pure Tin (≥ 97 %) shall not be used on internal and external elements of the hybrid, this includes underplating.

c. The hybrid manufacturer shall demonstrate that the procured materials and piece parts have no impact on the reliability of the passive and active parts in the hybrid environment.

## 9.3 Specifications

a. All materials and piece parts shall be procured in conformance with the specifications in the PID.

b. All specifications shall be subjected to configuration control.

c. The procurement specification of materials and piece parts shall include, as a minimum, the following:

1. The physical and chemical characteristics guaranteed by the supplier with reference to the test methods.
2. The outgoing tests performed on each lot by the supplier with reference to the test methods and acceptance criteria.
3. The provisions for lot definition and traceability.
4. The delivery conditions.

d. Whenever a new procurement specification is established, it shall conform to a European standardization system.

## 9.4 Requirements for materials and piece parts

a. All materials and piece parts shall be procured as traceable homogeneous lots.

b. The definition of the materials and piece parts shall be specified in the procurement specification.

c. Each material and piece part shall be submitted to an incoming inspection procedure, which defines the inspections and tests to be carried out to verify the characteristics guaranteed by the supplier (confidence test) and to verify the compatibility of the item with the hybrid application (user tests).

# 10 Manufacturing and screening of hybrid circuit lots

## 10.1 Manufacturing

a. All manufacturing and inspection operations shall be conducted in conformance with the corresponding manufacturer PID.

## 10.2 Marking

### 10.2.1 General

a. Marking shall be on the body of the hybrid circuit.

b. Apart from serialization, all marking shall be clearly visible when normal mounting procedures are followed.

c. If a hybrid is too small to accommodate all marking, the device shall show, as a minimum, the polarity or lead identification and as much marking as is possible in the prescribed order of precedence as defined in 10.2.1f below.

d. Any marking that cannot be accommodated on the cases themselves shall be shown on the individual containers, excluding the serial numbers, which shall be shown on a tag attached to one of the leads.

e. Marking shall remain legible after all the tests specified in this Standard have been performed and shall withstand all solvents used in conformance with MIL-STD-883 method 2015.

f. Each hybrid circuit shall be marked with the following information in the given order of precedence:

1. Polarity or lead identification as defined in its detail specification specified in Annex B.

2. Part number as defined in its detail specification specified in Annex B, followed by the suffix 1 or 2, depending on the testing level.

3. Manufacturing date code, a 4 digit code used where: the first two digits are the last two digits of the calendar year: the last two digits are the number of the week in which the hybrid was encapsulated

4. For testing level 1, the serial number, consisting of a sequential number of two or more digits for each selected sub-lot.

5. Manufacturer's name, symbol or trade mark.

g. The production lot number may be also marked.

h. The serial number specified in 10.2.1f.4_shall not be duplicated when more than one selected sub-lot has been taken from a production lot.

### 10.2.2 Special cases

a. If a hybrid microcircuit contains Beryllium oxide substrates or carriers, it shall be marked with the notation: « Contains BeO », or in the case of insufficient space on the package, indicate only « BeO ».

b. If a hybrid microcircuit is sensitive to electrostatic discharge, the ESD sensitivity classification shall be marked on the package.

## 10.3 Screening

### 10.3.1 General

a. The screening test sequence for FM hybrid circuits shall, as a minimum, conform to the requirements of Figure 10-1.

b. Two nominal levels (level 1 or level 2) shall be chosen depending on the project's mission characteristics

NOTE For example, quality level, or in-orbit lifetime.

c. The sequence of all tests to be performed shall be as given in Figure 10-1 unless the manufacturer has formally requested and obtained permission from the customer to deviate from this sequence.

d. All hybrids for delivery and all hybrids used for environmental and endurance tests shall meet all of the relevant screening test sequence requirements.

e. Any hybrid that does not meet these requirements shall be removed from the lot.

**Final production step except encapsulation**

↓

| Test no. | Inspection and screening test | Specification and test method | Test condition | Sample size | Testing level 1 | Testing level 2 |
|---|---|---|---|---|---|---|
| 1 | Thermographic | See 10.3.2 | | 1 piece | R | |
| 2 | Non-destructive bond pull | MIL-STD-883 Method 2023 | | 100 % | O | |
| 3 | Pre-seal burn-in | See 10.3.3 | See detail specification | 100 % | O | O |
| 4 | Electrical test | In conformance with manufacturing specification | | 100 % | O | O |
| 5 | Photograph of circuit | See 10.3.4 | | 1 piece | O | |
| 6 | Pre-cap visual inspection | MIL-STD-883 Method 2017 Class K | | 100 % | R | R |

Key: R = Required O = Optional

**Vacuum bake-out: in conformance with PID**

↓

*(continued)*

**Figure 10-1: Screening test sequence**

**Encapsulation / in conformance with PID**

↓

| Test no. | Inspection and screening test | Specification and test method | Test condition | Sample size | Testing level 1 | Testing level 2 |
|---|---|---|---|---|---|---|
| 7 | Stabilization bake | MIL-STD-883 Method 1008 | Condition B 72 hours | 100 % | O | O |
| 8 | Thermal cycling | MIL-STD-883 Method 1010 | Condition B 10 cycles | 100 % | R | R |
| 9 | Mechanical shock or constant acceleration | MIL-STD-883 Method 2002 or 2001 | Y1 axis only (see 10.3.5) | 100 % | R | R |
| 10 | Particle impact noise detection (PIND) | MIL-STD-883 Method 2020 specification | Condition A (see 10.3.6) | 100 % | R | R |
| 11 | Fine leak | MIL-STD-883 Method 1014 | Condition A2 (see 10.3.7) | 100 % | O | O |
| 12 | Gross leak | MIL-STD-883 Method 1014 | Condition C1 or C2 (see 10.3.7) | 100 % | O | O |
| 13 | Physical dimensions | MIL-STD-883 Method 2016 | See 10.3.8 | 3 hybrids | R | R |

Key: R = Required O = Optional

↓

**Marking and serialization**

↓

*(continued)*

**Figure 10-1: Screening test sequence (Part 2)**

| Test No. | Inspection and screening test | Specification and test method | Test condition | Sample size | Testing level 1 | Testing level 2 |
|---|---|---|---|---|---|---|
| 14 | Pre burn-in electrical measurements | Detail specification Table 4 and Table 2 | Ambient temperature | 100 % | R<br>Read and record | R<br>Go/no go |
| 15 | Burn-in | Detail specification | Detail specification Table 5<br>See 10.3.9 | 100 % | R<br>240 h | R<br>168 h |
| 16 | Parameter drift calculation | Detail specification Table 4 | | 100 % | R<br>Read and record | |
| 17 | Electrical measurements ambient temperature | Detail specification Table 2 | | 100 % | R<br>Read and record | R<br>Go/no go |
| 18 | Electrical measurements high and low temperature | Detail specification Table 3 | | 100 % | R<br>Read and record | R<br>Go/no go |
| 19 | Radiographic inspection | MIL-STD-883 Method 2012 | See 10.3.10 | 100 % | R | R |
| 20 | Fine leak | MIL-STD-883 Method 1014 | Condition A2 | 100 % | R | R |
| 21 | Gross leak | MIL-STD-883 Method 1014 | Condition C1 or C2 | 100 % | R | R |
| 22 | External visual inspection | MIL-STD-883 Method 2009.8 | | 100 % | R | R |

Key: R = Required O = Optional

**Figure 10-1: Screening test sequence (Part 3)**

## 10.3.2 Thermographic test

a. Thermographic test shall be performed only to hybrid circuits where thermal studies or design approval tests during CTA activities have indicated the existence of hot spots at maximum rated power.

b. A point at which the delta temperature between the surface and the case is higher than 30 °C for active components, or higher than 60 °C for passive components, shall be considered as a hot spot.

c. Lot by lot, a suitable evaluation method shall be used to evaluate the temperature reached by the critical components when powered and thus demonstrate thermal resistance reproducibility throughout the assembly process.

d. If an infrared microscope is used, the circuit shall be coated to obtain a uniform emissivity factor from the metallization surfaces.

NOTE This test is destructive.

### 10.3.3 Pre-seal burn-in

a. Pre-seal burn-in need not be performed.

NOTE Pre-seal burn-in is optional.

b. If Pre-seal burn-in test is performed, the test procedure, the environment and duration shall be approved as part of the line capability approval activity by the approving authority.

c. Pre-seal burn-in shall be performed in an inert atmosphere.

d. The total burn-in time shall not be less than 240 h.

e. The total burn-in time may be divided between pre-seal burn-in and post-seal burn-in, provided that the latter lasts 144 h or more.

### 10.3.4 Photograph of circuits

a. If a photograph is not made as part of the screening, it shall be done during the CTA or during the manufacturing of the first production lot.

b. Magnification shall be such that the layout can be easily identified.

c. The same circuit shall also be photographed at a magnification at which the chip surface pattern is easily identifiable.

### 10.3.5 Conditions for constant acceleration and mechanical shock

a. The test conditions for constant acceleration and mechanical shock shall be a function of the hybrid package size, as specified in Table 10-1.

**Table 10-1: Test conditions for constant acceleration and mechanical shock**

| Hybrid package size | Constant acceleration | Mechanical shock |
|---|---|---|
| Up to 25,4 mm × 25,4 mm | 10 000 *g*<br>(Condition B) | 1 500 *g* – 0,5 ms<br>(Condition B) |
| From 25,4 mm × 25,4 mm<br>Up to 25,4 mm × 50,8 mm | 5 000 *g*<br>(Condition A) | 1 500 *g* – 0,5 ms<br>(Condition B) |
| Above 25,4 mm × 50,8 mm | Not applicable | 1 000 *g* – 0,5 ms |
| NOTE: These conditions can be modified on a case by case basis through a duly justified RFD (request for deviation). | | |

### 10.3.6 Test condition for PIND

a. This test may be waived by the approving authority in the case of internally coated hybrids.

### 10.3.7 Leak tests

a. Pressurization and time shall depend on the package sizes in conformance with MIL-STD-883 Method 1014.

b. The exact test condition shall be as specified in the PID.

c. The applicable package test condition shall be as specified in the Detail Specification.

NOTE This test can be performed, at this point in the sequence, at the manufacturer's discretion.

### 10.3.8 Physical dimensions

a. Physical dimension measurements may be omitted where the hybrid manufacturer is also the customer.

### 10.3.9 Burn-in test

a. Taking into account the power applied, the oven temperature shall be defined so that the junction temperature of the most stressed active chip component shall be between 125 °C and 150 °C.

b. If another temperature is selected, the burn-in duration shall be adjusted in conformance with MIL-STD-883 method 1015.

### 10.3.10 Radiographic inspection

a. This inspection may be performed at any point during the test sequence.

NOTE The performance of this test depends on the technology.

b. This test may be omitted only in the case of aluminium wires and epoxy bonding of chips.

## 10.4 Lot rejection

### 10.4.1 Definition of failure modes

#### 10.4.1.1 General

a. A hybrid shall be considered as having failed if it exhibits one or more of the failure modes described in clauses 10.4.1.2 to 10.4.1.5.

#### 10.4.1.2 Parameter drift failure

a. When the changes between the 0 hour and the 240 hour measurements of burn-in, based on the 0 hour reading, are larger than the specified delta limit shall be considered a parameter drift failure.

b. The acceptable delta limit is specified in Table 4 of the hybrid detail specification specified in Annex B.

#### 10.4.1.3 Parameter limit failure

a. When one or more parameters exceed the limits shown in Table 2 or Table 3 of the hybrid detail specification (specified in Annex B) shall be considered a parameter limit failure.

b. Any hybrid, that exhibits a limit failure before burn-in shall be rejected, but shall not be counted when determining the lot rejection.

#### 10.4.1.4 PIND failure

a. A hybrid which when tested in conformance with the provisions of MIL-STD-883, Method 2020 Condition A, produces noise bursts as detected by any of the three detection systems shall be considered as a PIND failure.

b. Background noise may be excluded, except those caused by the shock blows, during the monitoring periods.

#### 10.4.1.5 Other Failures

a. A hybrid shall be considered to be a failure if any of the following occur:

1. catastrophic failure,
2. mechanical failure,
3. handling failure,
4. lost component.

### 10.4.2 Criteria for lot rejection

a. For parameter drift failure, if the number of failed hybrids exceeds 5 % PDA of the number of hybrids submitted to the burn-in and electrical measurements, the lot shall be rejected.

b. If the cumulative total of parameter drift failures (see clause 10.4.1.2) and parameter limit failures (see clause 10.4.1.3) exceeds 10 % PDA of the number of hybrids submitted to the burn-in and electrical measurements, the lot shall be rejected.

c. For PIND testing, the hybrids the following shall be perform:

1. Submit to testing a maximum of 5 times.
2. After each run, remove defective hybrids from the lot.
3. Accept the lot on any of the 5 runs if the percentage of defective devices is less than 1 % of the devices tested (or 1, whichever is greater).
4. Reject the lots that do not meet the 1 % PDA on the 5$^{th}$ run or which at any time exceed 25 % cumulative failures.

### 10.4.3 Disposition of rejected lots

a. Rejected lots shall be segregated and kept in bonded store for further investigation at the customer's discretion.

## 10.5 Repair provisions

### 10.5.1 General

a. All repair processes carried out on hybrid circuits shall be approved and performed in conformance with the procedures specified in the approved PID.

### 10.5.2 Element replacement

a. Any polymer attached element may be replaced twice at a given location on any hybrid circuit.

b. Any metallic attached element may be replaced once at a given location.

c. The total number of replacements shall be limited to a maximum of 10 % of the total number of elements in the hybrid circuit.

d. Except for substrates attached to a package using mechanical fasteners for which the replacement number is not limited, adhesive bonded substrates may be removed, replaced or put into a new package once.

e. There shall be a maximum of 4 heating cycles for element removal.

f. It shall be demonstrated that the reliability of the remaining elements is not impacted.

### 10.5.3 Wire re-bonding

a. Re-bonding may be performed for chip to substrate, substrate to package pins, and substrate pad to substrate pad wires.

b. All re-bonds shall be placed on at least 50 % undisturbed metal (excluding probe marks that do not expose underlying metallization or oxide).

c. If the first bond is not successful, no more than one re-bond attempt shall be made at the same place.

d. Re-bonds shall not touch any area of exposed oxide caused by lifted or blistered metal.

e. The total number of chip to substrate or substrate pad to substrate pad wire re-bondings shall be limited to a maximum of 10 % of the total number of wires on the hybrid circuit.

f. The total number of substrate to package pin wire re-bondings shall be limited to a maximum of 15 % of the total number of wires in the hybrid circuit.

### 10.5.4 Compound bonding

a. Compound bonding shall not be performed for other than gold.

b. Compound bonds shall be limited to one bond over the original bond, wire, or ribbon.

c. When a compound bond is used to secure an existing bond, then the bond shall be non-destructively pull tested.

d. Only monometallic compound bonds of the same size wire or ribbon shall be used (i.e. the original bond wire and that used for compound bonding shall be of the same material).

### 10.5.5 Delidding of hybrid circuits

a. If hybrid circuits may be delidded and relidded for repair:

   1. The customer is informed before the operation.

   2. No more than one delid-relid cycle is performed.

b. When hybrid circuits may be delidded and relidded for_repair, suitable screening tests shall be performed on the delidded-relidded hybrid circuits.

c. These screening tests shall be defined at the stage when the delidding-relidding takes place and depend on the type of_repair performed.

# 11
# Customer inspection and review

a. The degree of customer involvement in the approval of documents and inspections shall be agreed between the customer and the manufacturer at the time of contract negotiation.

b. The customer shall approve the following documents prepared by the manufacturer:

   1. the detail specification for the actual hybrid circuit type;
   2. the PAD;
   3. the technology identification form (for category 2 only);
   4. any nonconformance documents.

c. The customer shall be invited to the following key inspections:

   1. pre-cap visual inspection;
   2. final acceptance of the hybrids after the performance of all tests including LAT.

d. The customer may delegate another authority to carry out the actual inspections in agreement with the manufacturer.

# 12
# Lot acceptance tests for hybrid circuits

## 12.1 General

### 12.1.1 Overview

Quality acceptance of the production of the FM hybrid circuits depends on the category of the manufacturer (category 1 or 2) as defined in clause 5.

### 12.1.2 Samples

a. Lot acceptance testing shall be carried out on samples of circuits having passed a complete screening sequence.

b. Lot acceptance test shall be performed on one of the following:

— Option 1: production lot control.

— Option 2: production lines under TRB management with periodic testing and statistical process control.

NOTE A technology review board (TRB) is a formal group, at manufacturer level, where the design, materials and parts procurement, manufacturing, testing, reliability, and quality assurance functions are represented. The mission of this group is to:

- define and implement a quality management plan for continuous quality improvement;
- identify and analyse the new needs, improvement of the process and nonconformances;
- define and implement the associated validation, preventive and corrective actions;
- inform and justify the evolutions and actions taken on the hybrid production line to the approving authority.

c. The option chosen by the manufacturer shall be declared in the PID.

## 12.2 Category 1 manufacturer

### 12.2.1 Option 1: Production lot control

#### 12.2.1.1 Sampling

a. For each production lot of hybrid circuits, the number of samples depends on the lot size as given in Table 12-1.

b. For a given type of hybrid, there shall be n samples for the first production lot and n-1 samples for the subsequent production lots of the same hybrid type.

**Table 12-1: Sample size for hybrids lot acceptance tests**

| Lot size | Sample size for the 1st production lot (n) | Sample size for the subsequent production lot(s) (m) |
|---|---|---|
| 1 - 25 | 2 | 1 |
| 26 - 50 | 3 | 2 |
| 51 - 90 | 4 | 3 |
| > 90 | 5 | 4 |

#### 12.2.1.2 Lot acceptance tests

a. The LAT samples shall be submitted to the test sequence given in Table 12-2.

**Table 12-2: Lot acceptance tests and sample size**

| Test sequence | Number of samples | | Test conditions |
|---|---|---|---|
| | 1st lot | Subsequent lots | |
| Internal water vapour content | 1 | 0 | Before delidding of reference DPA sample in conformance with MIL-STD-883 Method 1018. |
| Reference DPA after screening sequence | 1 | 0 | In conformance with DPA sequence defined in clause 14. |
| Accelerated life test | n-1 | m | 1 000 h life test at 125 °C in conformance with Table 7 of the detail specification (Annex B) (or equivalent time-temperature in conformance with MIL-STD-883 Method 1005). |
| Electrical measurements | n-1 | m | In conformance with Table 2 and Table 6 of the detail specification (Annex B). |
| DPA after life test | 1 | 1 | In conformance with DPA sequence defined in clause 14. |

#### 12.2.1.3 Acceptance criteria

a. The production lot shall be accepted if all the following conditions are fulfilled:

1. The PDA of each production lot is below the limit as per 10.4.2.
2. No failure on the internal water vapour content test.
3. No failure on the reference DPA (in the case of the first production lot).
4. No failure on the electrical measurements after the life-test.
5. No failure on the DPA sample submitted to life test.

#### 12.2.1.4 Manufacturer pending approval by the approving authority

a. For a manufacturer pending capability approval, the lot(s) produced and approved in conformance with the procedure described above shall not be delivered to the project until the approving authority has approved the production line.

### 12.2.2 Option 2: Lines under TRB management and statistical process control

#### 12.2.2.1 General

a. Category 1 manufacturers using this option shall implement a TRB management and statistical process control system that is approved by the approving authority.

b. Also, Category 1 manufacturers using this option shall establish a statistical process control on the main processes of the manufacturing line.

c. The Ppk of a process is the long-term capability of the process which reflects the process centering and variability with respect to specification requirements, being the Ppk defined as follows:

$$Ppk = \min\left\{\frac{(Ts - m)}{3\sigma}, \frac{(m - Ti)}{3\sigma}\right\}$$

where

*Ts* is the upper limit of the specification;

*m* is the mean value;

*Ti* is the lower limit of the specification;

σ is the standard deviation.

NOTE See also references [1] and [2].

d. The Ppk value shall be higher than 1,33 to demonstrate capability of each process.

NOTE The higher the Ppk number, the more capable the process.

e. Under these conditions, and after approval by the approving authority, a lot acceptance test of the hybrids may be applied to the hybrid technological family through a standard evaluation circuit (SEC) with the conditions given in clause 12.2.2.2 to 12.2.2.4.

NOTE See Annex D for technological family definition and examples.

#### 12.2.2.2 Sampling a standard evaluation circuit (SEC)

a. For each set of production lots grouped in one representative production lot, 1 % of all hybrid circuits concerned shall be sampled with a minimum of one sample manufactured within a maximum period of 3 months.

#### 12.2.2.3 Production lot acceptance tests

a. The SEC samples shall be submitted to the test sequence given in Table 12-3.

#### 12.2.2.4 Acceptance criteria

a. The representative production lot shall not be accepted unless all the following conditions are fulfilled:

1. The PDA on each representative production lot is below the limit as per 10.4.2.
2. The SPC performed during the manufacturing of the representative production lot are under the fixed limits.
3. There is no failure in the bond pull test and shear test.
4. There is no failure in the seal test and PIND test after ageing.

## 12.3 Category 2 manufacturer (validated for the project)

a. The sequence of lot acceptance tests for the first production lot shall be as in Figure 12-1.

b. For subsequent lots and on condition that the test results for the initial lots are satisfactory, the lot acceptance procedure (category 1 manufacturer, option 1) in conformance with clause 12.2.1 shall be applied for each type.

c. The specifications and conditions for the tests specified in Figure 12-1 shall be as given in Table 12-4.

**Table 12-3: Production acceptance tests and sampling**

| Test sequence | SEC number of samples | Test conditions |
|---|---|---|
| Seal test | 1 % | MIL-STD-883/1014 A2<br>MIL-STD-883/1014 C |
| PIND test | 1 % | MIL-STD-883 / 2020 A |
| Thermal cycling | 1 % | MIL-STD-883 / 1010<br>(-55 °C - 125 °C for 100 cycles) |
| External visual inspection | 1 % | MIL-STD-883 / 2009.8 |
| Seal test | 1 % | MIL-STD-883 / 1014 A2<br>MIL-STD-883 / 1014 C |
| PIND test | 1 % | MIL-STD-883/ 2020 A |
| Internal visual inspection | 1 % | MIL-STD-883 / 2017 S<br>MIL-STD-883 / 2010 A<br>MIL-STD-750 / 2072<br>MIL-STD-750 / 2073 |
| Bond pull test | 1 % (50 % wires) | MIL-STD-883 / 2011 |
| Die shear test | 1 % (50 % chips) | MIL-STD-883 / 2019 |
| High temperature storage | 1 % | (1h at 300 °C or equivalent time-temperature as defined in 8.3.2) |
| Bond pull test | 1 % (remaining wires) | MIL-STD-883 / 2011 |

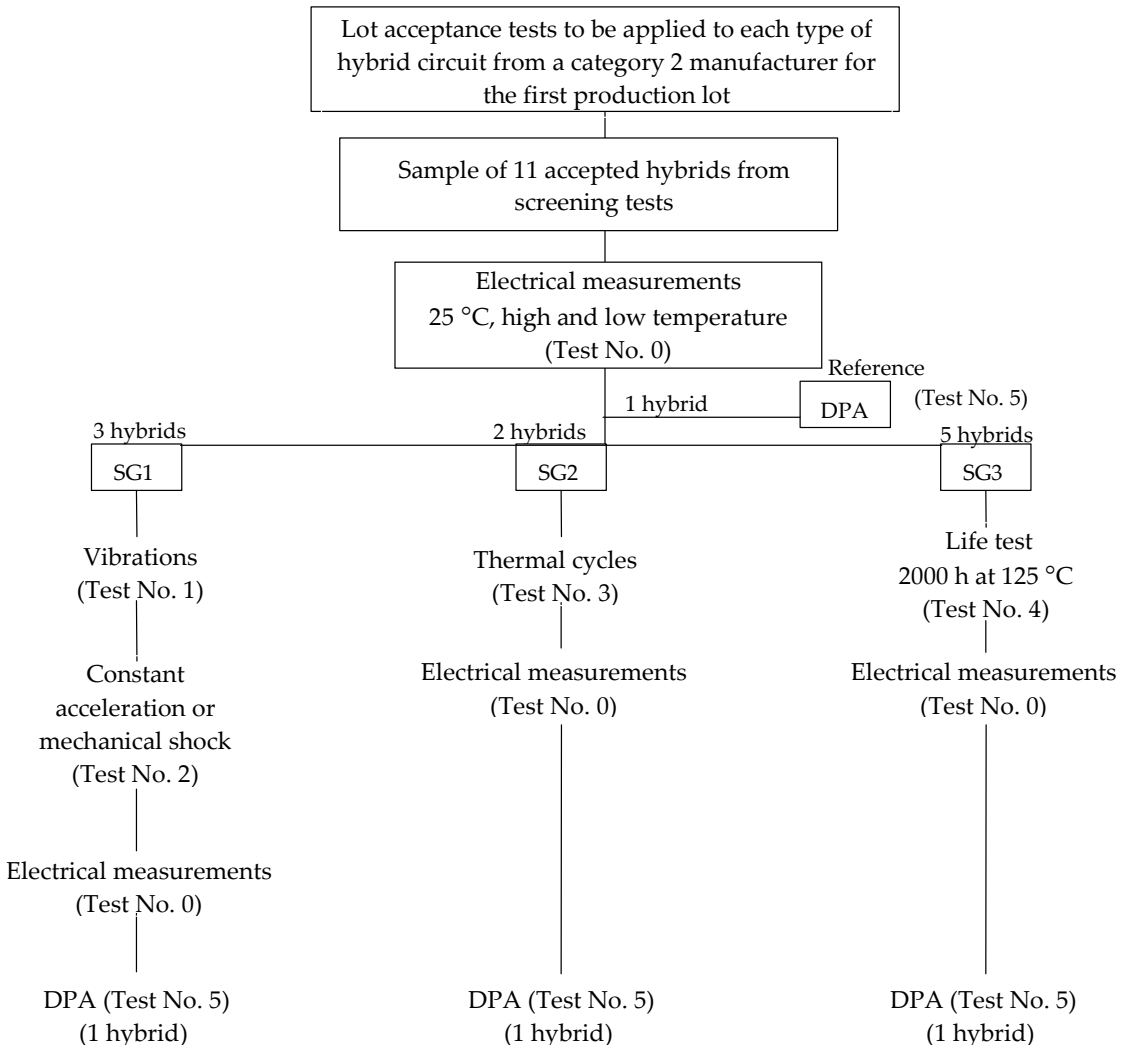



**Figure 12-1: Lot acceptance tests for the first production lot manufactured by a category 2 manufacturer**

**Table 12-4: Definition of tests**

| Test No. | Test designation | Applicable specification MIL-STD-883 | Comments |
|---|---|---|---|
| 0 | Electrical measurements at 3 temperatures (ambient, high and low) | | In conformance with detail specification |
| 1 | Vibrations | Method 2007 condition A | Along X and Y axis |
| 2 | Constant acceleration or mechanical shocks | Method 2001 condition A or B or Method 2002 condition B (see 10.3.5) | Along Y1 axis<br>Along Y1 axis (substrate attach strength) |
| 3 | Thermal cycling | Method 1010 condition B | 100 cycles |
| 4 | Life test | Method 1005 | Project LAT extended to 2 000 h at 125 °C |
| 5 | DPA shall be conducted on 1 reference piece and 3 pieces (SG1, SG2, and SG3) in conformance with clause 14.<br>In addition, this test sequence shall be conducted on one piece from SG1 or SG2: | | |
| | - marking permanency; | Method 2015 | |
| | - lead integrity; | Method 2004 condition B2 | |
| | - solderability; | Method 2003 | |
| | - internal water vapour content. | Method 1018 procedure 1<br>5 000 × $10^{-6}$ parts water vapour maximum at 100 °C | |

# 13
# Hybrid delivery and data package

## 13.1 General

a. The delivery of hybrid items shall be agreed with the customer at the contract negotiation stage.

b. Delivery shall include the following items:

1. the delivery lot;
2. documentation conforming to the requirements of clause 13.2.

## 13.2 Data documentation

### 13.2.1 General

a. Each delivery of a hybrid shall include a data documentation package.

b. If one is not delivered, all data shall be retained by the manufacturer for a minimum of 5 years, and available during this time to the customer for review upon request.

c. Depending on the testing level and lot acceptance testing specified, this package shall be agreed with the customer and constitute the following:

1. Cover Sheet (or sheets).
2. Certificate of conformity (COC).
3. MIP reports.
4. RFWs, RFDs, NCRs.
5. CTA test data (if applicable).
6. Burn-in and electrical measurement data with delta values.
7. Lot acceptance test data including DPA reports (when applicable).
8. PDA calculation.
9. Photographs and X-ray pictures on request.

### 13.2.2 Cover sheets

a. The cover sheet(s) of the data documentation package shall include as a minimum:

1. Manufacturer's name and location of manufacturing plant.
2. Date and manufacturer's signature.
3. Hybrid circuit type identification.
4. Reference to the generic and detail specification, including issue and date.
5. Reference to the manufacturing dossier.
6. Lot identification.
7. Reference to the purchase order.

### 13.2.3 Certificate of conformity

a. The certificate of conformity shall include as a minimum:

1. Manufacturer's name and location of manufacturing plant.
2. Date and manufacturer's QA signature.
3. Serial numbers of hybrids delivered.
4. Reference to the applicable PID including issue and date.
5. Reference to the detail specification, including issue and date.

## 13.3 Packaging and despatch

a. Hybrids shall be packaged and despatched in conformance with the requirements of ESCC 20600.

# 14
# DPA test sequence

a. DPA test sequence depends on the technology and shall be performed in conformance with the following methods:

1. External visual inspection, MIL-STD-883 Method 2009.8.
2. X-rays (if soldered items or gold wires are present), MIL-STD-883 Method 2012.
3. SAM inspection, MIL-STD-883 Method 2030.
4. Seal test, MIL-STD-883 Method 1014 Condition A2 – Condition C.
5. PIND test, MIL-STD-883 Method 2020 Condition A.
6. Internal visual inspection, MIL-STD-883 Method 2017 Class K, MIL-STD-883 Method 2010 Condition A, MIL-STD-750 Method 2072, MIL-STD-750 Method 2073, MIL-STD-883 Method 2032.
7. SEM inspection, MIL-STD-883 Method 2018 (Provide photos of typical assemblies and possible anomalies).
8. Bond pull test, MIL-STD-883 Method 2011 Condition D (Pull all wires).
9. Die shear test, MIL-STD-883 Method 2019 (Shear all chips).

# Annex A (normative) Hybrid circuit technology identification form (HTIF) - DRD

## A.1 DRD identification

### A.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-60-05, requirements 6.2.1a and 6.2.4.2b.

### A.1.2 Purpose and objective

The hybrid circuit technology identification form (HTIF) is used by a manufacturer (whatever his status, category 1 or 2, regarding the capability approval) wishing to produce or to use a hybrid circuit in a space project, to provide the customer with the appropriate information to assess the technology.

Category 1 manufacturers need not to deliver formally the HTIF to the customer.

## A.2 Expected response

### A.2.1 Scope and content

#### <1> General

a. The HTIF shall be as shown in Table A-1.

**Table A-1: Hybrid circuit technology identification form (HTIF)**

<table>
<tr><td colspan="3">Project:<br><br>Manufacturer/country:</td></tr>
<tr><td>HTIF reference:</td><td>Revision:</td><td>Date:</td></tr>
<tr><td colspan="3">Hybrid circuit identification<br><br>Hybrid name:<br><br>Hybrid reference or code:<br><br>Function:<br><br>Maximum power dissipation:<br><br>Maximum frequency of operation:</td></tr>
<tr><td></td><td colspan="2">Hybrid manufacturer product assurance manager</td></tr>
<tr><td>Name:<br><br>Date:<br><br>Signature:</td><td colspan="2"></td></tr>
</table>

**1. Substrate(s)**

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Material | | C(1) NC(2) | |
| Supplier | | C NC | |
| Number of substrates in the package | | C NC | |
| Dimensions (mm) L × W × T | | C NC | |

Comments

**Important: Indicate clearly if beryllium oxide is used as substrate or carrier material**

**2. Conductors**

**2.1 Thin film**

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Deposition process | | C NC | |
| Material | | C NC | |
| Minimum (design) conductor width (mm) | | C NC | |
| Minimum (design) distance between conductors (mm) | | C NC | |

Comments

**2.2 Thick film**

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Material | | C NC | |
| Type and Supplier | | C NC | |
| Number of layers | | C NC | |
| Minimum (design) conductor width (mm) | | C NC | |
| Minimum (design) distance between conductors (mm) | | C NC | |
| Via's dimensions (mm) | | C NC | |

Comments

**3. Resistors**

**3.1. Thin film**

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Material | | C NC | |
| Resistivity (Ωm) | | C NC | |
| Number of resistors) | | C NC | |
| Trimming method | | C NC | |
| Comments | | | |

**3.2 Thick film**

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Material/Type | | C NC | |
| Supplier | | C NC | |
| Minimum and maximum resistivity (Ωm) | | C NC | |
| Number of resistors for each resistivity | | C NC | |
| Resistors printed on dielectric | | C NC | |
| Trimming method | | C NC | |
| Comments | | | |

**4. Dielectric/overglaze layers**

**4.1 Thin film**

| | | PID Conformance (C) | If NC references of specifications related to the material/process |
|---|---|---|---|
| Material/Type | | C NC | |
| Use (see Note 3) | | C NC | |
| Comments | | | |

**4.2 Thick film**

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Material/Type | | C NC | |
| Supplier | | C NC | |
| Use (see Note 3) | | C NC | |
| Comments | | | |

**5. Mounting of passive chips**

| | | | | |
|---|---|---|---|---|
| Chip type (See Note 4) | | | | |
| Chip size (mm) | | | | |
| Metallization of chip termination | | | | |

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Chip type | | C NC | |
| Method of mechanical attachment | | C NC | |
| Material | | C NC | |
| Supplier | | C NC | |
| Maximum chip size | | C NC | |
| Method of electrical connection | | C NC | |

Comments
(see also Part 10 of this form)

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Chip type | | C NC | |
| Method of mechanical attachment | | C NC | |
| Material | | C NC | |
| Supplier | | C NC | |
| Method of electrical connection | | C NC | |

Comments
(see also Part 10 of this form)

**6. Mounting of active chips**

| | | | | |
|---|---|---|---|---|
| Chip type (see Note 5) | | | | |
| Chip size (mm) | | | | |
| Metallization back side of chip | | | | |
| Metallization top side of chip (see Note 6) | | | | |

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Chip type | | C NC | |
| Method of mechanical attachment | | C NC | |
| - Material | | C NC | |
| - Supplier | | C NC | |
| - Maximum chip size | | C NC | |
| Use of a carrier<br>- Material<br>- Size (mm)<br>- Supplier | | C NC | |
| Method of electrical connection | | C NC | |

Comments
(see also Part 10 of this form)

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Chip type | | C NC | |
| Method of mechanical attachment | | C NC | |
| - Material | | C NC | |
| - Supplier | | C NC | |
| - Maximum chip size | | C NC | |
| Use of a carrier<br>- Material<br>- Size (mm)<br>- Supplier | | C NC | |
| Method of electrical connection | | C NC | |

Comments
(see also Part 10 of this form)

**7. Mounting of encapsulated components**

| | | | | |
|---|---|---|---|---|
| Components type | | | | |
| Package type | | | | |
| Metallization | | | | |

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Method of mechanical attachment | | C NC | |
| - Material | | C NC | |
| - Supplier | | C NC | |
| - Maximum part size | | C NC | |
| Method of electrical connection | | C NC | |

Comments
(see also Part 10 of this form)

## 8. Wire bonding

### 8.1 From active chips to substrate

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Wire material | | C NC | |
| Supplier | | C NC | |
| Wire diameter (µm) | | C NC | |
| Bonding method (see Note 7) | | C NC | |

Comments

### 8.2 From passive chips to substrate

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Wire material | | C NC | |
| Supplier | | C NC | |
| Wire diameter (µm) | | C NC | |
| Bonding method | | C NC | |

Comments

### 8.3 From substrate to package posts/leads

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Wire material | | C NC | |
| Supplier | | C NC | |
| Wire diameter (µm) | | C NC | |
| Bonding method | | C NC | |

Comments

### 8.4 From substrate to substrate

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Wire material | | C NC | |
| Supplier | | C NC | |
| Wire diameter (µm) | | C NC | |
| Bonding method | | C NC | |

Comments

**9. Encapsulation**

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Package type (see Note 8) | | C NC | |
| External dimensions (mm) | | C NC | |
| Body (bottom-frame) | | C NC | |
| - base material | | | |
| - plating material/type (see Note 9) | | | |
| Leads | | C NC | |
| - base material | | | |
| - plating material/type | | | |
| External dimensions (mm) | | C NC | |
| Number of leads | | C NC | |
| Feed-through type (see Note 10) | | C NC | |
| | | C NC | |
| Supplier | | C NC | |
| Lid/Cover | | | |
| - base material | | C NC | |
| - plating material/type | | | |

| | | PID Conformance (C) | If NC, references of specifications related to the material/process |
|---|---|---|---|
| Substrate to package attachment method | | C NC | |
| Material | | C NC | |
| Supplier | | C NC | |
| Sealing method | | C NC | |
| Comments | | | |

**10. Added-on component list**

| | Function | Type | Total number per type | Supplier | Comments |
|---|---|---|---|---|---|
| Passive chips | | | | | |
| Active chips | | | | | |
| Encapsulated components | | | | | |
| Miscellaneous | | | | | |

**Notes:**

0: General: write NA for not applicable - information.

1: C = in conformance with the relevant PID.

2: NC = no conformance with the relevant PID.

3: Indicate whether used, for example, for multilayer construction, capacitor realization, resistors overglaze, wire cross-over protection.

4: Passive chip type, can include:
- chip capacitor (for example multilayer ceramic capacitor chip, tantalum chip capacitor other type);
- chip resistor (for example thick film resistor chip (e.g. Alumina), thin film resistor chip (e.g. Alumina, Silicon);
- miniature coils (e.g. inductor chip, transformer);

5: Active chip type, e.g. diode, transistor, integrated circuit.

6: Indicate whether the chip surface is passivated.

7: Wire bonding method can be, for example, thermocompression, ultrasonic, thermosonic, parallel gap welding.

8: Package type can be, for example, metallic or ceramic or platform plug-in, solid sidewall plug-in, flat pack.
Indicate also if low power or high power.

9: Plating type can be, for example, electrolytic or electroless.

10: Feed-through type: for glass-to-metal seals, indicate if matched seals or compression seals.

#### <2> Hybrid circuit topography

a. The HTIF shall include a photograph of the hybrid circuit showing the substrate(s) and all conductor patterns and active or passive elements deposited on it, as well as the semiconductor dies, as applicable (format ~ 20 cm × 27 cm).

b. This requirement may also be satisfied by the manufacturer's assembly drawing with a minimum magnification of 10×.

### A.2.2 Special remarks

a. For category 2 manufacturers, the HTIF shall be included as part of the PAD.

# Annex B (normative) Format of the detail specification of a hybrid circuit - DRD

## B.1 DRD identification

### B.1.1 Requirement identification and source document

This DRD is called up from ECSS-Q-ST-60-05, requirement 7.2a.

### B.1.2 Purpose and objective

The detail specification of a hybrid circuit is a document prepared by the manufacturer to provide the technical details of the hybrid circuit.

## B.2 Expected response

### B.2.1 Response identification

a. The detail specification shall include a version index and a change form for configuration management.

b. A cover page shall include a brief definition of the function performed and the product's technological characteristics.

c. The detail specification for each type of hybrid circuit shall constitute the tables and figures specified in B.2.2.

### B.2.2 Scope and content

#### <1> Table 1: Maximum ratings

a. This table shall include the limiting electrical, mechanical and thermal parameters.

b. In particular, it shall specify the recommended methods for mounting the hybrid to the next level of assembly.

c. The maximum values for the assembly process time and temperature shall be specified.

d. ESD sensitivity classification shall also be mentioned if applicable.

e. Radiation tolerance shall be mentioned if applicable.

### <2> Table 2: Electrical measurements at ambient temperature with static and dynamic parameters

a. This table shall list the parameters measured, their units, symbol, measurement conditions, and minimum and maximum values.

### <3> Table 3: Electrical measurements at high and low temperatures

a. This table shall list the parameters measured at high and low level temperatures.

b. The high and low temperature values shall be taken by default +125 °C and -55 °C.

### <4> Table 4: Parameter drifts

a. This table shall list the electrical parameters before and after burn-in with the maximum drift allowed.

### <5> Table 5: Burn-in conditions

a. This table shall list the oven temperature and power applied to comply with ECSS-Q-ST-60-05, clause 10.3.9.

b. This table shall be completed by a diagram defining the circuit excitation conditions.

### <6> Table 6: Electrical measurements after endurance tests

a. This table shall list the parameters measured, and the minimum and maximum values tolerated, after the life test at the ambient temperature and at high and low temperatures.

### <7> Table 7: Life-test conditions

a. This table shall list the oven temperature and power applied to comply with ECSS-Q-ST-60-05, clause 10.3.9.

b. A diagram defining the electrical excitation conditions, if these are different from Table 5, shall complete this table

### <8> Table 8: Content of the DPAs

a. This table shall detail the content of the DPAs.

**<9> Figure 1: Drawing of package**

a. The detail specification shall include a drawing of package and dimensions with tolerance indications.

**<10> Figure 2: Electrical diagram**

a. The detail specification shall include an electrical diagram of the hybrid circuit with assignment of inputs and outputs.

### B.2.3 Special remarks

None.

# Annex C (normative)
# Similarity form - DRD

## C.1 DRD identification

### C.1.1 Requirement identification and source document

This DRD is called up from ECSS-Q-ST-60-05, requirement 7.3.1.2a.

### C.1.2 Purpose and objective

The similarity form is a proposal prepared by the supplier, to be used by the customer in combination with the hybrid circuit technology identification form (HTIF, see ECSS-Q-ST-60-05 Annex A) for the purpose of determining whether design approval for the new circuit can be acquired through similarity with a previously approved circuit type (referred to as the reference circuit).

## C.2 Expected response

### C.2.1 Scope and content

a. The Similarity form shall be as in Table C-1.

**Table C-1 Similarity form**

| Identification | New circuit | Reference circuit |
|---|---|---|
| Type-reference | | |
| Year of manufacture | | |
| Detail specification | | |
| HTIF | | |

| Description of the electrical function |
|---|
| New circuit |
| Reference circuit |

| Similarity criteria | New circuit | Reference circuit |
|---|---|---|
| Maximum power density<br><br>Maximum use frequency<br><br>Maximum voltage<br><br>Maximum current<br><br>Number of discrete active chips mounted<br><br>Number of integrated circuit chips mounted<br><br>Number of passive chips mounted<br><br>Maximum size of active chips<br><br>Maximum size of passive chips (specify the type) | | |
| Maximum electrical charge for the most stressed chips | | |
| Maximum electrical charge on the technological level (e.g. wires, dielectric, printed conductors) | | |

### C.2.2 Special remarks

a. The similarity form shall be enclosed with the request for use (PAD).

# Annex D (informative) Technological family

## D.1 Definition of a technological family

A hybrid technology family includes all the hybrids manufactured with the same materials and processes and the same assembly sequence (flow chart) defined in the PID.

The aspect of electrical function is not taken into account; only the manufacturing processes using the same materials and the same manufacturing equipment are considered.

## D.2 Example of a hybrid technological family

Hybrids are considered to be part of the same technological family if they have the following characteristics:

- Use a plug-in package of a defined material manufactured by manufacturer A.
- Use thick film processing on substrates (manufacturer B) with C, D, E inks and manufacturing equipment U.
- Have gluing of substrates using glue F and manufacturing equipment V.
- Have conductive gluing of parts using glue G and manufacturing equipment W.
- Have non-conductive gluing of parts using glue H and manufacturing equipment W.
- Have wiring by thermosonic bonding using 25 µm gold wire (manufacturer I) and manufacturing equipment X.
- Have wiring by ultrasonic bonding using 25 µm aluminium wire (manufacturer J) and manufacturing equipment Y.
- Have sealing by parallel seam welding using machine Z.

In a family, the most complex hybrids are candidates for being representative of that technological family.

## D.3 Associated statistical process control (SPC) on processes and examples of parameters or characteristics under control

- SPC on thick film substrate manufacturing:
  - on process parameters, e.g. machine settings, temperature profile,
  - on product, e.g. layer adhesion, resistivity, dimensions.
- SPC on active and passive parts gluing:
  - on process parameters, e.g. machine settings, curing cycle,
  - on product, e.g. shear test.
- SPC on thermosonic or ultrasonic bonding wiring:
  - on process parameters, e.g. machine settings,
  - on product, e.g. footprint dimension, bond pull test, breakdown category.
- SPC on gluing of substrates:
  - on process parameters, e.g. machine settings, curing cycle,
  - on product, e.g. shear test.
- SPC on sealing with parallel seam machine:
  - on process parameters, e.g. machine settings, baking profile,
  - on product, e.g. seal test, internal water vapour content test.

# Annex E (informative) References

[1] *Introduction to Statistical Process Control*, Douglas C. Montgomery, John Wiley and Sons.

[2] *Appliquer la maitrise statistique des procédés MSP/SPC*, Maurice Pillet, 2nd Edition, Editions d'organisation.

# Bibliography


| | |
|---|---|
| ECSS-S-ST-00 | ECSS system — Description and implementation and general requirements |
| ESA-PSS-01-605 | Capability approval programme for hermetic thin-film hybrid microcircuits |
| ESA-PSS-01-606 | The capability approval programme for hermetic thick-film hybrid microcircuits |
| ESA-PSS-01-607 | Check list for thick-film hybrid microcircuits manufacturer and line survey |
| ESA-PSS-01-611 | Check list for thin-film hybrid microcircuits manufacturer and line survey |
| ESA-PSS-01-612 | Capability approval programme for microwave hybrid integrated circuits (MHICs) |